The LMX2572LPEVM is designed to evaluate the performance of LMX2572LP. This board consists of a LMX2572LP device.

The LMX2572LP is a low-power, high-performance wideband synthesizer that can generate any frequency from 12.5 MHz to 2 GHz without using an internal VCO doubler. The PLL delivers excellent performance while consuming just 70 mA from a single 3.3-V supply.

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Trademarks
All trademarks are the property of their respective owners.
1 LMX2572LPEVM Evaluation Module

1.1 Evaluation Module Contents

In the box, there is:

- One LMX2572LPEVM board (SV601308-004)
- One Reference PRO board (SV601349)
- Two SMA Male-to-Male adaptors (132168)
- One USB cable
- One 10-pin ribbon cable

1.2 Evaluation Setup Requirement

The evaluation requires the following hardware and software:

- A DC power supply
- A spectrum analyzer or a signal analyzer
- A PC running Windows 7 or more recent version
- An oscilloscope (optional)
- A high quality signal generator (optional)
- Texas Instruments Clocks and Synthesizers TICS Pro software
- Texas Instruments PLLatinum Simulator Tool (optional)

1.3 Resources

Related evaluation and development resources are as follows:

- LMX2572LP data sheet
- TICS Pro software
- PLLatinum Simulator Tool (PLL Sim)

2 Setup

2.1 Connection Diagram
2.2 **Power Supply**

Apply 3.3 V to the $V_{cc}$ SMA connector. The acceptable supply voltage range is 3 V to 3.6 V. The maximum current consumption in the most extreme configuration must not exceed 150 mA.

By default, the onboard DC/DC converter is not used.

2.3 **Reference Clock**

Use the SMA Male-to-male adopter to connect the OSCinP SMA connector with one of the outputs from the Reference PRO. The OSCinM SMA connector is not connected to LMX2572LP, so this connector can be left open.

The EVM is configured for single-ended input with the OSCin pin connected to the OSCinP SMA connector and the OSCinM pin 50-Ω terminated onboard. If required, the EVM can be modified to operate with a different clock source in a different configuration. See Appendix A for more details.

Terminate the unused output of the Reference PRO board with a 50-Ω resistor or SMA load. By default, the output clock from the Reference PRO is a 100-MHz LVPECL clock. Appendix B has the details of the Reference PRO.

2.4 **RF Output**

Connect either the RFoutAP or RFoutAM SMA connector to a signal analyzer. The unused connector must be terminated with a 50-Ω resistor or SMA load. Output frequency is 1.5 GHz and the amplitude is about +0.5 dBm.

By default, the TICS Pro evaluation software has RFoutB power down. These SMA connectors can be left open.

2.5 **Programming**

Connect the ribbon cable from the Reference PRO to the LMX2572LPEVM.

Connect the USB cable from a PC to USB port in the Reference PRO. This provides power supply to the Reference PRO board and communication with the TICS Pro. A firmware update may be required. See Appendix B for more details.
2.6 **Evaluation Software**

Download and install TICS Pro to a PC.

Run the software and follow these steps to start the program.

1. Go to "Select Device" → "PLL + VCO" → "LMX2572" → "LMX2572LP".

![Select Device in TICS Pro](image)

2. Go to "Default Configuration" → "Default Mode YYYY-MM-DD".

![Default Mode](image)

2.7 **EVM Strap Options**

2.7.1 **MUXout_SW**

There are two switches in MUXout_SW. Switch 1 is used for register readback, while Switch 2 is used to provide a visual PLL lock status through the LED D1. By default, both switches are in the Make position. To read back register in TICS Pro, set Switch 2 to the Break position.

![MUXout_SW Switch](image)
3 Typical Measurement

3.1 Default Configuration

3.1.1 Loop Filter

The parameters for the loop filter are listed in Table 1.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCO frequency</td>
<td>Designed for 6 GHz, but works over the whole frequency range</td>
</tr>
<tr>
<td>VCO gain</td>
<td>66 MHz/V</td>
</tr>
<tr>
<td>Effective charge pump gain</td>
<td>2500 µA</td>
</tr>
<tr>
<td>Phase detector frequency</td>
<td>100 MHz</td>
</tr>
<tr>
<td>Loop bandwidth</td>
<td>115 kHz</td>
</tr>
<tr>
<td>Phase margin</td>
<td>48 degrees</td>
</tr>
<tr>
<td>C1_LF, C3_LF</td>
<td>Open</td>
</tr>
<tr>
<td>C2_LF</td>
<td>15 nF</td>
</tr>
<tr>
<td>C4_LF</td>
<td>2.2 nF</td>
</tr>
<tr>
<td>R2_LF</td>
<td>330 Ω</td>
</tr>
<tr>
<td>R3_LF, R4_LF</td>
<td>0 Ω</td>
</tr>
</tbody>
</table>

3.1.2 Typical Output

1. Follow Section 2 to set up the evaluation.
2. Click "Write All Registers" to write all the registers to LMX2572LP.

The default output is 1.5 GHz.
3.2 Additional Tests

3.2.1 Phase Adjustment

Use Equation 1 to adjust the phase of the RF output signal.

\[
\text{Phase shift in degree} = 360° \times \left(\frac{\text{MASH\_SEED}}{\text{PLL\_DEN}}\right) \times \left(\frac{P}{\text{CHDIV}}\right)
\]

where

- \( P = 2 \) when \( \text{VCO\_PHASE\_SYNC\_EN} = 1 \), otherwise \( P = 1 \) \hspace{1cm} (1)

Table 2 and Equation 2 show an example.

Table 2. Phase Adjustment Setting

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>EXAMPLE VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>MASH_SEED</td>
<td>800</td>
</tr>
<tr>
<td>PLL_DEN</td>
<td>1000</td>
</tr>
<tr>
<td>CHDIV</td>
<td>32</td>
</tr>
<tr>
<td>VCO_PHASE_SYNC_EN</td>
<td>0</td>
</tr>
</tbody>
</table>

Phase shift = \( 360° \times \left(\frac{800}{1000}\right) \times \left(\frac{1}{32}\right) = 9° \) \hspace{1cm} (2)

The user can write 800 to MASH\_SEED 40 times to get the 360° phase shift.

![Figure 7. Phase Adjustment Setting](image-url)
3.2.2 Calibration-Free Automatic Ramping

The LMX2572LP supports linear frequency ramp without the need of VCO calibration in the middle of the ramp. The output waveform is a continuous frequency sweep between the start and the end frequencies. However, the frequency ramp range is limited. When using ramp, these parameters must be set accordingly:

- \(\text{OUT\_FORCE} = 1\)
- \(\text{LD\_DLY} = 0\)
- \(\text{PLL\_DEN} = 2^{32} - 1\)

![Figure 8. Phase Adjustment](image)

### Table 3. Calibration-free Automatic Ramp Example

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>EXAMPLE VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ramping start frequency</td>
<td>4795 MHz</td>
</tr>
<tr>
<td>Ramping stop frequency</td>
<td>4805 MHz</td>
</tr>
<tr>
<td>Phase detector frequency</td>
<td>50 MHz</td>
</tr>
<tr>
<td>Ramp up / down time</td>
<td>200 (\mu)s</td>
</tr>
<tr>
<td>RAMP_LIMIT_HIGH</td>
<td>4995 MHz</td>
</tr>
<tr>
<td>RAMP_LIMIT_LOW</td>
<td>4595 MHz</td>
</tr>
</tbody>
</table>

This is a triangular ramp example. Ramp up is defined by RAMP0 while ramp down is defined by RAMP1. RAMP\_THRESH, RAMP\_DLY\_CNT, and RAMP\_SCALE\_COUNT are set to "don't care" because there is no plan to trigger VCO calibration. RAMP\_MANUAL = 0 means Automatic Ramping mode.

Set RAMP\_EN = 1 to start ramping. Set RAMP\_EN = 0 to turn off ramping.
3.2.3 Automatic Ramping

This ramping mode supports wider ramp frequency, but there are glitches in the middle of the ramp because of the VCO calibrations that are required to ensure the continuity of the ramp.

Table 4. Automatic Ramp Example

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>EXAMPLE VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ramping start frequency</td>
<td>4740 MHz</td>
</tr>
<tr>
<td>Ramping stop frequency</td>
<td>4860 MHz</td>
</tr>
<tr>
<td>Phase detector frequency</td>
<td>50 MHz</td>
</tr>
<tr>
<td>Ramp up / down time</td>
<td>1000 µs</td>
</tr>
<tr>
<td>RAMP_LIMIT_HIGH</td>
<td>5060 MHz</td>
</tr>
<tr>
<td>RAMP_LIMIT_LOW</td>
<td>4540 MHz</td>
</tr>
<tr>
<td>fOSCin</td>
<td>100 MHz</td>
</tr>
<tr>
<td>CAL_CLK_DIV</td>
<td>0</td>
</tr>
<tr>
<td>RAMP_THRESH</td>
<td>40 MHz</td>
</tr>
<tr>
<td>Pause time for VCO calibration</td>
<td>500 µs</td>
</tr>
</tbody>
</table>
3.2.4 FSK Modulation

The LMX2572LP supports direct digital FSK modulation. The FSK SPI mode supports discrete 2-, 4-, or 8-level FSK modulation while the FSK SPI FAST and FSK I2S modes support arbitrary level FSK modulation. Table 5 shows a FSK SPI FAST mode example.

Table 5. FSK SPI FAST Mode Example

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>EXAMPLE VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Phase detector frequency</td>
<td>100 MHz</td>
</tr>
<tr>
<td>CHDIV</td>
<td>8</td>
</tr>
<tr>
<td>PLL_DEN</td>
<td>8000000</td>
</tr>
<tr>
<td>FSK_DEV_SCALE</td>
<td>1</td>
</tr>
<tr>
<td>Frequency deviation</td>
<td>±648 Hz; ±1944 Hz</td>
</tr>
</tbody>
</table>
Write the correct values to the FSK_SPI_FAST_DEV register field. The output of LMX2572LP is a discrete 4-level FSK modulation signal.

Figure 13. FSK SPI FAST Mode Setting

Figure 14. FSK SPI FAST Mode
3.2.5 Register Readback

To read back the written register values, follow these steps:

1. Set MUXout_SW Switch 2 to Break position. See Section 2.7.1 for details.
2. Set MUXOUT_LD_SEL to Readback in TICS Pro.

![Figure 15. Readback Setting](image)

3. Click on the Register Name that you want to read back.
4. Click the Read Register button to read back the register value.

![Figure 16. Register Readback](image)
Figure 17. LMX2572LPEVM Schematic (Page 1)
Figure 18. LMX2572LPEVM Schematic (Page 2)
5 PCB Layout and Layer Stack-Up

5.1 PCB Layer Stack-Up

The top layer is 1-oz. copper.

![Layer Stack-Up Diagram](image)

Figure 19. PCB Layer Stack-Up

5.2 PCB Layout

![Top Layer Diagram](image)

Figure 20. Top Layer
Figure 21. GND Layer

Figure 22. Power Layer
Figure 23. Bottom Layer
### Table 6. Bill of Materials

<table>
<thead>
<tr>
<th>DESIGNATOR</th>
<th>QUANTITY</th>
<th>DESCRIPTION</th>
<th>PART NUMBER</th>
<th>MANUFACTURER</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1, C3, C9, C14, C15, C17, C19, C30</td>
<td>8</td>
<td>CAP, CERM, 0.1 µF, 16 V, ±5%, X7R, 0603</td>
<td>0603YC104JAT2A</td>
<td>AVX</td>
</tr>
<tr>
<td>C2, C4, C8, C16</td>
<td>4</td>
<td>CAP, CERM, 10 µF, 10 V, ±10%, X5R, 0805</td>
<td>C0805C106K8PACTU</td>
<td>Kemet</td>
</tr>
<tr>
<td>C2_LF</td>
<td>1</td>
<td>CAP, CERM, 0.015 µF, 50 V, ±5%, X7R, 0603</td>
<td>GRM188R71H153KA01D</td>
<td>MuRata</td>
</tr>
<tr>
<td>C4_LF</td>
<td>1</td>
<td>CAP, CERM, 2200 pF, 50 V, ±5%, C0G/NP0, 0603</td>
<td>GRM188S1H222JA01D</td>
<td>MuRata</td>
</tr>
<tr>
<td>C5, C7, C10, C12</td>
<td>4</td>
<td>CAP, CERM, 0.01 µF, 16 V, ±10%, X7R, 0602</td>
<td>520L103KT16T</td>
<td>AT Ceramics</td>
</tr>
<tr>
<td>C18, C23, C26, C27, C28, C29</td>
<td>6</td>
<td>CAP, CERM, 1 µF, 16 V, ±10%, X7R, 0603</td>
<td>C1608X7R1C105K080AC</td>
<td>TDK</td>
</tr>
<tr>
<td>C20, C21, C22</td>
<td>3</td>
<td>CAP, CERM, 10 µF, 10 V, ±20%, X5R, 0603</td>
<td>C1608X5R1A106M080AC</td>
<td>TDK</td>
</tr>
<tr>
<td>C24</td>
<td>1</td>
<td>CAP, CERM, 0.01 µF, 50 V, ±5%, X7R, 0603</td>
<td>C0603C103J5RACTU</td>
<td>MuRata</td>
</tr>
<tr>
<td>C25</td>
<td>1</td>
<td>CAP, CERM, 0.47 µF, 25 V, ±10%, X7R, 0603</td>
<td>GRM188R71E474KA12D</td>
<td>MuRata</td>
</tr>
<tr>
<td>CE_TP, CSB_TP, GND_TP, MUXout_TP, RampCLK_TP, RampDiR_TP, SCK_TP, SDI_TP, SYNC_TP, SysRefReq_TP, Vcc_TP, VccRF_TP, Vtune_TP</td>
<td>13</td>
<td>Test Point, Compact, White, TH</td>
<td>5007</td>
<td>Keystone</td>
</tr>
<tr>
<td>Cin_0</td>
<td>1</td>
<td>CAP, CERM, 10 µF, 25 V, ±10%, X5R, 0805</td>
<td>GRM219R61E106KA12D</td>
<td>MuRata</td>
</tr>
<tr>
<td>Cout0</td>
<td>1</td>
<td>CAP, CERM, 22 µF, 16 V, ±10%, X5R, 0805</td>
<td>C2012X9R1C226K125AC</td>
<td>TDK</td>
</tr>
<tr>
<td>Css</td>
<td>1</td>
<td>CAP, CERM, 3300 pF, 50 V, ±5%, C0G/NP0, 0603</td>
<td>GRM188S1H323JA01D</td>
<td>MuRata</td>
</tr>
<tr>
<td>D1</td>
<td>1</td>
<td>LED, Green, SMD</td>
<td>LTST-C190GTK</td>
<td>Lite-On</td>
</tr>
<tr>
<td>L1_TPS</td>
<td>1</td>
<td>Inductor, Shielded, Composite, 2.2 μH, 3.7 A, 0.02 Ω, SMD</td>
<td>XFL4020-222MEB</td>
<td>Coilcraft</td>
</tr>
<tr>
<td>MUXout_SW</td>
<td>1</td>
<td>Switch, SPST, Slide, Off-On, 2 Pos, 0.1 A, 20 V, SMD</td>
<td>2119-2MST</td>
<td>CTS Electrocomponents</td>
</tr>
<tr>
<td>OSCinM, OSCinP, SYNC, SysRef, Vcc</td>
<td>5</td>
<td>Connector, SMT, End launch SMA 50 Ω</td>
<td>142-0701-851</td>
<td>Emerson Network Power Connectivity</td>
</tr>
<tr>
<td>R1</td>
<td>1</td>
<td>RES, 330 Ω, 5%, 0.1 W, 0603</td>
<td>RC0603JR-07330RL</td>
<td>Yageo America</td>
</tr>
<tr>
<td>R2</td>
<td>1</td>
<td>RES, 100 kΩ, 5%, 0.1 W, 0603</td>
<td>CRCW0603100KJNEA</td>
<td>Vishay-Dale</td>
</tr>
<tr>
<td>R2_LF</td>
<td>1</td>
<td>RES, 330 Ω, 5%, 0.1 W, 0603</td>
<td>CRCW06033330RJNEA</td>
<td>Vishay-Dale</td>
</tr>
<tr>
<td>R3_LF, R4_LF, R12, R15, R24, R26, R31</td>
<td>7</td>
<td>RES, 0 Ω, 0.1 W, 0603</td>
<td>CRCW06030000Z0EA</td>
<td>Vishay-Dale</td>
</tr>
<tr>
<td>R5, R7, R8, R9, R16, R19, R20, R22</td>
<td>8</td>
<td>RES, 12 kΩ, 5%, 0.1 W, 0603</td>
<td>CRCW060312K0JNEA</td>
<td>Vishay-Dale</td>
</tr>
<tr>
<td>R25, R30</td>
<td>2</td>
<td>RES, 51 Ω, 0.1 W, 0603</td>
<td>CRCW060351RJNEA</td>
<td>Vishay-Dale</td>
</tr>
<tr>
<td>R34, R35, R36, R41, R42, R43, R44, R45</td>
<td>8</td>
<td>RES, 0 Ω, 0.1 W, 0603</td>
<td>CRCW06030000Z0EA</td>
<td>Vishay-Dale</td>
</tr>
<tr>
<td>Rfb1</td>
<td>1</td>
<td>RES, 180 kΩ, 0.1%, 0.1 W, 0603</td>
<td>RT0603BRD07180KL</td>
<td>Yageo America</td>
</tr>
<tr>
<td>Rfb2</td>
<td>1</td>
<td>RES, 562 kΩ, 1%, 0.1 W, 0603</td>
<td>CRCW0603562KFKEA</td>
<td>Vishay-Dale</td>
</tr>
<tr>
<td>RFoutAM, RFoutAP, RFoutBM, RFoutBP</td>
<td>4</td>
<td>JACK, SMA, 50 Ω, Gold, Edge Mount</td>
<td>142-0771-831</td>
<td>Johnson</td>
</tr>
<tr>
<td>U1</td>
<td>1</td>
<td>High Performance, Wideband PLLatinum RF Synthesizer</td>
<td>LMX2572LPRHAR</td>
<td>Texas Instruments</td>
</tr>
<tr>
<td>uWire</td>
<td>1</td>
<td>Header (shrouded), 100 mil, 5x2, Gold plated, SMD</td>
<td>52601-S10-8LF</td>
<td>FCI</td>
</tr>
</tbody>
</table>
7 Troubleshooting Guide

If the EVM does not work as expected, use Figure 24 to identify potential root causes. Consider the following:

- Do not make modifications to the EVM or change the default settings until AFTER it is verified to be working.
- Register readback requires the correct hardware and software setup. See Section 3.2.5 for details.
- The POR current of the LMX2572LPEVM is approximately 30 mA.
- The power-down current of the LMX2572LPEVM is approximately 2.5 mA.

Figure 24. Troubleshooting Guide
These are the different options to provide a reference clock to LMX2572LPEVM. By default, the EVM is configured for an external single-ended clock.

### Table 7. Reference Clock Input Configuration

<table>
<thead>
<tr>
<th>INPUT</th>
<th>EXTERNAL CLOCK</th>
<th>CRYSTAL OSCILLATOR</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single-ended</td>
<td><img src="image1" alt="Single-ended Diagram" /></td>
<td><img src="image2" alt="Single-ended Diagram" /></td>
</tr>
<tr>
<td>Differential (LVDS)</td>
<td><img src="image3" alt="Differential Diagram" /></td>
<td><img src="image4" alt="Differential Diagram" /></td>
</tr>
</tbody>
</table>
The Reference PRO board is used to program the LMX2572LPEVM and provide a clean reference clock to LMX2572LPEVM at the same time. The board has several control pins dedicated for control of output format, output frequency, and output enable control. These control pins are configurable through the jumpers by strapping the center pin to Vdd position or GND position. Connections from the Vdd position to the device supply or from the GND position to the ground plane are connected by 1.5-kΩ resistors. By default, the board is configured for 100-MHz LVPECL output. Connect the Reference PRO to the PC through the USB interface to provide the Reference PRO a steady power supply.

### B.1 Output Frequency Selection

Jumpers FS1 and FS0 are used to set the output frequency.

<table>
<thead>
<tr>
<th>FS1</th>
<th>FS0</th>
<th>OUTPUT FREQUENCY (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>GND</td>
<td>GND</td>
<td>100</td>
</tr>
<tr>
<td>GND</td>
<td>NC</td>
<td>312.5</td>
</tr>
<tr>
<td>GND</td>
<td>Vdd</td>
<td>125</td>
</tr>
<tr>
<td>NC</td>
<td>GND</td>
<td>106.25</td>
</tr>
<tr>
<td>NC</td>
<td>NC</td>
<td>156.25</td>
</tr>
<tr>
<td>NC</td>
<td>Vdd</td>
<td>212.5</td>
</tr>
<tr>
<td>Vdd</td>
<td>GND</td>
<td>62.5</td>
</tr>
</tbody>
</table>
B.2 Output Format Selection

The OE pin is used to enable or disable the output.

The OS pin is used to bias internal drivers and change the output format.

<table>
<thead>
<tr>
<th>OE</th>
<th>OS</th>
<th>OUTPUT FORMAT</th>
</tr>
</thead>
<tbody>
<tr>
<td>GND</td>
<td>Don't Care</td>
<td>Disabled</td>
</tr>
<tr>
<td>Vdd</td>
<td>GND</td>
<td>LVPECL</td>
</tr>
<tr>
<td>Vdd</td>
<td>NC</td>
<td>LVDS</td>
</tr>
<tr>
<td>Vdd</td>
<td>Vdd</td>
<td>HCSL</td>
</tr>
</tbody>
</table>

It is imperative to match the output termination passive components as shown in Table 10.

<table>
<thead>
<tr>
<th>OUTPUT FORMAT</th>
<th>COUPLING</th>
<th>COMPONENT</th>
<th>VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>LVPECL</td>
<td>AC (Default configuration)</td>
<td>R15, R28</td>
<td>0 Ω</td>
</tr>
<tr>
<td></td>
<td></td>
<td>R26, R29</td>
<td>150 Ω</td>
</tr>
<tr>
<td></td>
<td></td>
<td>C24, C25</td>
<td>0.01 µF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>R27, R30, R31</td>
<td>DNP</td>
</tr>
<tr>
<td></td>
<td>DC(1)</td>
<td>R15, R28, C24, C25</td>
<td>0 Ω</td>
</tr>
<tr>
<td></td>
<td></td>
<td>R26, R27, R29, R30, R31</td>
<td>DNP</td>
</tr>
<tr>
<td>LVDS(2)</td>
<td>AC</td>
<td>R25, R27, R28, R30</td>
<td>0 Ω</td>
</tr>
<tr>
<td></td>
<td></td>
<td>R31</td>
<td>100 Ω</td>
</tr>
<tr>
<td></td>
<td></td>
<td>C24, C25</td>
<td>0.01 µF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>R26, R29</td>
<td>DNP</td>
</tr>
<tr>
<td></td>
<td>DC</td>
<td>R25, R27, R28, R30, C24, C25</td>
<td>0 Ω</td>
</tr>
<tr>
<td></td>
<td></td>
<td>R31</td>
<td>100 Ω</td>
</tr>
<tr>
<td></td>
<td></td>
<td>R26, R29</td>
<td>DNP</td>
</tr>
<tr>
<td>HCSL</td>
<td>AC</td>
<td>R25, R28</td>
<td>0 Ω</td>
</tr>
<tr>
<td></td>
<td></td>
<td>R26, R29</td>
<td>50 Ω</td>
</tr>
<tr>
<td></td>
<td></td>
<td>C24, C25</td>
<td>0.01 µF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>R27, R30, R31</td>
<td>DNP</td>
</tr>
<tr>
<td></td>
<td>DC</td>
<td>R25, R28, C24, C25</td>
<td>0 Ω</td>
</tr>
<tr>
<td></td>
<td></td>
<td>R26, R29</td>
<td>50 Ω</td>
</tr>
<tr>
<td></td>
<td></td>
<td>R27, R30, R31</td>
<td>DNP</td>
</tr>
</tbody>
</table>

(1) 50-Ω to VCC – 2-V termination is required on receiver.
(2) 100-Ω differential termination (R31) is provided onboard. Removing this termination is possible if the differential termination is available on the receiver.

Figure 25. Output Termination Schematic
B.3 Typical Output Characteristics

Figure 26. Default Output Phase Noise

Figure 27. Default Output Waveform

B.4 Firmware Update

Usually when the Reference PRO board is used at the first time, TICS Pro will request a firmware update. Follow the pop-up instructions to complete the update. This update is necessary to ensure that the USB connection between the PC and the Reference PRO board is properly set up, otherwise the programming to LMX2572LPEVM will not be successful.

1. When you see this message, click the “OK” button.

Figure 28. Firmware Requirement
2. Next, follow the on-screen procedure.

![Figure 29. Firmware Loader](image)

3. The BSL button is located next to the USB connector.

![Figure 30. BSL Button](image)
4. Follow the on-screen procedure until the "Update Firmware" button pops up.

5. Click the "Upgrade Firmware" button to start the upgrade and click the "Close" button after the upgrade is complete.
6. Check the USB connection in TICS Pro by clicking “USB communications” → “Interface”. Make sure that the "USB Connected" button is green.

![Figure 33. USB Communications](image)
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3 **Regulatory Notices:**

3.1 United States

3.1.1 Notice applicable to EVMs not FCC-Approved:

**FCC NOTICE:** This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:

**CAUTION**

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

**FCC Interference Statement for Class A EVM devices**

*NOTE:* This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.
FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

3.2 Canada

3.2.1 For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

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1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan.

2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or

3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.
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