1 Introduction

The LM5050-1 evaluation board is designed to demonstrate the capabilities of the LM5050-1 OR-ing Diode Controller. One high side N-channel power MOSFET is used. The LM5050-1 evaluation board schematic is shown in Figure 5. The evaluation board is designed to highlight applications with a small solution size. For more information about LM5050-1 functional and electrical characteristics, refer to the LM5050-1 High Side OR-ing FET Controller (SNVS629) data sheet.

2 Operating Range

- Minimum Input Voltage, 6V
- Maximum Input Voltage, 50V
- Output Current Range: 0A to 15A
- Ambient Temperature Range 0°C to 50°C
- Board Size 1.50 inches x 2.25 inches

The load current capability is limited at 15A by the ratings of the terminals and the PCB copper area and weight. The PCB layout has not been tested for currents above 15A, so this should only be done with some degree of caution.

The maximum input voltage is limited by the breakdown voltage rating of both D1 and D2.

Typical evaluation board performance and characteristics curves are shown in Figure 1 through Figure 2. The PCB layout is shown in Figure 7 and Figure 8. Test points are provided for optional control and signal monitoring.

3 Evaluation Board Start-Up

Before applying power to the LM5050-1 evaluation board, all external connections should be verified. The external power supply must be turned off and connected with proper polarity to the VS, VIN, VOUT, and GND terminals. Under basic evaluation conditions the Off test point is left open.

The evaluation board will be in the normal operating mode when power is applied. The Off terminal is used only when there is a desire to disable normal operation.
4 **Inductive Kick-Back Protection**

Diode D1 and capacitor C1 (as do diode D2 and capacitor C2) serve as inductive kick-back protection to limit negative transient voltage spikes generated on the input when the input supply voltage is abruptly taken to zero volts.

5 **Off Test Point**

The Off test point provided on the LM5050-1 evaluation board is used to control the LM5050-1 operation. The Off test point is connected directly to the LM5050-1 OFF pin. See the LM5050-1High Side OR-ing FET Controller (SNVS629) data sheet for more details.

To enable the LM5050-1 apply a voltage less than 0.8V to the Off test point, connect the Off test point to GND, or leave the Off test point open (default). If the Off test point is left open, the LM5050-1 OFF pin internal pull-down will ensure that the LM5050-1 becomes operational.

To disable the LM5050-1 apply a voltage greater than 2.0V to the Off test point.

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**Figure 1. Forward Waveforms**

**Figure 2. Reverse Waveforms**

**Figure 3. OFF pin vs GATE**

**Figure 4. Connection Diagram**
**Figure 5. Schematic Diagram**

**Figure 6. Component Placement**
Figure 7. Evaluation Board, Top Side (Component)

Figure 8. Evaluation Board, Bottom Side
# 6 Bill of Materials

<table>
<thead>
<tr>
<th>ID</th>
<th>Description</th>
<th>Manufacturer</th>
<th>Mfgr Part Number</th>
</tr>
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<tr>
<td>U1</td>
<td>IC; Ideal OR-ing Diode Controller</td>
<td>Texas Instruments</td>
<td>LM5050</td>
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<tr>
<td>C1</td>
<td>Capacitor: MLCC; 1.0µF; ±10%; 100V; 1825</td>
<td>Vishay/Vitramon</td>
<td>VJ1825Y105KBBAT4X</td>
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<tr>
<td>C2</td>
<td>Capacitor: 22 µF; ±20%; 100V; Aluminum Electrolytic; SMT</td>
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<td>C3</td>
<td>Capacitor: 0.1 µF; MLCC; ±10%; 100V; X7R; 1210</td>
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<td>D1</td>
<td>Diode: Schottky Barrier Rectifier; 1A; 60V; SMA</td>
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<td>D2</td>
<td>Diode: TVS; Unidirectional; 600W; 60V; SMB</td>
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<td>Q1</td>
<td>MOSFET: N-Channel; 100V; 40A; 0.025Ω; D'PAK</td>
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<td>SUM40N10-30-E3</td>
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<td>R1</td>
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<td>CRCW0603100RFKEA</td>
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<td>R2</td>
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<td>VIN</td>
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<td></td>
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<td>Off</td>
<td>Test Point Terminal: 0.040in Dia Mtg Hole; White</td>
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