Test Data
For PMP7877 RevB
11/29/2012

Texas Instruments
# Test Specifications

<table>
<thead>
<tr>
<th>Vin Nominal</th>
<th>12V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vout 1 (U2 Output) LM2130</td>
<td>1V @ 5A</td>
</tr>
<tr>
<td>Vout 2 (U4 CH1 Output) LM25119 (-A)</td>
<td>1.8V @ 2.5A</td>
</tr>
<tr>
<td>Vout 3 (U4 CH2 Output) LM25119 (-B)</td>
<td>1.5V @ 6A*</td>
</tr>
<tr>
<td>Vout 4 (U7 Output) (LM21305)</td>
<td>3.3V @ 5A</td>
</tr>
<tr>
<td>Vout 5 (U8 Output) (LM21305)</td>
<td>3.3V @ 5A</td>
</tr>
<tr>
<td>Vout 6 (U6 Output) (LMR12020)</td>
<td>5V @ 2A</td>
</tr>
<tr>
<td>Vout 7 (U5 Output) (TPS51200)</td>
<td>0.75V @ 1A continuous; 3A peak</td>
</tr>
</tbody>
</table>

*Note: The U4 CH2 Output of 6A includes the 1A drawn by the U5 LDO.*

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# Typical Performance

**Efficiency**
Efficiency was measured with each output channel being incremented by 10% of their corresponding full load current.

Waveforms
Startup

Startup Sequencing (into no load)
Shutdown Sequencing (Each output loaded to 50% of corresponding channel’s full load value)
U2 (1V @ 5A) Startup into No Load (all other channel outputs not loaded)
U2 (1V @ 5A) Startup into 5A Load (all other channel outputs not loaded)
U4 CH1 (1.8V @ 2.5A) Startup into No Load (all other channel outputs not loaded)
**Test Report PMP7877 RevA**

U4 CH1 (1.8V @ 2.5A) Startup into 2.5A Load (all other channel outputs not loaded)

<table>
<thead>
<tr>
<th>Measured Value</th>
<th>PI: Input(C1)</th>
<th>P2: ...</th>
<th>P2: ...</th>
<th>PI: ...</th>
<th>PS: ...</th>
<th>PS: ...</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Supply</td>
<td>1.8V @ 2.5A</td>
<td>...</td>
<td>...</td>
<td>...</td>
<td>...</td>
<td>...</td>
</tr>
<tr>
<td>Status</td>
<td>Power Good</td>
<td>...</td>
<td>...</td>
<td>...</td>
<td>...</td>
<td>...</td>
</tr>
</tbody>
</table>

**Graph Description**

- **V<sub>in</sub>**: Input voltage
- **V<sub>out</sub>**: Output voltage

**Graph Details**

- **Timebase**: 0.0 ms
- **Trigger**: Edge, Positive
- **Slope**: 4.0 mV
- **Sampling**: 1.0 MS/s

11/29/12
U4 CH2 (1.5V @ 6A) Startup into No Load (all other channel outputs not loaded)
U4 CH2 (1.5V @ 6A) Startup into 6A Load (all other channel outputs not loaded)
U7 (3.3V @ 5A) Startup into No Load (all other channel outputs not loaded)
U7 (3.3V @ 5A) Startup into 5A Load (all other channel outputs not loaded)
U8 (3.3V @ 5A) Startup into No Load (all other channel outputs not loaded)
U8 (3.3V @ 5A) Startup into 5A Load (all other channel outputs not loaded)
U6 (5V @ 2A) Startup into No Load (all other channel outputs not loaded)
U6 (5V @ 2A) Startup into 2A Load (all other channel outputs not loaded)
U5 (0.75V @ 1A continuous; 3A peak) Startup into No Load (all other channel outputs not loaded)
U5 (0.75V @ 1A continuous; 3A peak) Startup into 1A Load (all other channel outputs not loaded)
Output Voltage Ripple

U2 (1V @ 5A) Output Voltage Ripple at 5A Load (Vripple ≈ 10mV)
U4 CH1 (1.8V @ 2.5A) Output Voltage Ripple at 2.5A Load (while U4 CH2 output not loaded)

(Vripple ≈ 10mV)
U4 CH1 (1.8V @ 2.5A) Output Voltage Ripple at 2.5A Load (while U4 CH2 output loaded at 6A)

(Vripple ≈ 10mV)
U4 CH2 (1.5V @ 6A) Output Voltage Ripple at 6A Load (while U4 CH1 output not loaded)

(Vripple ≈ 28mV)
U4 CH2 (1.5V @ 6A) Output Voltage Ripple at 6A Load (while U4 CH1 output loaded at 2.5A)

(Vripple ≈ 28mV)
**Test Report PMP7877 RevA**

**U7 (3.3V @ 5A) Output Voltage Ripple at 5A Load (V_{ripple} ≈ 8mV)**
U8 (3.3V @ 5A) Output Voltage Ripple at 5A Load (Vripple = 8mV)
U6 (5V @ 2A) Output Voltage Ripple at 2A Load (Vripple \approx 20mV)
U5 (0.75V @ 1A continuous; 3A peak) Output Voltage Ripple at 1A Load (while U6 output not loaded) (Vripple ≈ 15mV)
Load Transient Response

U2 (1V @ 5A) Output Load Transient Response (50%-to-100% Load Step)
U7 (3.3V @ 5A) Output Load Transient Response (50%-to-100% Load Step)
U8 (3.3V @ 5A) Output Load Transient Response (50%-to-100% Load Step)
U4 CH1 (1.8V @ 2.5A) Output Load Transient Response (50%-to-100% Load Step)
U4 CH2 (1.5V @ 6A) Output Load Transient Response (50%-to-100% Load Step)
U6 (5V @ 2A) Output Load Transient Response (50%-to-100% Load Step)
U5 (0.75V @ 1A continuous; 3A peak) Output Load Transient Response (50%-to-100% Load Step)
Short Circuit Testing

U2 (1V @ 5A) Output Short Circuit
U2 (1V @ 5A) Output Short Circuit Recovery
U4 CH1 (1.8V @ 2.5A) Output Short Circuit
U4 CH1 (1.8V @ 2.5A) Output Short Circuit Recovery
U4 CH2 (1.5V @ 6A) Output Short Circuit
U4 CH2 (1.5V @ 6A) Output Short Circuit Recovery
U7 (3.3V @ 5A) Output Short Circuit
U7 (3.3V @ 5A) Output Short Circuit Recovery
U8 (3.3V @ 5A) Output Short Circuit
U8 (3.3V @ 5A) Output Short Circuit Recovery
U6 (5V @ 2A) Output Short Circuit
U6 (5V @ 2A) Output Short Circuit Recovery
U5 (0.75V @ 1A continuous; 3A peak) Output Short Circuit
U5 (0.75V @ 1A continuous; 3A peak) Output Short Circuit Recovery
Top Side Thermal Image at Steady State (All outputs running at 100% load)
Bottom Side Thermal Image at Steady State (All outputs running at 100% load; soaked for 15 minutes)
FABRICATION

Board dimensions: 1.5” x 5”

Top Side
Bottom Side
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