PMP8610 Test Results

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1. Block Diagram

---

[Diagram showing a block diagram with labeled components and connections]

- **24V_{nom}**
  - LMZ23608H
  - TPS84320
  - TPS84A20
  - TPS84B20
  - TPS84A20
  - TPS51200

- **12V**
  - 3.3V @ 2A
  - 1.5V @ 1.2A
  - 2.5V @ 6A
  - 1.2V @ 7A
  - 1.1V @ 13A
  - 1.5V @ 9.3A

---

Legend:

- MM = Sequencing Order

---

[Caption: Altera Arria V]
2. Startup/Sequencing

The startup waveform is shown in Figure 1 and Figure 1.1. The input voltage is 12V, with no load at the output.

*Figure 1*

Ch1 => Output voltage 1.2V order #1  
Ch2 => Output voltage 1.1V order #1  
Ch3 => Output voltage 2.5V order #2  
Ch4 => Output voltage 3.3V order #2

2ms/div  
Full Bandwidth
Figure 2.1

Ch1 => Output voltage 1.5V order #3
Ch3 => Output voltage 2.5V order #2
Ch4 => Output voltage 3.3V order #2

2ms/div
Full Bandwidth
A selection of startup waveforms is shown in Figure 1.2 to demonstrate LDO startup. The input voltage is 12V, with no load at the output.

**Figure 1.2**

*Ch1 => Output voltage 2.5V order #2*
*Ch2 => LDO Output voltage 1.5V order #2 + LDO delay*
*Ch2 => Output Voltage 1.5V order #3*

2.5ms/div
Full Bandwidth
3. Synchronization

The switching nodes of the buck stages are shown in Figure 2 and Figure 2.1. The input voltage is 12V, with no load at the output.

![Figure 3]

Ch1 => Switching node for 1.1 Vout
Ch2 => Switching node for 1.2 Vout
Ch3 => Switching node for 2.5 Vout
Ch4 => Switching node for 3.3 Vout

Common frequency: 500 kHz

1µs/div
Full Bandwidth
Figure 4.1

\textit{Ch1 => Switching node for 1.1 Vout}
\textit{Ch2 => Switching node for 1.2 Vout}
\textit{Ch3 => Switching node for 1.5 Vout}

\textit{Common frequency: 500 kHz}

\textit{1\mu s/div}

\textit{Full Bandwidth}
4. DDR Tracking

DDR tracking is shown in the Figures 3 and 4.

![Figure 5](image)

Ch1 => DDR3 1.5V output voltage from buck stage  
Ch2 => DDR3 0.75V termination voltage from TPS51200  
500µs/div  
Full Bandwidth

![Figure 6](image)

Ch1 => DDR3 1.5V output voltage from buck stage  
Ch2 => DDR3 0.75V termination voltage from TPS51200  
20ms/div  
Full Bandwidth
5. Efficiency

The respective efficiencies of the buck stages providing 3.3V, 2.5V, 1.2V, 1.1V, and 1.5V are shown in Figures 7, 8, 9, 10, and 11 below. The input voltage is 12V.

![Graph: Efficiency vs. Output Current](image)

**Figure 7: TPS84320 3.3V Output**

<table>
<thead>
<tr>
<th>VIN (V)</th>
<th>IIN (A)</th>
<th>VOUT (V)</th>
<th>IOUT (A)</th>
<th>PIN (W)</th>
<th>POUT (W)</th>
<th>Eff (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>12.00</td>
<td>0.20</td>
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<td>0.5</td>
<td>2.400</td>
<td>1.655</td>
<td>68.96</td>
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<tr>
<td>12.00</td>
<td>0.35</td>
<td>3.3</td>
<td>1.0</td>
<td>4.200</td>
<td>3.300</td>
<td>78.57</td>
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<td>12.00</td>
<td>0.50</td>
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<td>1.5</td>
<td>6.000</td>
<td>4.920</td>
<td>82.00</td>
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<tr>
<td>12.00</td>
<td>0.65</td>
<td>3.27</td>
<td>2.0</td>
<td>7.800</td>
<td>6.540</td>
<td>83.85</td>
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</tbody>
</table>
Figure 8: TPS84A20 2.5V Output

<table>
<thead>
<tr>
<th>VIN (V)</th>
<th>IIN (A)</th>
<th>VOUT (V)</th>
<th>IOUT (A)</th>
<th>PIN (W)</th>
<th>POUT (W)</th>
<th>Eff (%)</th>
</tr>
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<tbody>
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<td>12.00</td>
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<td>1.0</td>
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<td>12.00</td>
<td>0.58</td>
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<td>6.960</td>
<td>6.100</td>
<td>87.64</td>
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<td>12.00</td>
<td>0.70</td>
<td>2.42</td>
<td>3.0</td>
<td>8.340</td>
<td>7.260</td>
<td>87.05</td>
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<tr>
<td>12.00</td>
<td>0.81</td>
<td>2.39</td>
<td>3.5</td>
<td>9.720</td>
<td>8.365</td>
<td>86.06</td>
</tr>
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<td>12.00</td>
<td>0.93</td>
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<td>4.0</td>
<td>11.160</td>
<td>9.480</td>
<td>84.95</td>
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<td>12.00</td>
<td>1.04</td>
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<td>4.5</td>
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<td>84.74</td>
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<td>1.16</td>
<td>2.34</td>
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<td>1.27</td>
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<td>1.39</td>
<td>2.30</td>
<td>6.0</td>
<td>16.680</td>
<td>13.800</td>
<td>82.73</td>
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</table>
Figure 9: TPS84A20 1.2V Output

<table>
<thead>
<tr>
<th>VIN (V)</th>
<th>IIN (A)</th>
<th>VOUT (V)</th>
<th>IOUT (A)</th>
<th>PIN (W)</th>
<th>POUT (W)</th>
<th>Eff (%)</th>
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<tbody>
<tr>
<td>11.99</td>
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<tr>
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<td>1.5</td>
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<td>1.20</td>
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<td>3.5</td>
<td>4.908</td>
<td>4.207</td>
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<td>0.47</td>
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<td>5.626</td>
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Figure 10: TPS84B20 1.1V Output

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<th>VIN (V)</th>
<th>IIN (A)</th>
<th>VOUT (V)</th>
<th>IOUT (A)</th>
<th>PIN (W)</th>
<th>POUT (W)</th>
<th>Eff (%)</th>
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<td>7.680</td>
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</table>
### Figure 11: TPS84A20 1.5V Output

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<th>VIN (V)</th>
<th>IIN (A)</th>
<th>VOUT (V)</th>
<th>IOUT (A)</th>
<th>PIN (W)</th>
<th>POUT (W)</th>
<th>Eff (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>11.99</td>
<td>0.16</td>
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<td>1.0</td>
<td>1.918</td>
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<td>79.70</td>
</tr>
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<td>0.30</td>
<td>1.53</td>
<td>2.0</td>
<td>3.594</td>
<td>3.058</td>
<td>85.09</td>
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<td>0.44</td>
<td>1.53</td>
<td>3.0</td>
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<td>4.0</td>
<td>6.997</td>
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<td>7.640</td>
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<td>10.0</td>
<td>18.357</td>
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</table>
6. Load Step

The load regulation of the TPS84320 3.3V output is shown in Figures 12 and 13 below. The input voltage is 12V. The load step increases from 1A to 2A.

**Figure 12**

Ch1 => AC coupled output voltage
Ch4 => Output current
1V = 10A
Slope of step: 1A/16.5µs

**Figure 13**

Ch1 => AC coupled output voltage
Ch4 => Output current
1V = 10A
Slope of step: 1A/20µs
The load regulation of the TPS84A20 2.5V output is shown in Figures 14 and 15 below. The input voltage is 12V. The load step increases from 3A to 6A.

![Figure 14](image1)

**Figure 14**

Ch1 => AC coupled output voltage

Ch4 => Output current
1V = 10A

Slope of step: 3A/22μs

![Figure 15](image2)

**Figure 15**

Ch1 => AC coupled output voltage

Ch4 => Output current
1V = 10A

Slope of step: 3A/18μs
The load regulation of the TPS84A20 1.2V output is shown in the Figures 16 and 17 below. The input voltage is 12V. The load step increases from 3.5A to 7A.

**Figure 16**

Ch1 => AC coupled output voltage
Ch4 => Output current
1V = 10A
Slope of step: 3.5A/19µs

**Figure 17**

Ch1 => AC coupled output voltage
Ch4 => Output current
1V = 10A
Slope of step: 3.5A/11µs
The load regulation of the TPS84B20 1.1V output is shown in the Figures 18 and 19 below. The input voltage is 12V. The load step increases from 6.5A to 13A.

Figure 18

Ch1 => AC coupled output voltage
Ch4 => Output current
1V = 10A
Slope of step: 6.5A/33.5µs

Figure 19

Ch1 => AC coupled output voltage
Ch4 => Output current
1V = 10A
Slope of step: 6.5A/34µs
The load regulation of the TPS84A20 1.5V output is shown in the Figures 20 and 21 below. The input voltage is 12V. The load step increases from 4.5A to 9A.

**Figure 20**

Ch1 => AC coupled output voltage
Ch4 => Output current
1V = 10A
Slope of step: 4.5A/12μs

**Figure 21**

Ch1 => AC coupled output voltage
Ch4 => Output current
1V = 10A
Slope of step: 4.5A/13μs
The load regulation of the 1.5V LDO output is shown in the Figures 22 and 23 below. The input voltage is 12V. The load step increases from 0A to 1.2A.

**Figure 22**

Ch1 => AC coupled output voltage
Ch4 => Output current
1V = 10A
Slope of step: 1.2A/205μs

**Figure 23**

Ch1 => AC coupled output voltage
Ch4 => Output current
1V = 10A
Slope of step: 1.2A/85μs
7. Frequency Response

Figure 24 shows the loop response of the TPS84320 3.3V output with 1A load and 12V input.

Table 1 summarizes the results from Figure 24.

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
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<tbody>
<tr>
<td><strong>Bandwidth (kHz)</strong></td>
<td>31.21</td>
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<tr>
<td><strong>Phase Margin</strong></td>
<td>77.99°</td>
</tr>
<tr>
<td><strong>Slope (20dB/Decade)</strong></td>
<td>-0.981</td>
</tr>
</tbody>
</table>

Table 1
Figure 25 shows the loop response of the TPS84A20 2.5V output with 3A load and 12V input.

Table 2 summarizes the results from Figure 25.

<table>
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<tr>
<th>Bandwidth (kHz)</th>
<th>7.861</th>
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<tr>
<td>Phase Margin</td>
<td>62.94°</td>
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<tr>
<td>Slope (20dB/Decade)</td>
<td>-1.34</td>
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</tbody>
</table>

Table 2
Figure 26 shows the loop response of the TPS84A20 1.2V output with 3.5A load and 12V input.

Table 3 summarizes the results from Figure 26.

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<td>Bandwidth (kHz)</td>
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<tr>
<td>Phase Margin</td>
<td>63.55°</td>
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<tr>
<td>Slope (20dB/Decade)</td>
<td>-1.27</td>
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</table>
Figure 27 shows the loop response of the TPS84B20 1.1V output with 2A load and 12V input.

Table 4 summarizes the results from Figure 26.

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<td><strong>Bandwidth (kHz)</strong></td>
<td>12.67</td>
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<tr>
<td><strong>Phase Margin</strong></td>
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</tr>
<tr>
<td><strong>Slope (20dB/Decade)</strong></td>
<td>-1.03</td>
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Table 4
Figure 28 shows the loop response of the TPS84A20 1.5V output with 5A load and 12V input.

Table 5 summarizes the results from Figure 26.

<p>| | |</p>
<table>
<thead>
<tr>
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<tr>
<td><strong>Bandwidth (kHz)</strong></td>
<td>11.25</td>
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<tr>
<td><strong>Phase Margin</strong></td>
<td>69.9°</td>
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<tr>
<td><strong>Slope (20dB/Decade)</strong></td>
<td>-1.08</td>
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Table 5
8. Miscellaneous

In order to synchronize the different buck stages, a square wave clock signal is required with a duty cycle between 20% and 80%. The TPS84B20 is used as the master clock but its duty cycle is only 9.2%. The following schematic and figure show the circuit used in order to provide a clock signal with 50% duty cycle.

![Synchronization circuit diagram]

**Figure 29: Synchronization circuit**

![Waveform chart]

**Ch2 =>** Switching node of the TPS84B20

**Ch3 =>** output of the synchronization circuit

Ch2 => Measured duty cycle of the switching node: 9.3%

Ch3 => Measured duty cycle of the synchronization signal: 48.6%
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