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OMAP4430/4460 Multimedia Devices TRM Addendum - Functional Differences Highlights between OMAP4430 Silicon Revision 2.x and OMAP4460 Silicon Revision 1.x

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OMAP4430/4460 Multimedia Devices TRM Addendum - Functional Differences Highlights between OMAP4430 Silicon Revision 2.x and OMAP4460 Silicon Revision 1.x

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Delta Readers' Guide

The purpose of this document is to highlight functional modifications between OMAP4430 Silicon Revision 2.x and OMAP4460 Silicon Revision 1.x. To easily locate the updates and focus on the modified functionalities, the document is organized as follows:

- For all sections, except the Register Manual section:
  - A high level description of the differences between the two devices is given in the most appropriate location
  - The high level changes appear in red color
  - The full versions of chapters updated are available in the regular TRM
- For the Register Manual section, only modified or added registers are given:
  - Old bit-fields or registers appear in strikethrough
  - New or updated bit-fields or registers appear in red color
  - Unchanged information remains in the regular formatting

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History

The following table summarizes the OMAP4430/4460 Multimedia Device TRM Addendum - Functional Differences Highlights between OMAP4430 Silicon Revision 2.x and OMAP4460 Silicon Revision 1.x multimedia devices.

Table 1. TRM Addendum versions

Version	Literature Number	Date	Notes
1.11	SWPU278	December 2011	OMAP4430/4460 Multimedia Device TRM Addendum - Functional Differences Highlights between OMAP4430 Silicon Revision 2.x and OMAP4460 Silicon Revision 1.x - Initial release (SWPU278).
1.12	SWPU278	February 2012	OMAP4430/4460 Multimedia Device TRM Addendum - Functional Differences Highlights between OMAP4430 Silicon Revision 2.x and OMAP4460 Silicon Revision 1.x (SWPU278). Updates in ISS and Control Module chapters.
1.13	SWPU278	March 2012	OMAP4430/4460 Multimedia Device TRM Addendum - Functional Differences Highlights between OMAP4430 Silicon Revision 2.x and OMAP4460 Silicon Revision 1.x (SWPU278). Updates in PRCM and ISS chapters.
1.14	SWPU278	April 2012	OMAP4430/4460 Multimedia Device TRM Addendum - Functional Differences Highlights between OMAP4430 Silicon Revision 2.x and OMAP4460 Silicon Revision 1.x (SWPU278). Updates in Control Module chapter.
1.15	SWPU278	May 2012	OMAP4430/4460 Multimedia Device TRM Addendum - Functional Differences Highlights between OMAP4430 Silicon Revision 2.x and OMAP4460 Silicon Revision 1.x (SWPU278). Updates in ISS chapter.
1.16	SWPU278	August 2012	OMAP4430/4460 Multimedia Device TRM Addendum - Functional Differences Highlights between OMAP4430 Silicon Revision 2.x and OMAP4460 Silicon Revision 1.x (SWPU278). Updates in Control Module chapter.

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Chapter 1. Introduction

This chapter describes the differences in the features, supporting subsystems, and architecture between the OMAP4430 Silicon Revision 2.x and OMAP4460 Silicon Revision 1.x multimedia devices

Note

Exhaustive lists of functional differences are given in the respective chapters of this document.

1.1. Overview

Refer to OMAP4460 Silicon Revision 1.x TRM

1.2. Environment

The increased speed of Cortex-A9 MPU subsystem implies higher power demands for the MPU power domain. A discrete DC-DC power regulator replaces the TWL6030 VCORE1 power resource.

1.3. Description

Direct paths between the Cortex-A9 MPU subsystem and the EMIF modules are created to decrease the latency of memory accesses.

1.3.1. Cortex-A9 MPU Subsystem Description

Refer to OMAP4460 Silicon Revision 1.x TRM

1.3.2. DSP Subsystem Description

Refer to OMAP4460 Silicon Revision 1.x TRM

1.3.3. IVA-HD Subsystem Description

Refer to OMAP4460 Silicon Revision 1.x TRM

1.3.4. Cortex-M3 MPU Subsystem Description

Refer to OMAP4460 Silicon Revision 1.x TRM

1.3.5. Display Subsystem Description

Support for the 1080p@24Hz 3D Stereoscopic frame-packing format of HDMI v1.4 standard is added.

The analog TV-out port (CVIDEO) and the video encoder are no longer supported.

1.3.6. ABE Subsystem Description

Refer to OMAP4460 Silicon Revision 1.x TRM

1.3.7. ISS Description

Refer to OMAP4460 Silicon Revision 1.x TRM

In addition to the two CSI interfaces supported by OMAP4430, OMAP4460 provides a 16-bit parallel camera interface.

1.3.8. 2D/3D Graphics Accelerator Description

Refer to OMAP4460 Silicon Revision 1.x TRM

1.3.9. Face Detect Module Description

Refer to OMAP4460 Silicon Revision 1.x TRM

1.3.10. On-Chip Debug Support Description

Refer to OMAP4460 Silicon Revision 1.x TRM

1.3.11. Power, Reset, and Clock Management Description

Refer to OMAP4460 Silicon Revision 1.x TRM

1.3.12. On-Chip Memory Description

Refer to OMAP4460 Silicon Revision 1.x TRM

1.3.13. Memory Management Description

Refer to OMAP4460 Silicon Revision 1.x TRM

1.3.14. External Memory Interface Description

Refer to OMAP4460 Silicon Revision 1.x TRM

1.3.15. DSP Subsystem Description

Refer to OMAP4460 Silicon Revision 1.x TRM

1.3.16. System and Connection Peripherals

Refer to OMAP4460 Silicon Revision 1.x TRM

1.4. Package-On-Package Concept

Refer to OMAP4460 Silicon Revision 1.x TRM

1.5. Device Identification

ID_CODE register is changed as follows:

- Hawkeye is replaced by Ramp system in OMAP4460 ES1.x.
  - Hawkeye number value for OMAP4430 ES2.1, ES2.2 and ES2.3 is 0xB95C
  - Ramp system value for OMAP4460 ES1.0 and ES1.1 is 0xB94E

- Revision number value is changed from 0x6 for OMAP4430 ES2.3 to 0x2 for OMAP4460 ES1.1.

- The ID_CODE value is changed from 0x6B95C02F for OMAP4430 ES2.3 to 0x2B94E02F for OMAP4460 ES1.1.

Table 1.1. Device Identification Registers

Register Name	Alias Name	Physical Address	Address Offset	Size
STD_FUSE_DIE_ID_0[31:0]	DIE_ID[31:0]	0x4A00 2200	0x200	32
ID_CODE[31:0]	ID_CODE[31:0]	0x4A00 2204	0x204	32
STD_FUSE_DIE_ID_1[31:0]	DIE_ID[63:32]	0x4A00 2208	0x208	32
STD_FUSE_DIE_ID_2[31:0]	DIE_ID[95:64]	0x4A00 220C	0x20C	32
STD_FUSE_DIE_ID_3[31:0]	DIE_ID[127:96]	0x4A00 2210	0x210	32
STD_FUSE_PROD_ID_0[31:0]	PROD_ID[31:0]	0x4A00 2214	0x214	32
STD_FUSE_PROD_ID_1[31:0]	PROD_ID[63:32]	0x4A00 2218	0x218	32

1.7.

Note

This section contains only modified registers.

Table 1.2. STD_FUSE_PROD_ID_1

Address Offset	0x0000 0218		
Physical Address	SeeTable 1.1	**Instance**	GENERAL
Description	This register shows the device type.		
Type	R		

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
RESERVED	SILICON_TYPE	RESERVED	

Bits	Field Name	Description	Type	Reset
31:18	RESERVED	Reserved	R	0x-
17:16	SILICON_TYPE	Define the silicon performance type 0x0:~~Low performance (0.8 GHz)~~Reserved 0x1: Standard performance (~~1~~1.2GHz) 0x2: High performance (~~1.2~~1.5GHz) 0x3: Reserved	R	0x-
15:0	RESERVED	Reserved	R	0x-

Chapter 2. Memory Mapping

This chapter describes differences in the memory mapping between the OMAP4430 Silicon Revision 2.x and OMAP4460 Silicon Revision 1.x multimedia devices.

2.1. Introduction

Refer to OMAP4460 Silicon Revision 1.x TRM.

2.2. L3 Memory Space Mapping

Table 2.1. Global Memory Space Mapping

Quarter	Module Name	Start Address (hex)	End Address (hex)	Size	Description
Q0 (1GB)	Boot space GPMC[1]	0x0000 0000	0x3FFF FFFF	1GB	
	GPMC	0x0000 0000	0x3FFF FFFF	1GB	8/16 Ex[2]/R/W
Q1 (1GB)	On-chip memory	0x4000 0000	0x7FFF FFFF	1GB	ROM/SRAM address space
	Reserved	0x4000 0000	0x4002 7FFF	160KB	Reserved
	Boot ROM internal	~~0x4002 8000~~ 0x4003 0000	~~0x4003 3FFF~~ 0x4003 BFFF	48KB	32-bit Ex/R Boot ROM
	Reserved	0x4003 4000	0x400F FFFF	816KB	Reserved
	Audio back-end (ABE)	0x4010 0000	0x401F FFFF	1MB	ABE domain (direct Cortex-A9 MPU access).
	Reserved	0x4020 0000	0x402F FFFF	1MB	Reserved
	L3 OCM_RAM	0x4030 0000	0x4030 DFFF	56KB	32-bit Ex/R/W
	Reserved	0x4030 E000	0x43FF FFFF	63MB	Reserved
	L3 configuration registers	0x4400 0000	0x47FF FFFF	64MB	L3 configuration registers
	L4_PER domain	0x4800 0000	0x48FF FFFF	16MB	Peripheral domain.
	L4_ABE domain	0x4900 0000	0x49FF FFFF	16MB	ABE domain (double-mapped for Cortex-A9 MPU)

1. Boot space location depends on the external sys_boot[5:0] pins.
2. Ex = Executable

2.2.1. L3_EMU Memory Space Mapping

Refer to OMAP4460 Silicon Revision 1.x TRM.

2.3. L4 Memory Space Mapping

2.3.1. L4_CFG Memory Space Mapping

2.3.2. L4_WKUP Memory Space Mapping

2.3.3. L4_PER Memory Space Mapping

Refer to OMAP4460 Silicon Revision 1.x TRM.

2.3.4. L4_ABE Memory Space Mapping

Refer to OMAP4460 Silicon Revision 1.x TRM.

2.4. Dual Cortex-M3 Subsystem Memory Space Mapping

2.4.1. L4_CFG Memory Space Mapping

Table 2.2. L4_CFG Memory Space Mapping

Module Name	Start Address (hex)	End Address (hex)	Size	Description
Reserved	0x4A10 C000	0x4A20 3FFF	992KB	Reserved
C2C-Init firewall	0x4A20 4000	0x4A20 4FFF	4KB	Module
	0x4A20 5000	0x4A20 5FFF	4KB	L4 interconnect
C2C-Target firewall	0x4A20 6000	0x4A20 6FFF	4KB	Module
	0x4A20 7000	0x4A20 7FFF	4KB	L4 interconnect
Reserved	0x4A20 8000	~~0x4A20 BFFF~~ 0x4A20 9FFF	~~16KB~~ 8KB	Reserved
MA firewall	0x4A20 A000	0x4A20 AFFF	4KB	Memory Adapter Configuration registers
	0x4A20 B000	0x4A20 BFFF	4KB	L4 interconnect
EMIF firewall	0x4A20 C000	0x4A20 CFFF	4KB	Configuration registers
	0x4A20 D000	0x4A20 DFFF	4KB	L4 interconnect
Reserved	0x4A20 E000	0x4A20 FFFF	8KB	Reserved
GPMC firewall	0x4A21 0000	0x4A21 0FFF	4KB	Configuration registers
	0x4A21 1000	0x4A21 1FFF	4KB	L4 interconnect
OCMC RAM firewall	0x4A21 2000	0x4A21 2FFF	4KB	Module
	0x4A21 3000	0x4A21 3FFF	4KB	L4 interconnect

2.5. DSP Subsystem Memory Space Mapping

Refer to OMAP4460 Silicon Revision 1.x TRM.

2.6. Display Subsystem Memory Space Mapping

The Video DAC (VDAC) functionality is not supported.

2.6.1. L3 Interconnect View of the Display Memory Space

Refer to OMAP4460 Silicon Revision 1.x TRM.

2.6.2. L4 Interconnect View of the Display Memory Space

Refer to OMAP4460 Silicon Revision 1.x TRM.

Chapter 3. Power, Reset, and Clock Management

This chapter describes the differences in the Power, Reset, and Clock Management between OMAP4430 Silicon Revision 2.x and OMAP4460 Silicon Revision 1.x.

3.1. Device Power Management Introduction

3.1.1. AVS Overview

- SmartReflex Class-1.5 description is added.
- SmartReflex Class-2 description is removed.
- SmartReflex Class-3 description is updated.

3.2. PRCM Subsystem Overview

Refer to OMAP4460 Silicon Revision 1.x TRM.

3.3. PRCM Subsystem Environment

- New pin c2c_pwkup is added:
  - Pre-wakeup request input going directly to PRCM.
  - Used to wake up the device before the C2C_WAKEREQ_IN is asserted.

3.4. PRCM Subsystem Integration

Refer to OMAP4460 Silicon Revision 1.x TRM.

3.5. Reset Management Functional Description

- Updated bit-fields to warm reset insensitive:
  - List of registers impacted:
    - CM1_ABE_GPTIMER5_CLKCTRL
- New reset signals going to Cortex-A9 Memory Adapter are added:
  - MPU_MA_RST
  - MPU_MA_RET_RST
  - MPU_MA_PWRON_RET_RST

3.6. Clock Management Functional Description

- DCC feature is added for DPLL_MPU:
  - New section 'Tactical Clocking Adjustment' is added.
  - List of registers impacted:
    - CM_CLKSEL_DPLL_MPU
- New clocks EOCP_MA_ICLK and EOCP_L3_ICLK for EMIF modules added:
  - The two clocks are exclusive.
  - EMIF modules are clocked by EOCP_MA_ICLK when MPU is active, otherwise EOCP_L3_ICLK clock is used.
- New clock dividers added to form clocks versus DPLL_MPU_CLK:
  - List of registers impacted:
    - CM_MPU_MPU_CLKCTRL
- New clocks for BANDGAP and Control Module added:
  - WKUP_TS_FCLK is used as optional clock for BANDGAP instead of WKUP_32K_FCLK.
  - CORE_TS_FCLK is a new optional clock going to SYSCTRL_GENERAL_CORE.
  - List of registers impacted:
    - CM_WKUP_BANDGAP_CLKCTRL
    - CM_WKUP_CLKSTCTRL
    - CM_L4CFG_CLKSTCTRL
- New clock divider added to form WKUP_TS_FCLK and CORE_TS_FCLK:
  - L4WKUP_ICLK clock is going into the divider.

- Available divider options are 1/8, 1/16 and 1/32.
- List of registers impacted:
  - CM_WKUP_BANDGAP_CLKCTRL
- Reset value of Sigma-Delta divider is updated:
  - List of registers impacted:
    - CM_CLKSEL_DPLL_USB
- DELTAMSTEP bit-field updated for DPLL_USB:
  - List of registers impacted:
    - CM_SSC_DELTAMSTEP_DPLL_USB
- The Video DAC (VDAC) functionality is not supported

3.7. Power Management Functional Description

- New status bit-fields are added for last power state entered:
  - List of registers impacted:
    - PM_CAM_PWRSTST
    - PM_SGX_PWRSTST
    - PM_DSS_PWRSTST
    - PM_EMU_PWRSTST
- Wakeup dependencies are modified:
  - List of registers impacted:
    - PM_DSS_DSS_WKDEP
    - CM_L4CFG_DYNAMICDEP
    - CM_L4CFG_DYNAMICDEP_RESTORE
- Power down control setting is updated:
  - List of registers impacted:
    - CM_DIV_M4_DPLL_CORE
    - CM_DIV_M5_DPLL_CORE
    - CM_DIV_M6_DPLL_CORE
    - CM_DIV_M7_DPLL_CORE
    - CM_DIV_M4_DPLL_CORE_RESTORE
    - CM_DIV_M5_DPLL_CORE_RESTORE
    - CM_DIV_M6_DPLL_CORE_RESTORE
    - CM_DIV_M7_DPLL_CORE_RESTORE
    - CM_DIV_M4_DPLL_IVA
    - CM_DIV_M4_DPLL_PER
    - CM_DIV_M5_DPLL_PER
    - CM_DIV_M6_DPLL_PER
    - CM_DIV_M7_DPLL_PER
- MPU power domain controls are updated:
  - List of registers impacted:
    - PM_MPU_PWRSTCTRL

3.8. Voltage Management Functional Description

- New OPPs are available:
  - OPP119 is added for VDD_CORE_L.
  - OPP_NITRO is added for VDD_IVA_L.
  - OPP_NTSB is added for VDD_IVA_L and VDD_MPU_L.

ABB Set2 voltage mode is added. That mode is enabled at OPP_TURBO. ABB Set2 is enabled through ACTIVE_RBB_SEL bit.

ABB strategies for the Cortex-A9 MPU and IVA-HD (when operating at OPP_TURBO) are added.

3.9. Device Low-Power States

Refer to OMAP4460 Silicon Revision 1.x TRM.

3.10. PRCM Module Programming Guide

3.10.1. Voltage Management Low-Level Programming Models

Subsequence – FSM Configuration is updated.

Disable sequence for AVS (SmartReflex) and VP is added.

ABB Set2 mode is added in the **Changing OPP** procedure.

3.11. PRCM Register Manual

3.11.1. PRM Instance Summary

Table 3.1. PRM Instance Summary

Module Name	L4 Base Address	Size
INTRCONN_SOCKET_PRM	0x4A30 6000	256Bytes
CKGEN_PRM	0x4A30 6100	256Bytes
MPU_PRM	0x4A30 6300	256Bytes
DSP_PRM	0x4A30 6400	256Bytes
ABE_PRM	0x4A30 6500	256Bytes
ALWAYS_ON_PRM	0x4A30 6600	256Bytes
CORE_PRM	0x4A30 6700	2KBytes
IVAHD_PRM	0x4A30 6F00	256Bytes
CAM_PRM	0x4A30 7000	256Bytes
DSS_PRM	0x4A30 7100	256Bytes
SGX_PRM	0x4A30 7200	256Bytes
L3INIT_PRM	0x4A30 7300	256Bytes
L4PER_PRM	0x4A30 7400	512Bytes
WKUP_PRM	0x4A30 7700	256Bytes
WKUP_CM	0x4A30 7800	256Bytes
EMU_PRM	0x4A30 7900	256Bytes
EMU_CM	0x4A30 7A00	256Bytes
DEVICE_PRM	0x4A30 7B00	256Bytes
INSTR_PRM	0x4A30 7F00	256Bytes

3.11.2. INTRCONN_SOCKET_PRM Registers

Refer to OMAP4460 Silicon Revision 1.x TRM.

3.11.3. CKGEN_PRM Registers

Refer to OMAP4460 Silicon Revision 1.x TRM.

3.11.4. MPU_PRM Registers

3.11.4.1. MPU_PRM Register Summary

Table 3.2. MPU_PRM Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	MPU_PRM L4 Base Address
PM_MPU_PWRSTCTRL	RW	32	0x0000 0000	0x4A30 6300
PM_MPU_PWRSTST	R	32	0x0000 0004	0x4A30 6304
RM_MPU_RSTST	RW	32	0x0000 0014	0x4A30 6314
RM_MPU_MPU_CONTEXT	RW	32	0x0000 0024	0x4A30 6324

3.11.4.2. MPU_PRM Register Description

Note

This section contains only modified registers.

Table 3.3. PM_MPU_PWRSTCTRL

Address Offset	0x0000 0000		
Physical Address	SeeTable 3.2	**Instance**	MPU_PRM
Description	This register controls the MPU domain power state to reach upon a domain sleep transition		
Type	RW		

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
RESERVED	MPU_RAM_ONSTATE, MPU_L2_ONSTATE, ~~MPU_L1_ONSTATE~~ RESERVED	RESERVED, MPU_RAM_RETSTATE, MPU_L2_RETSTATE, MPU_L1_RETSTATE	RESERVED, LOWPOWERSTATECHANGE, RESERVED, LOGICRETSTATE, POWERSTATE

Bits	Field Name	Description	Type	Reset
31:22	RESERVED		R	0x000
21:20	MPU_RAM_ONSTATE	MPU_RAM memory state when domain is ON. Read 0x3: Memory bank is on when the domain is ON.	R Returns1s	0x3
19:18	MPU_L2_ONSTATE	MPU_L2 memory state when domain is ON. Read 0x3: Memory bank is on when the domain is ON.	R Returns1s	0x3
~~17:16~~	~~MPU_L1_ONSTATE~~	~~MPU_L1 memory state when domain is ON.~~ ~~Read 0x3: Memory bank is on when the domain is ON.~~	~~R Returns1s~~	~~0x3~~
~~15~~17:11	RESERVED		R	0x00
10	MPU_RAM_RETSTATE	MPU_RAM memory state when domain is RETENTION. 0x0: Memory bank is off when the domain is in the RETENTION state. ~~Read 1:~~0x1: Memory bank is retained when domain is in RETENTION state.	~~RW~~ RO Returns1s	1
9	MPU_L2_RETSTATE	MPU_L2 memory state when domain is RETENTION. 0x0: Memory bank is off when the domain is in the RETENTION state. 0x1: Memory bank is retained when domain is in RETENTION state.	RW	1
~~8~~	~~MPU_L1_RETSTATE~~	~~MPU_L1 memory state when domain is RETENTION. Should always be same as LogicRETState bit-field.~~ ~~0x0: Memory bank is off when the domain is in the RETENTION state.~~ ~~0x1: Memory bank is retained when domain is in RETENTION state.~~	~~RW~~	~~1~~
~~7~~8:5	RESERVED		R	0x0
4	LOWPOWERSTATECHANGE	Power state change request when domain has already performed a sleep transition. Allows going into deeper low power state without waking up the power domain.	RW W Special	0

Bits	Field Name	Description	Type	Reset
		0x0: Do not request a low power state change. 0x1: Request a low power state change. This bit is automatically cleared when the power state is effectively changed or when power state is ON.		
3	RESERVED		R	0
2	LOGICRETSTATE	Logic state when power domain is RETENTION 0x0: Only retention registers are retained and remaing logic is off when the domain is in RETENTION state. 0x1: Whole logic is retained when domain is in RETENTION state.	RW	1
1:0	POWERSTATE	Power state control. 0x0: OFF state 0x1: RETENTION state 0x2: INACTIVE state 0x3: ON State	RW	0x3

Table 3.4. Register Call Summary for Register PM_MPU_PWRSTCTRL

Power Management Functional Description
• Power Management Functional Description:[0]

Table 3.5. PM_MPU_PWRSTST

Address Offset	0x0000 0004		
Physical Address	SeeTable 3.2	**Instance**	MPU_PRM
Description	This register provides a status on the MPU domain current power state. [warm reset insensitive]		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								LASTPOWERSTATEENTERED								RESERVED				INTRANSITION				RESERVED				MPU_RAM_STATEST		MPU_L2_STATEST		MPU_L1_STATEST	RESERVED			RESERVED		LOGICSTATEST		POWERSTATEST	

Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25:24	LASTPOWERS-TATEENTERED	Last low power state entered. Set to 0x3 upon write of the same only. This register is intended for debug purpose only. Read 0x3: Power domain was previously ON-ACTIVE Read 0x2: Power domain was previously ON-INACTIVE Read 0x1: Power domain was previously in RETENTION	RW W 1toSet	0x0

Bits	Field Name	Description	Type	Reset
		Read 0x0: Power domain was previously OFF		
23:21	RESERVED		R	0x0
20	INTRANSITION	Domain transition status Read 0x0: No on-going transition on power domain Read 0x1: Power domain transition is in progress.	R	0
19:10	RESERVED		R	0x000
9:8	MPU_RAM_STATEST	MPU_RAM memory state status Read 0x0: Memory is OFF Read 0x1: Memory is RETENTION Read 0x2: Reserved Read 0x3: Memory is ON	R	0x3
7:6	MPU_L2_STATEST	MPU_L2 memory state status Read 0x0: Memory is OFF Read 0x1: Memory is RETENTION Read 0x2: Reserved Read 0x3: Memory is ON	R	0x3
~~5:4~~	~~MPU_L1_STATEST~~	~~MPU_L1 memory state status~~ ~~Read 0x0: Memory is OFF~~ ~~Read 0x1: Reserved~~ ~~Read 0x2: Reserved~~ ~~Read 0x3: Memory is ON~~	~~R~~	~~0x3~~
5:3	RESERVED		R	0x0
2	LOGICSTATEST	Logic state status Read 0x0: Logic in domain is OFF Read 0x1: Logic in domain is ON	R	1
1:0	POWERSTATEST	Current power state status Read 0x0: Power domain is OFF Read 0x1: Power domain is in RETENTION Read 0x2: Power domain is ON-INACTIVE Read 0x3: Power domain is ON-ACTIVE	R	0x3

Table 3.6. RM_MPU_MPU_CONTEXT

Address Offset	0x0000 0024		
Physical Address	See Table 3.2	**Instance**	MPU_PRM
Description	This register contains dedicated MPU context statuses. [warm reset insensitive]		
Type	RW		

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
RESERVED	LOSTMEM_MPU_RAM	LOSTMEM_MPU_L2	~~LOSTMEM_MPU_L1~~ RESERVED	~~RESERVED~~ LOSTCONTEXT_RFF	LOSTCONTEXT_DFF

Bits	Field Name	Description	Type	Reset
31:11	RESERVED		R	0x000000
10	LOSTMEM_MPU_RAM	Specify if memory-based context in MPU_RAM memory bank has been lost due to a previous power transition or other reset source (not affected by a global warm reset). 0x0: Context has been maintained 0x1: Context has been lost	RW W 1toClr	1
9	LOSTMEM_MPU_L2	Specify if memory-based context in MPU_L2 memory bank has been lost due to a previous power transition or other reset source. 0x0: Context has been maintained 0x1: Context has been lost	RW W 1toClr	1
8	~~LOSTMEM_MPU_L1~~	~~Specify if memory-based context in MPU_L1 memory bank has been lost due to a previous power transition or other reset source. Not applicable to Cortex-A9 SMP.~~ ~~0x0: Context has been maintained~~ ~~0x1: Context has been lost~~	~~RW W 1toClr~~	~~1~~
~~7:1~~8:2	RESERVED		R	0x00
1	LOSTCONTEXT_RFF	Specify if RFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of MPU_MA_PWRON_RET_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W 1toClr	1
0	LOSTCONTEXT_DFF	Specify if DFF-based context has been lost due to a previous power transition or other reset source. (set upon assertion of MPU_RST signal) 0x0: Context has been maintained 0x1: Context has been lost	RW W 1toClr	1

3.11.5. DSP_PRM Registers

Refer to OMAP4460 Silicon Revision 1.x TRM.

3.11.6. ABE_PRM Registers

Refer to OMAP4460 Silicon Revision 1.x TRM.

3.11.7. ALWAYS_ON_PRM Registers

Refer to OMAP4460 Silicon Revision 1.x TRM.

3.11.8. CORE_PRM Registers

Refer to OMAP4460 Silicon Revision 1.x TRM.

3.11.9. IVAHD_PRM Registers

Refer to OMAP4460 Silicon Revision 1.x TRM.

3.11.10. CAM_PRM Registers

3.11.10.1. CAM_PRM Register Summary

Table 3.7. CAM_PRM Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	CAM_PRM L4 Base Address
PM_CAM_PWRSTCTRL	RW	32	0x0000 0000	0x4A30 7000
PM_CAM_PWRSTST	RW	32	0x0000 0004	0x4A30 7004
RM_CAM_ISS_CONTEXT	RW	32	0x0000 0024	0x4A30 7024
RM_CAM_FDIF_CONTEXT	RW	32	0x0000 002C	0x4A30 702C

3.11.10.2. CAM_PRM Register Description

Note

This section contains only modified registers.

Table 3.8. PM_CAM_PWRSTST

Address Offset	0x0000 0004		
Physical Address	See Table 3.7	**Instance**	CAM_PRM
Description	This register provides a status on the current CAM power domain state. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						RESERVED LASTPOWERSTATEENTERED		RESERVED			INTRANSITION	RESERVED												CAM_MEM_STATEST				RESERVED		LOGICSTATEST	POWERSTATEST	

Bits	Field Name	Description	Type	Reset
31:2126	RESERVED		R	0x000
25:24	LASTPOWERSTATEENTERED	Last low power state entered. Set to 0x3 upon write of the same only. This register is intended for debug purpose only. Read 0x0: Power domain was previously ON-ACTIVE Read 0x1: Power domain was previously ON-INACTIVE Read 0x2: Power domain was previously in RETENTION Read 0x3: Power domain was previously ON-ACTIVE	RW W 1toSet	0x0

Bits	Field Name	Description	Type	Reset
23:21	RESERVED		R	0x000
20	INTRANSITION	Domain transition status Read 0x0: No on-going transition on power domain Read 0x1: Power domain transition is in progress.	R	0
19:6	RESERVED		R	0x0000
5:4	CAM_MEM_STATEST	CAM_MEM memory state status Read 0x0: Memory is OFF Read 0x1: Reserved Read 0x2: Reserved Read 0x3: Memory is ON	R	0x3
3	RESERVED		R	0
2	LOGICSTATEST	Logic state status Read 0x0: Logic in domain is OFF Read 0x1: Logic in domain is ON	R	1
1:0	POWERSTATEST	Current power state status Read 0x0: Power domain is OFF Read 0x1: Power domain is in RETENTION Read 0x2: Power domain is ON-INACTIVE Read 0x3: Power domain is ON-ACTIVE	R	0x3

Table 3.9. Register Call Summary for Register PM_CAM_PWRSTST

Power Management Functional Description

- Power Management Functional Description:[0]

3.11.11. DSS_PRM Registers

3.11.11.1. DSS_PRM Register Summary

Table 3.10. DSS_PRM Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	DSS_PRM Base Address
PM_DSS_PWRSTCTRL	RW	32	0x0000 0000	0x4A30 7100
PM_DSS_PWRSTST	RW	32	0x0000 0004	0x4A30 7104
PM_DSS_DSS_WKDEP	RW	32	0x0000 0020	0x4A30 7120
RM_DSS_DSS_CONTEXT	RW	32	0x0000 0024	0x4A30 7124
RM_DSS_DEISS_CONTEXT	RW	32	0x0000 002C	0x4A30 712C

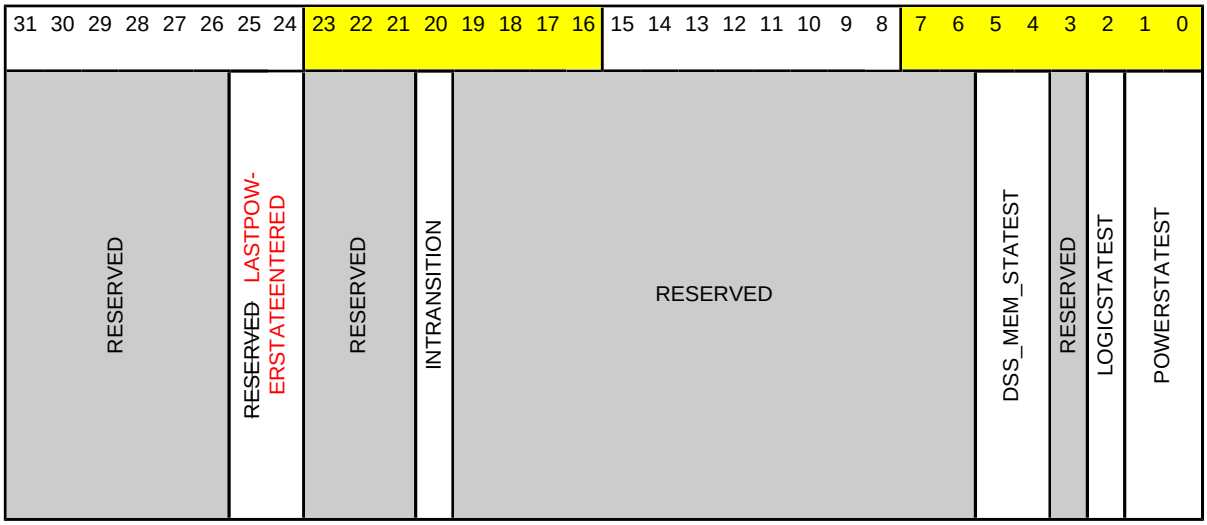
3.11.11.2. DSS_PRM Register Description

Note

This section contains only modified registers.

Table 3.11. PM_DSS_PWRSTST

Address Offset	0x0000 0004		
Physical Address	SeeTable 3.10	**Instance**	DSS_PRM
Description	This register provides a status on the current DSS power domain state. [warm reset insensitive]		
Type	R		



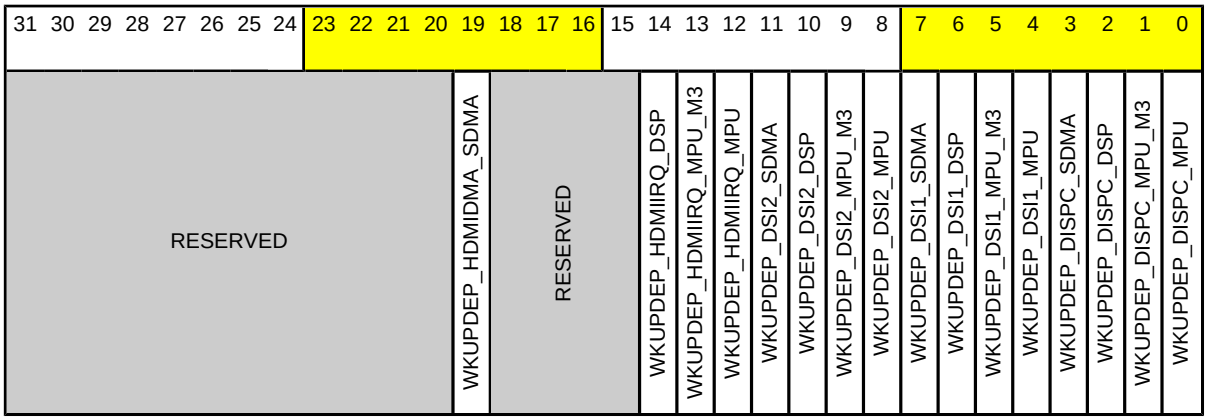
Bits	Field Name	Description	Type	Reset
31:21~~26~~	RESERVED		R	0x00
25:24	LASTPOWERS-TATEENTERED	Last low power state entered. Set to 0x3 upon write of the same only. This register is intended for de-bug purpose only. Read 0x0: Power domain was previously OFF Read 0x1: Power domain was previously in RETENTION Read 0x2: Power domain was previously ON-INACTIVE Read 0x3: Power domain was previously ON-ACTIVE	RW W 1toSet	0x0
23:21	RESERVED		R	0x0
20	INTRANSITION	Domain transition status Read 0x0: No on-going transition on power domain Read 0x1: Power domain transition is in progress.	R	0
19:6	RESERVED		R	0x0000
5:4	DSS_MEM_STATEST	DSS_MEM state status Read 0x0: Memory is OFF Read 0x1: Reserved Read 0x2: Reserved Read 0x3: Memory is ON	R	0x3
3	RESERVED		R	0
2	LOGICSTATEST	Logic state status Read 0x0: Logic in domain is OFF Read 0x1: Logic in domain is ON	R	1
1:0	POWERSTATEST	Current power state status Read 0x0: Power domain is OFF Read 0x1: Power domain is in RETENTION Read 0x2: Power domain is ON-INACTIVE Read 0x3: Power domain is ON-ACTIVE	R	0x3

Table 3.12. Register Call Summary for Register PM_DSS_PWRSTST

Power Management Functional Description
• Power Management Functional Description:[0]

Table 3.13. PM_DSS_DSS_WKDEP

Address Offset	0x0000 0020		
Physical Address	SeeTable 3.10	**Instance**	DSS_PRM
Description	This register controls wakeup dependency based on DSS service requests.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:20	RESERVED		R	0x000
19	WKUPDEP_HDMIDMA_SD-MA	Wakeup dependency from HDMI module (SWakeup_HDMI_dma signal) towards SDMA + L3_2 domains ~~0x0: Dependency is disabled~~ 0x1: Dependency is enabled	RW~~W~~Rreturns1s	1
18:15	RESERVED		R	0x0
14	WKUPDEP_HDMIIRQ_DSP	Wakeup dependency from HDMI module (SWakeup_HDMI_irq signal) towards DSP + L3_1 + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
13	WKUPDEP_HD-MIIRQ_MPU_M3	Wakeup dependency from HDMI module (SWakeup_HDMI_irq signal) towards MPU_A3 + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
12	WKUPDEP_HDMIIRQ_MPU	Wakeup dependency from HDMI module (SWakeup_HDMI_irq signal) towards MPU + L3_1 + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
11	WKUPDEP_DSI2_SDMA	Wakeup dependency from DSI2 module (SWakeup_DSI2 signal) towards SDMA + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
10	WKUPDEP_DSI2_DSP	Wakeup dependency from DSI2 module (SWakeup_DSI2 signal) towards DSP + L3_1 + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
9	WKUPDEP_DSI2_MPU_M3	Wakeup dependency from DSI2 module (SWakeup_DSI2 signal) towards MPU_A3 + L3_2 domains	RW	0

Bits	Field Name	Description	Type	Reset
		0x0: Dependency is disabled 0x1: Dependency is enabled		
8	WKUPDEP_DSI2_MPU	Wakeup dependency from DSI2 module (SWakeup_DSI2 signal) towards MPU + L3_1 + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
7	WKUPDEP_DSI1_SDMA	Wakeup dependency from DSI1 module (SWakeup_DSI1 signal) towards SDMA + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
6	WKUPDEP_DSI1_DSP	Wakeup dependency from DSI1 module (SWakeup_DSI1 signal) towards DSP + L3_1 + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
5	WKUPDEP_DSI1_MPU_M3	Wakeup dependency from DSI1 module (SWakeup_DSI1 signal) towards MPU_A3 + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
4	WKUPDEP_DSI1_MPU	Wakeup dependency from DSI1 module (SWakeup_DSI1 signal) towards MPU + L3_1 + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
3	WKUPDEP_DISPC_SDMA	Wakeup dependency from DISPC module (SWake-up_DISPC signal) towards SDMA + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
2	WKUPDEP_DISPC_DSP	Wakeup dependency from DISPC module (SWake-up_DISPC signal) towards DSP + L3_1 + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
1	WKUPDEP_DISPC_MPU_M3	Wakeup dependency from DISPC module (SWake-up_DISPC signal) towards MPU_A3 + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0
0	WKUPDEP_DISPC_MPU	Wakeup dependency from DISPC module (SWake-up_DISPC signal) towards MPU + L3_1 + L3_2 domains 0x0: Dependency is disabled 0x1: Dependency is enabled	RW	0

Table 3.14. Register Call Summary for Register PM_DSS_DSS_WKDEP

Power Management Functional Description
• Power Management Functional Description:[0]

3.11.12. SGX_PRM Registers

3.11.12.1. SGX_PRM Register Summary

Table 3.15. SGX_PRM Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	GFX_PRM Base Address
PM_SGX_PWRSTCTRL	RW	32	0x0000 0000	0x4A30 7200
PM_SGX_PWRSTST	RW	32	0x0000 0004	0x4A30 7204
RM_SGX_SGX_CONTEXT	RW	32	0x0000 0024	0x4A30 7224

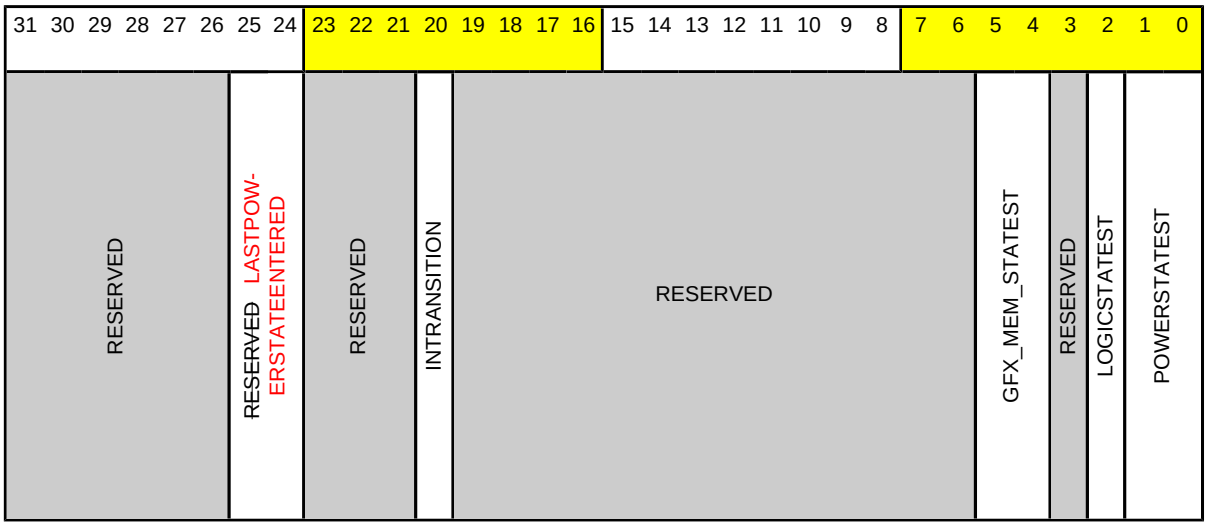
3.11.12.2. SGX_PRM Register Description

Note

This section contains only modified registers.

Table 3.16. PM_SGX_PWRSTST

Address Offset	0x0000 0004		
Physical Address	Please refer toTable 3.15	**Instance**	SGX_PRM
Description	This register provides a status on the current GFX power domain state. [warm reset insensitive]		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:~~21~~26	RESERVED		R	0x00
25:24	LASTPOWERS-TATEENTERED	Last low power state entered. Set to 0x3 upon write of the same only. This register is intended for de-bug purpose only. Read 0x0: Power domain was previously OFF Read 0x1: Power domain was previously in RETENTION Read 0x2: Power domain was previously ON-INACTIVE Read 0x3: Power domain was previously ON-ACTIVE	RW W 1toSet	0x0

Bits	Field Name	Description	Type	Reset
23:21	RESERVED		R	0x0
20	INTRANSITION	Domain transition status Read 0x1: Power domain transition is in progress. Read 0x0: No on-going transition on power domain	R	0
19:6	RESERVED		R	0x0000
5:4	GFX_MEM_STATEST	GFX_MEM memory bank state status Read 0x3: Memory is ON Read 0x2: Reserved Read 0x1: Reserved Read 0x0: Memory is OFF	R	0x3
3	RESERVED		R	0
2	LOGICSTATEST	Logic state status Read 0x1: Logic in domain is ON Read 0x0: Logic in domain is OFF	R	1
1:0	POWERSTATEST	Current power state status Read 0x3: Power domain is ON-ACTIVE Read 0x2: Power domain is ON-INACTIVE Read 0x1: Power domain is in RETENTION Read 0x0: Power domain is OFF	R	0x3

Table 3.17. Register Call Summary for Register PM_SGX_PWRSTST

Power Management Functional Description

- Power Management Functional Description:[0]

3.11.13. L3INIT_PRM Registers

Refer to OMAP4460 Silicon Revision 1.x TRM.

3.11.14. L4PER_PRM Registers

Refer to OMAP4460 Silicon Revision 1.x TRM.

3.11.15. WKUP_PRM Registers

Refer to OMAP4460 Silicon Revision 1.x TRM.

3.11.16. WKUP_CM Registers

3.11.16.1. WKUP_CM Register Summary

Table 3.18. WKUP_CM Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	WKUP_CM L4 Base Address
CM_WKUP_CLKSTC-TRL	RW	32	0x0000 0000	0x4A30 7800
CM_WKUP_L4WKUP_CLKCTRL	R	32	0x0000 0020	0x4A30 7820
RESERVED	R	32	0x0000 0028	0x4A30 7828

Register Name	Type	Register Width (Bits)	Address Offset	WKUP_CM L4 Base Address
CM_WKUP_WDTIMER2_CLKCTRL	RW	32	0x0000 0030	0x4A30 7830
CM_WKUP_GPIO1_CLKCTRL	RW	32	0x0000 0038	0x4A30 7838
CM_WKUP_GPTIMER1_CLKCTRL	RW	32	0x0000 0040	0x4A30 7840
RESERVED	R	32	0x0000 0048	0x4A30 7848
CM_WKUP_32KTIMER_CLKCTRL	R	32	0x0000 0050	0x4A30 7850
RESERVED	RW	32	0x0000 0058	0x4A30 7858
CM_WKUP_SARRAM_CLKCTRL	R	32	0x0000 0060	0x4A30 7860
CM_WKUP_KEYBOARD_CLKCTRL	RW	32	0x0000 0078	0x4A30 7878
RESERVED	RW	32	0x0000 0080	0x4A30 7880
CM_WKUP_BANDGAP_CLKCTRL	RW	32	0x0000 0088	0x4A30 7888

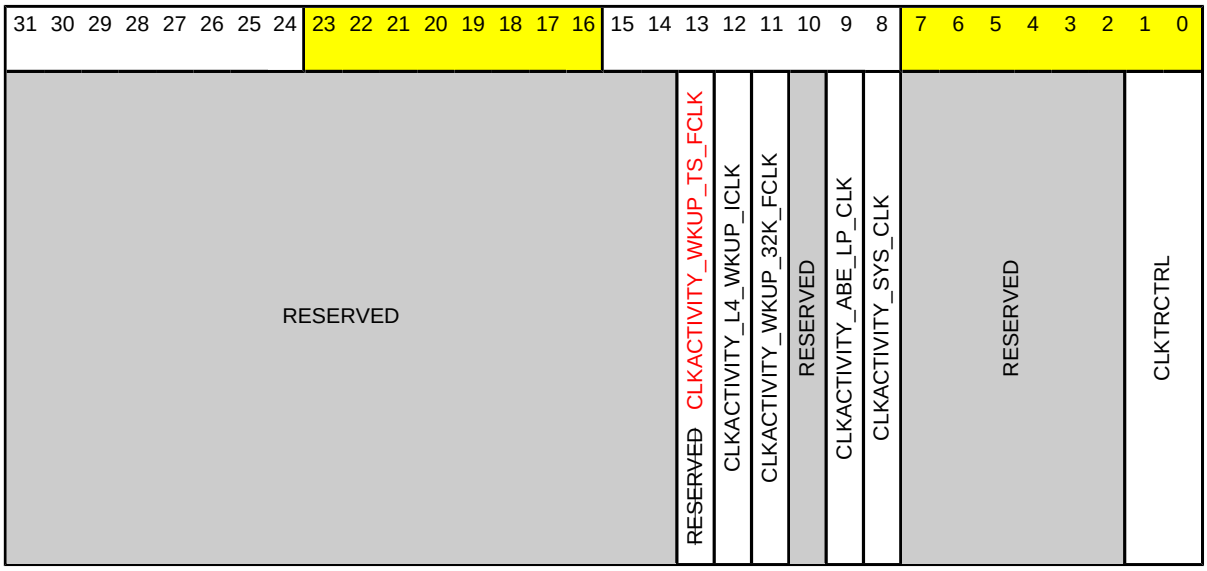
3.11.16.2. WKUP_CM Register Description

Note

This section contains only modified registers.

Table 3.19. CM_WKUP_CLKSTCTRL

Address Offset	0x0000 0000		
Physical Address	See Table 3.18	**Instance**	WKUP_CM
Description	This register enables the domain power state transition. It controls the HW supervised domain power state transition between ON-ACTIVE and ON-INACTIVE states. It also hold one status bit per clock input of the domain.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:~~13~~14	RESERVED		R	0x00000
13			R	0

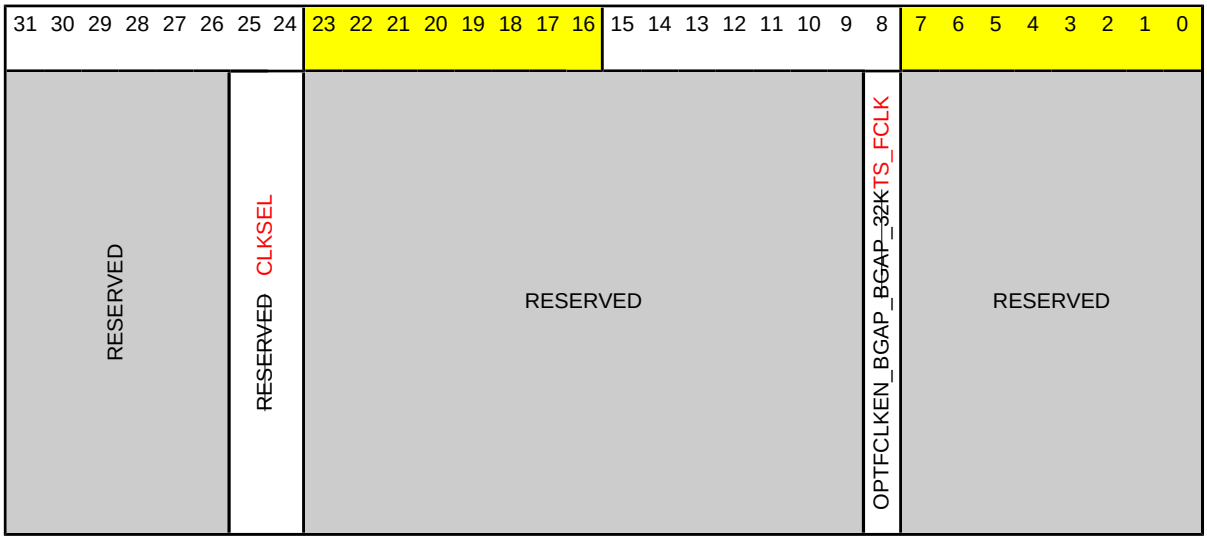
Bits	Field Name	Description	Type	Reset
	CLKACTIVITY_WKUP_TS_FCLK	This field indicates the state of the WKUP_TS_FCLK clock in the domain. [warm reset insensitive] Read 0x1: Corresponding clock is running or gating/ungating transition is on-going Read 0x0: Corresponding clock is definitely gated		
12	CLKACTIVITY_L4_WKUP_ICLK	This field indicates the state of the clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0
11	CLKACTIVITY_WKUP_32K_FCLK	This field indicates the state of the clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0
10	RESERVED		R	0
9	CLKACTIVITY_ABE_LP_CLK	This field indicates the state of the clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0
8	CLKACTIVITY_SYS_CLK	This field indicates the state of the SYS_CLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0
7:2	RESERVED		R	0x00
1:0	CLKTRCTRL	Controls the clock state transition of the WKUP clock domain. 0x0: NO_SLEEP: Sleep transition cannot be initiated. Wakeup transition may however occur. Read 0x1: Reserved Read 0x2: Reserved 0x3: HW_AUTO: Automatic transition is enabled. Sleep and wakeup transition are based upon hardware conditions.	RW	0x0

Table 3.20. Register Call Summary for Register CM_WKUP_CLKSTCTRL

Clock Management Functional Description
• Clock Management Functional Description:[0]

Table 3.21. CM_WKUP_BANDGAP_CLKCTRL

Address Offset	0x0000 0088		
Physical Address	See Table 3.18	**Instance**	WKUP_CM
Description	This register manages the ~~bandgap clock.~~ clock delivered to Bandgap and SYSCTRL_GENERAL_CORE modules for the Thermal Sensor feature. [warm reset insensitive]		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:926	RESERVED		R	0x000000
25:24	CLKSEL	Selects the divider value for generating the Thermal Sensor clock from L4WKUP_ICLK source. The divider has to be selected so as to guarantee a frequency between 1MHz and 2MHz. 0x0: Divide by 8 0x1: Divide by 16 0x2: Divide by 32 0x3: Reserved	RW	0x2
23:9	RESERVED		R	0x0000
8	OPTFCLKEN_BGAP_32K TS_FCLK	Optional functional clock control. 0x0: Optional functional clock is disabled 0x1: Optional functional clock is enabled	RW	0
7:0	RESERVED		R	0x00

Table 3.22. Register Call Summary for Register CM_WKUP_BANDGAP_CLKCTRL

Clock Management Functional Description

- Clock Management Functional Description:[0][1]

3.11.17. EMU_PRM Registers

3.11.17.1. EMU_PRM Register Summary

Table 3.23. EMU_PRM Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	EMU_PRM L4 Base Address
PM_EMU_PWRST CTRL	R	32	0x0000 0000	0x4A30 7900
PM_EMU_PWRSTST	R	32	0x0000 0004	0x4A30 7904
RM_EMU_DEBUG SS_CONTEXT	RW	32	0x0000 0024	0x4A30 7924

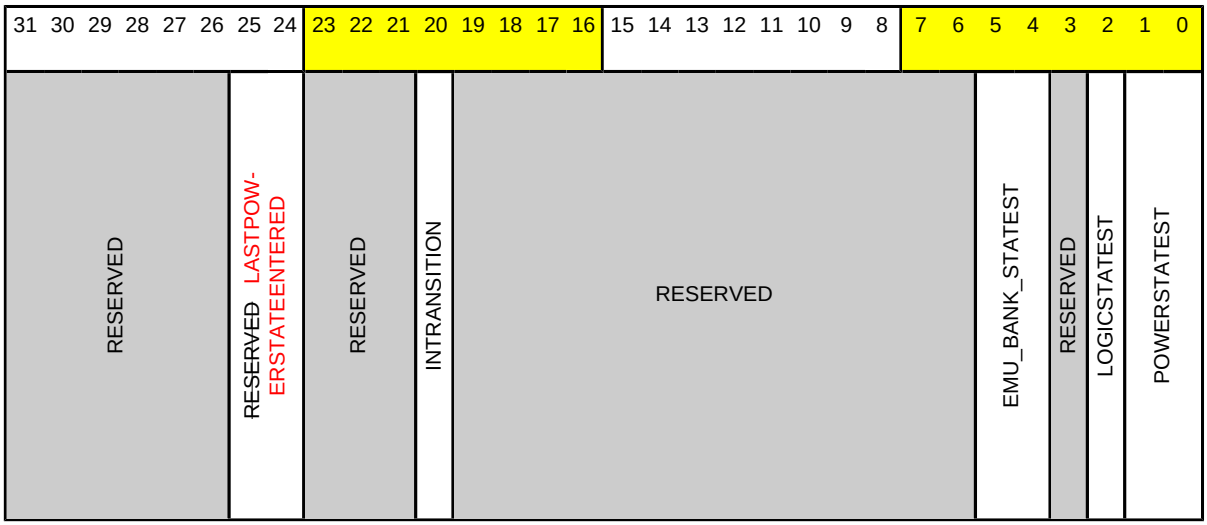
3.11.17.2. EMU_PRM Register Description

Note

This section contains only modified registers.

Table 3.24. PM_EMU_PWRSTST

Address Offset	0x0000 0004		
Physical Address	SeeTable 3.23	**Instance**	EMU_PRM
Description	This register provides a status on the EMU domain current power state. [warm reset insensitive]		
Type	R		



Bits	Field Name	Description	Type	Reset
31:21~~26~~	RESERVED		R	0x000
25:24	LASTPOWERS-TATEENTERED	Last low power state entered. Set to 0x3 upon write of the same only. This register is intended for debug purpose only. Read 0x0: Power domain was previously ON-ACTIVE Read 0x1: Power domain was previously ON-INACTIVE Read 0x2: Power domain was previously in RETENTION Read 0x3: Power domain was previously ON-ACTIVE	RW W 1toSet	0x0
23:21	RESERVED		R	0x000
20	INTRANSITION	Domain transition status Read 0x0: No on-going transition on power domain Read 0x1: Power domain transition is in progress.	R	0
19:6	RESERVED		R	0x0000
5:4	EMU_BANK_STATEST	EMU memory bank state status Read 0x0: Memory is OFF Read 0x1: Reserved Read 0x2: Reserved Read 0x3: Memory is ON It is supplied by WKUP LDO	R	0x3
3	RESERVED		R	0
2	LOGICSTATEST	Logic state status Read 0x0: Logic in domain is OFF Read 0x1: Logic in domain is ON	R	1
1:0	POWERSTATEST	Current power state status Read 0x0: Power domain is OFF Read 0x3: Power domain is ON-ACTIVE	R	0x3

Table 3.25. Register Call Summary for Register PM_EMU_PWRSTST

Power Management Functional Description
• Power Management Functional Description:[0]

3.11.18. EMU_CM Registers

Refer to OMAP4460 Silicon Revision 1.x TRM.

3.11.19. DEVICE_PRM Registers

3.11.19.1. DEVICE_PRM Register Summary

Table 3.26. DEVICE_PRM Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	DEVICE_PRM Base Address
PRM_RSTCTRL	RW	32	0x0000 0000	0x4A30 7B00
PRM_RSTST	RW	32	0x0000 0004	0x4A30 7B04
PRM_RSTTIME	RW	32	0x0000 0008	0x4A30 7B08
PRM_CLKREQCTRL	RW	32	0x0000 000C	0x4A30 7B0C
PRM_VOLTCTRL	RW	32	0x0000 0010	0x4A30 7B10
PRM_PWRREQCTRL	RW	32	0x0000 0014	0x4A30 7B14
PRM_PSCON_COUNT	RW	32	0x0000 0018	0x4A30 7B18
PRM_IO_COUNT	RW	32	0x0000 001C	0x4A30 7B1C
PRM_IO_PMCTRL	RW	32	0x0000 0020	0x4A30 7B20
PRM_VOLTSE-TUP_WARMRESET	RW	32	0x0000 0024	0x4A30 7B24
PRM_VOLTSE-TUP_CORE_OFF	RW	32	0x0000 0028	0x4A30 7B28
PRM_VOLTSE-TUP_MPU_OFF	RW	32	0x0000 002C	0x4A30 7B2C
PRM_VOLTSE-TUP_IVA_OFF	RW	32	0x0000 0030	0x4A30 7B30
PRM_VOLTSE-TUP_CORE _RET_SLEEP	RW	32	0x0000 0034	0x4A30 7B34
PRM_VOLTSE-TUP_MPU _RET_SLEEP	RW	32	0x0000 0038	0x4A30 7B38
PRM_VOLTSE-TUP_IVA _RET_SLEEP	RW	32	0x0000 003C	0x4A30 7B3C
PRM_VP_CORE_ CONFIG	RW	32	0x0000 0040	0x4A30 7B40
PRM_VP_CORE_STAT US	R	32	0x0000 0044	0x4A30 7B44
PRM_VP_CORE_VLIMIT-TO	RW	32	0x0000 0048	0x4A30 7B48
PRM_VP_CORE_ VOLTAGE	RW	32	0x0000 004C	0x4A30 7B4C
PRM_VP_CORE_ VSTEPMAX	RW	32	0x0000 0050	0x4A30 7B50
PRM_VP_CORE_ VSTEPMIN	RW	32	0x0000 0054	0x4A30 7B54
PRM_VP_MPU_CON-FIG	RW	32	0x0000 0058	0x4A30 7B58
PRM_VP_MPU_S TATUS	R	32	0x0000 005C	0x4A30 7B5C

Register Name	Type	Register Width (Bits)	Address Offset	DEVICE_PRM Base Address
PRM_VP_MPU_VLIMITTO	RW	32	0x0000 0060	0x4A30 7B60
PRM_VP_MPU_VOLTAGE	RW	32	0x0000 0064	0x4A30 7B64
PRM_VP_MPU_VSTEPMAX	RW	32	0x0000 0068	0x4A30 7B68
PRM_VP_MPU_VSTEPMIN	RW	32	0x0000 006C	0x4A30 7B6C
PRM_VP_IVA_CONFIG	RW	32	0x0000 0070	0x4A30 7B70
PRM_VP_IVA_STATUS	R	32	0x0000 0074	0x4A30 7B74
PRM_VP_IVA_VLIMITTO	RW	32	0x0000 0078	0x4A30 7B78
PRM_VP_IVA_VOLTAGE	RW	32	0x0000 007C	0x4A30 7B7C
PRM_VP_IVA_VSTEPMAX	RW	32	0x0000 0080	0x4A30 7B80
PRM_VP_IVA_VSTEPMIN	RW	32	0x0000 0084	0x4A30 7B84
PRM_VC_SMPS_SA	RW	32	0x0000 0088	0x4A30 7B88
PRM_VC_VAL_SMPS_RA_VOL	RW	32	0x0000 008C	0x4A30 7B8C
PRM_VC_VAL_SMPS_RA_CMD	RW	32	0x0000 0090	0x4A30 7B90
PRM_VC_VAL_CMD_VDD_CORE_L	RW	32	0x0000 0094	0x4A30 7B94
PRM_VC_VAL_CMD_VDD_MPU_L	RW	32	0x0000 0098	0x4A30 7B98
PRM_VC_VAL_CMD_VDD_IVA_L	RW	32	0x0000 009C	0x4A30 7B9C
PRM_VC_VAL_BYPASS	RW	32	0x0000 00A0	0x4A30 7BA0
PRM_VC_CFG_CHANNEL	RW	32	0x0000 00A4	0x4A30 7BA4
PRM_VC_CFG_I2C_MODE	RW	32	0x0000 00A8	0x4A30 7BA8
PRM_VC_CFG_I2C_CLK	RW	32	0x0000 00AC	0x4A30 7BAC
PRM_SRAM_COUNT	RW	32	0x0000 00B0	0x4A30 7BB0
PRM_SRAM_WKUP_SETUP	RW	32	0x0000 00B4	0x4A30 7BB4
PRM_LDO_SRAM_CORE_SETUP	RW	32	0x0000 00B8	0x4A30 7BB8
PRM_LDO_SRAM_CORE_CTRL	RW	32	0x0000 00BC	0x4A30 7BBC
PRM_LDO_SRAM_MPU_SETUP	RW	32	0x0000 00C0	0x4A30 7BC0
PRM_LDO_SRAM_MPU_CTRL	RW	32	0x0000 00C4	0x4A30 7BC4
PRM_LDO_SRAM_IVA_SETUP	RW	32	0x0000 00C8	0x4A30 7BC8
PRM_LDO_SRAM_IVA_CTRL	RW	32	0x0000 00CC	0x4A30 7BCC
PRM_LDO_ABB_MPU_SETUP	RW	32	0x0000 00D0	0x4A30 7BD0

Register Name	Type	Register Width (Bits)	Address Offset	DEVICE_PRM Base Address
PRM_LDO_ABB_MPU_CTRL	RW	32	0x0000 00D4	0x4A30 7BD4
PRM_LDO_ABB_IVA_SETUP	RW	32	0x0000 00D8	0x4A30 7BD8
PRM_LDO_ABB_IVA_CTRL	RW	32	0x0000 00DC	0x4A30 7BDC
PRM_LDO_BANDGAP_SETUP	RW	32	0x0000 00E0	0x4A30 7BE0
PRM_DEVICE_OFF_CTRL	RW	32	0x0000 00E4	0x4A30 7BE4
PRM_PHASE1_CNDP	R	32	0x0000 00E8	0x4A30 7BE8
PRM_PHASE2A_CNDP	R	32	0x0000 00EC	0x4A30 7BEC
PRM_PHASE2B_CNDP	R	32	0x0000 00F0	0x4A30 7BF0
PRM_MODEM_IF_CTRL	RW	32	0x0000 00F4	0x4A30 7BF4
PRM_VC_ERRST	RW	32	0x0000 00F8	0x4A30 7BF8

3.11.19.2. DEVICE_PRM Register Description

Note

This section contains only modified registers.

Table 3.27. PRM_LDO_ABB_MPU_SETUP

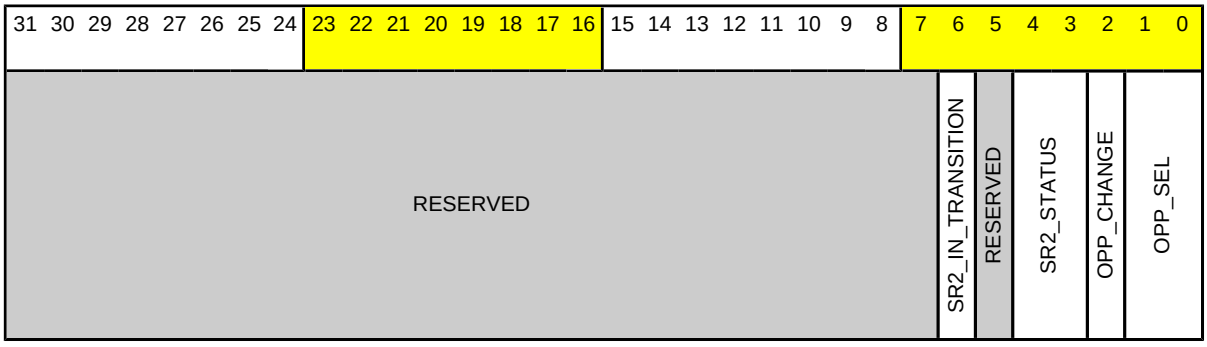
Address Offset	0x0000 00D0		
Physical Address	0x4A30 7BD0	**Instance**	DEVICE_PRM
Description	Selects the MPU_ABB LDO mode.		
Type	RW		

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
RESERVED		SR2_WTCNT_VALUE	RESERVED / NOCAP_EXPORT / RESERVED / ACTIVE_FBB_SEL / RESERVED ACTIVE_RBB_SEL / SR2EN

Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15:8	SR2_WTCNT_VALUE	LDO settling time for active-mode OPP change. Counting at a 16 system clock cycles rate. Target is 50us. [warm reset insensitive]	RW	0x00
7:5	RESERVED		R	0x0
4	NOCAP_EXPORT	Defines whether ABB LDO is cap-less or not. After PowerOn reset and Efuse sensing, this bit field is automatically loaded with an Efuse value from control module. Bit field remains writable after this. [warm reset insensitive] 0x0: ABB LDO uses an external cap 0x1: ABB LDO does not use an external cap	RW W Special	0
3	RESERVED	Reserved	RW	0
2	ACTIVE_FBB_SEL	Defines ABB LDO mode when voltage is in slow fast OPP. [warm reset insensitive] 0x0: ABB LDO is in bypass mode 0x1: ABB LDO is in ABB Set1 mode	RW	0
1	~~RESERVED~~ACTIVE_RBB_SEL	~~Reserved~~Defines ABB LDO mode when MPU voltage is in OPP_TURBO. [warm reset insensitive] 0x0: ABB LDO is in bypass mode 0x1: ABB LDO is in ABB Set2 mode	RW	0
0	SR2EN	Enable ABB power management 0x0: ABB LDO is put in bypass mode 0x1: ABB LDO will operate accordingly to settings	RW	0

Table 3.28. PRM_LDO_ABB_MPU_CTRL

Address Offset	0x0000 00D4		
Physical Address	0x4A30 7BD4	**Instance**	DEVICE_PRM
Description	Control and Status of ABB on MPU voltage domain. [warm reset insensitive]		
Type	RW		

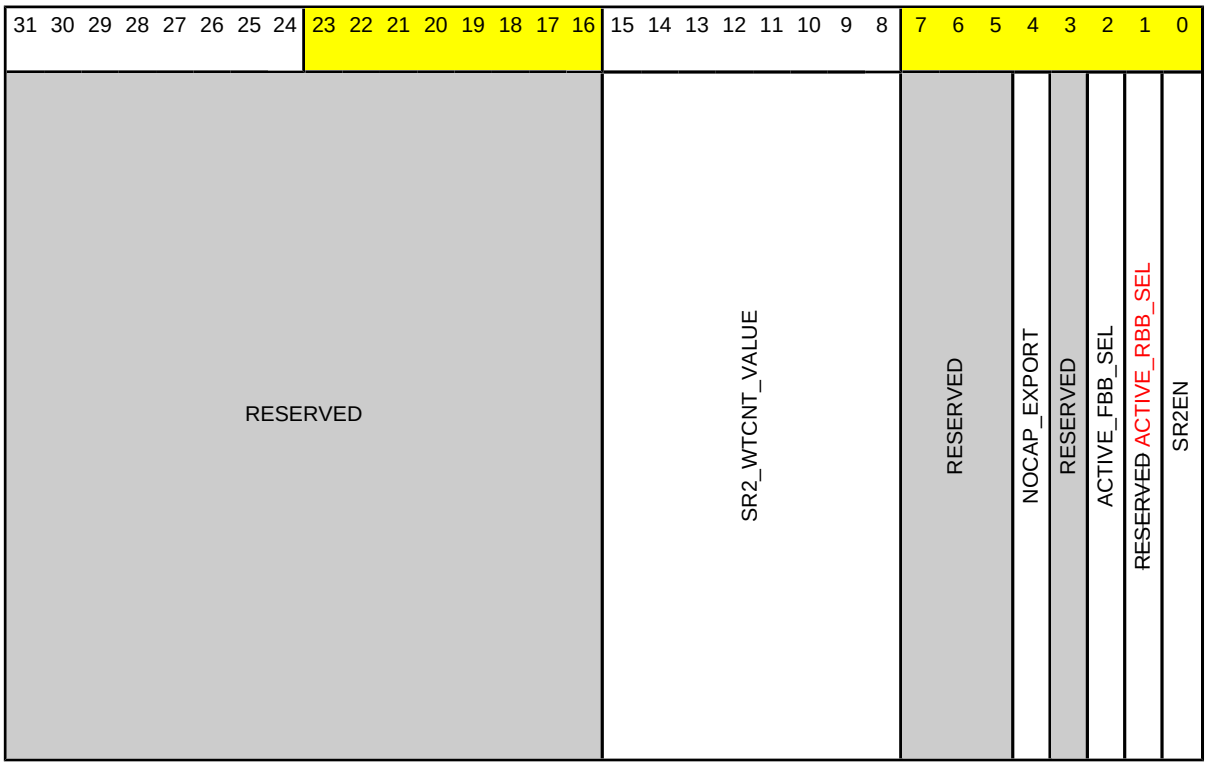


Bits	Field Name	Description	Type	Reset
31:7	RESERVED		R	0x0000
6	SR2_IN_TRANSITION	Indicates VBBLDO_CON is or is not in transition state. This output should be used by programming interface to clear OPP_CHANGE bit as an indication of OPP change completion. Read 0x0: Read 0x1: Indicates that VBBLDO_CON is in transition and SR2_STATUS bits are not stable to read.	R	0
5	RESERVED		R	0

Bits	Field Name	Description	Type	Reset
4:3	SR2_STATUS	Indicate ABB LDO current operation status Read 0x0: ABB LDO is placed in bypass mode. Read 0x1:~~Reserved~~ABB LDO is placed in ABB Set 2 active mode Read 0x2: ABB LDO is placed in ABB Set1 active mode. Read 0x3: Reserved	R	0x0
2	OPP_CHANGE	When OPP_CHANGE is set to 1, VBBLDO_CON samples OPP_SEL ACTIVE_FBB_SEL/ ACTIVE_RBB_SELupon detecting rising edge. VBBLDO_CON asserts signal SR2_IN_TRANSITION in response to OPP_CHANGE. OPP_CHANGE should be cleared to 0 when SR2_IN_TRANSITION from VBBLDO_CON is de-asserted.	RW W Special	0
1:0	OPP_SEL	Selects the OPP at which the MPU voltage domain is operating 0x0: default : Nominal 0x1: Fast OPP 0x2: Nominal 0x3: Slow OPP	RW	0

Table 3.29. PRM_LDO_ABB_IVA_SETUP

Address Offset	0x0000 00D8		
Physical Address	0x4A30 7BD8	**Instance**	DEVICE_PRM
Description	Selects the IVA_ABB LDO mode.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000

Bits	Field Name	Description	Type	Reset
15:8	SR2_WTCNT_VALUE	LDO settling time for active-mode OPP change. Counting at a 16 system clock cycles rate. Target is 50us. [warm reset insensitive]	RW	0x00
7:5	RESERVED		R	0x0
4	NOCAP_EXPORT	Defines whether ABB LDO is cap-less or not. After PowerOn reset and Efuse sensing, this bit field is automatically loaded with an Efuse value from control module. Bit field remains writable after this. [warm reset insensitive] 0x0: ABB LDO uses an external cap 0x1: ABB LDO does not use an external cap	RW W Special	0
3	RESERVED	Reserved	RW	0
2	ACTIVE_FBB_SEL	Defines ABB LDO mode when voltage is in slow fast OPP. [warm reset insensitive] 0x0: ABB LDO is in bypass mode 0x1: ABB LDO is in ABB Set1 mode	RW	0
1	~~RESERVED~~ACTIVE_RBB_SEL	~~Reserved~~Defines ABB LDO mode when IVA voltage is in OPP_TURBO. [warm reset insensitive] 0x0: ABB LDO is in bypass mode 0x1: ABB LDO is in ABB Set2 mode	RW	0
0	SR2EN	Enable ABB power management 0x0: ABB LDO is put in bypass mode 0x1: ABB LDO will operate accordingly to settings	RW	0

Table 3.30. PRM_LDO_ABB_IVA_CTRL

Address Offset	0x0000 00DC		
Physical Address	0x4A30 7BDC	**Instance**	DEVICE_PRM
Description	Control and Status of ABB on IVA voltage domain. [warm reset insensitive]		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								SR2_IN_TRANSITION	RESERVED	SR2_STATUS			OPP_CHANGE	OPP_SEL	

Bits	Field Name	Description	Type	Reset
31:7	RESERVED		R	0x0000
6	SR2_IN_TRANSITION	Indicates VBBLDO_CON is or is not in transition state. This output should be used by programming interface to clear OPP_CHANGE bit as an indication of OPP change completion. Read 0x0: Read 0x1: Indicates that VBBLDO_CON is in transition and SR2_STATUS bits are not stable to read.	R	0
5	RESERVED		R	0
4:3	SR2_STATUS	Indicate ABB LDO current operation status Read 0x0: ABB LDO is placed in bypass mode.	R	0x0

Bits	Field Name	Description	Type	Reset
		Read 0x1:~~Reserved~~ABB LDO is placed in ABB Set 2 active mode Read 0x2: ABB LDO is placed in ABB Set1 active mode. Read 0x3: Reserved		
2	OPP_CHANGE	When OPP_CHANGE is set to 1, VBBLDO_CON samples OPP_SEL ACTIVE_FBB_SEL/ ACTIVE_RBB_SELupon detecting rising edge. VBBLDO_CON asserts signal SR2_IN_TRANSITION in response to OPP_CHANGE. OPP_CHANGE should be cleared to 0 when SR2_IN_TRANSITION from VBBLDO_CON is de-asserted.	RW W Special	0
1:0	OPP_SEL	Selects the OPP at which the MPU voltage domain is operating 0x0: default : Nominal 0x1: Fast OPP 0x2: Nominal 0x3: Slow OPP	RW	0

Table 3.31. PRM_DEVICE_OFF_CTRL

Address Offset	0x0000 00E4		
Physical Address	Please refer toTable 3.26	**Instance**	DEVICE_PRM
Description	This register is used to control device OFF transition.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						~~RESERVED~~ EMIF2_OFFWKUP_DISABLE	~~RESERVED~~ EMIF1_OFFWKUP_DISABLE	RESERVED							DEVICE_OFF_ENABLE

Bits	Field Name	Description	Type	Reset
31:10	RESERVED		R	0x0000000~~0~~
9	EMIF2_OFFWKUP_DISABLE	Controls the EMIF2_DEVICE_OFFWKUP_CO RESRTACTST notifier sent to EMIF2 upon a dev ice wakeup from OFF mode. [warm reset insensitive] 0x0: Notifier is activated 0x1: Notifier is not activated - stays low	RW	0
8	EMIF1_OFFWKUP_DISABLE	Controls the EMIF1_DEVICE_OFFWKUP_CO RESRTACTST notifier sent to EMIF1 upon a dev ice wakeup from OFF mode. [warm reset insensitive] 0x0: Notifier is activated	RW	0

Bits	Field Name	Description	Type	Reset
		0x1: Notifier is not activated - stays low		
7:1	RESERVED		R	0x00
0	DEVICE_OFF_ENABLE	Controls transition to device OFF mode. 0x0: Device is not allowed to perform transition to OFF mode 0x1: Device is allowed to perform transition to OFF mode as soon as all power domains in MPU, IVA and CORE voltage are in OFF or OSWRET state (open switch retention)	RW	0

3.11.20. INSTR_PRM Registers

Refer to OMAP4460 Silicon Revision 1.x TRM.

3.11.21. CM1 Instance Summary

Table 3.32. CM1 Instance Summary

Module Name	L4 Base Address	Size
INTRCONN_SOCKET_CM1	0x4A00 4000	256Bytes
CKGEN_CM1	0x4A00 4100	512Bytes
MPU_CM1	0x4A00 4300	256Bytes
DSP_CM1	0x4A00 4400	256Bytes
ABE_CM1	0x4A00 4500	256Bytes
RESTORE_CM1	0x4A00 4E00	256Bytes
INSTR_CM1	0x4A00 4F00	256Bytes

3.11.22. INTRCONN_SOCKET_CM1 Registers

Refer to OMAP4460 Silicon Revision 1.x TRM.

3.11.23. CKGEN_CM1 Registers

3.11.23.1. CKGEN_CM1 Register Summary

Table 3.33. CKGEN_CM1 Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	CKGEN_CM1 L4 Base Address
CM_CLKSEL_CORE	RW	32	0x0000 0000	0x4A00 4100
CM_CLKSEL_ABE	RW	32	0x0000 0008	0x4A00 4108
CM_DLL_CTRL	RW	32	0x0000 0010	0x4A00 4110
CM_CLK-MODE_DPLL_CORE	RW	32	0x0000 0020	0x4A00 4120
CM_IDLEST_DPLL_CORE	R	32	0x0000 0024	0x4A00 4124
CM_AUTOIDLE_DPLL_CORE	RW	32	0x0000 0028	0x4A00 4128
CM_CLKSEL_DPLL_CORE	RW	32	0x0000 002C	0x4A00 412C
CM_DIV_M2_DPLL_CORE	RW	32	0x0000 0030	0x4A00 4130
CM_DIV_M3_DPLL_CORE	RW	32	0x0000 0034	0x4A00 4134
CM_DIV_M4_DPLL_CORE	RW	32	0x0000 0038	0x4A00 4138
	RW	32	0x0000 003C	0x4A00 413C

Register Name	Type	Register Width (Bits)	Address Offset	CKGEN_CM1 L4 Base Address
CM_DIV_M5_DPLL_CORE				
CM_DIV_M6_DPLL_CORE	RW	32	0x0000 0040	0x4A00 4140
CM_DIV_M7_DPLL_CORE	RW	32	0x0000 0044	0x4A00 4144
CM_SSC_DELTAMSTEP_DPLL_CORE	RW	32	0x0000 0048	0x4A00 4148
CM_SSC_MODFREQ-DIV_DPLL_CORE	RW	32	0x0000 004C	0x4A00 414C
CM_EMU_OVERRIDE_DPLL_CORE	RW	32	0x0000 0050	0x4A00 4150
CM_CLK-MODE_DPLL_MPU	RW	32	0x0000 0060	0x4A00 4160
CM_IDLEST_DPLL_MPU	R	32	0x0000 0064	0x4A00 4164
CM_AUTOIDLE_DPLL_MPU	RW	32	0x0000 0068	0x4A00 4168
CM_CLKSEL_DPLL_MPU	RW	32	0x0000 006C	0x4A00 416C
CM_DIV_M2_DPLL_MPU	RW	32	0x0000 0070	0x4A00 4170
CM_SSC_DELTAMSTEP_DPLL_MPU	RW	32	0x0000 0088	0x4A00 4188
CM_SSC_MODFREQ-DIV_DPLL_MPU	RW	32	0x0000 008C	0x4A00 418C
CM_BYP-CLK_DPLL_MPU	RW	32	0x0000 009C	0x4A00 419C
CM_CLK-MODE_DPLL_IVA	RW	32	0x0000 00A0	0x4A00 41A0
CM_IDLEST_DPLL_IVA	R	32	0x0000 00A4	0x4A00 41A4
CM_AUTOIDLE_DPLL_IVA	RW	32	0x0000 00A8	0x4A00 41A8
CM_CLKSEL_DPLL_IVA	RW	32	0x0000 00AC	0x4A00 41AC
CM_DIV_M4_DPLL_IVA	RW	32	0x0000 00B8	0x4A00 41B8
CM_DIV_M_DPLL_IVA	RW	32	0x0000 00BC	0x4A00 41BC
CM_SSC_DELTAMSTEP_DPLL_IVA	RW	32	0x0000 00C8	0x4A00 41C8
CM_SSC_MODFREQ-DIV_DPLL_IVA	RW	32	0x0000 00CC	0x4A00 41CC
CM_BYP-CLK_DPLL_IVA	RW	32	0x0000 00DC	0x4A00 41DC
CM_CLK-MODE_DPLL_ABE	RW	32	0x0000 00E0	0x4A00 41E0
CM_IDLEST_DPLL_ABE	R	32	0x0000 00E4	0x4A00 41E4
CM_AUTOIDLE_DPLL_ABE	RW	32	0x0000 00E8	0x4A00 41E8
CM_CLKSEL_DPLL_ABE	RW	32	0x0000 00EC	0x4A00 41EC
CM_DIV_M2_DPLL_ABE	RW	32	0x0000 00F0	0x4A00 41F0
CM_DIV_M3_DPLL_ABE	RW	32	0x0000 00F4	0x4A00 41F4

Register Name	Type	Register Width (Bits)	Address Offset	CKGEN_CM1 L4 Base Address
CM_SSC_DELTA MSTEP_DPLL_ABE	RW	32	0x0000 0108	0x4A00 4208
CM_SSC_MODFREQ-DIV_DPLL_ABE	RW	32	0x0000 010C	0x4A00 420C
RESERVED	RW	32	0x0000 0120	0x4A00 4220
RESERVED	R	32	0x0000 0124	0x4A00 4224
RESERVED	RW	32	0x0000 0128	0x4A00 4228
RESERVED	RW	32	0x0000 012C	0x4A00 422C
RESERVED	RW	32	0x0000 0130	0x4A00 4230
RESERVED	RW	32	0x0000 0138	0x4A00 4238
RESERVED	RW	32	0x0000 013C	0x4A00 423C
RESERVED	RW	32	0x0000 0140	0x4A00 4240
RESERVED	RW	32	0x0000 0148	0x4A00 4248
RESERVED	RW	32	0x0000 014C	0x4A00 424C
CM_SHA-DOW_FREQ_CON-FIG1	RW	32	0x0000 0160	0x4A00 4260
CM_SHA-DOW_FREQ_CON-FIG2	RW	32	0x0000 0164	0x4A00 4264
CM_DYN_DEP_P RESCAL	RW	32	0x0000 0170	0x4A00 4270
CM_RESTORE_ST	RW	32	0x0000 0180	0x4A00 4280

3.11.23.2. CKGEN_CM1 Register Description

Note

This section contains only modified registers.

Table 3.34. CM_DIV_M4_DPLL_CORE

Address Offset	0x0000 0038		
Physical Address	See Table 3.33	**Instance**	CKGEN_CM1
Description	This register provides controls over the CLKOUT1 o/p of the HSDIVIDER.		
Type	RW		

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
RESERVED		HSDIVIDER_CLKOUT1_PWDN, RESERVED, ST_HSDIVIDER_CLKOUT1, HSDIVIDER_CLKOUT1_GATE_CTRL	RESERVED, HSDIVIDER_CLKOUT1_DIVCHACK, HSDIVIDER_CLKOUT1_DIV

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000

Bits	Field Name	Description	Type	Reset
12	HS-DIVIDER_CLKOUT1_PWDN	~~Automatic power down for HSDIVIDER M4 divider and hence CLKOUT1 output when the o/p clock is gated.~~Direct power down control for HSDIVIDER M4 divider and CLKOUT1 output. Power down should be enabled only when clock is first gated. ~~Read 0x0: Keep M4 divider powered on even when CLKOUT1 is gated.~~ 0x0: Divider is powered up 0x1: Divider is powered down	RW	0
11:10	RESERVED		R	0x0
9	ST_HSDIVIDER_CLKOUT1	HSDIVIDER CLKOUT1 status Read 0x0: The clock output is gated Read 0x1: The clock output is enabled	R	0
8	HSDIVIDER_CLKOUT1_GATE_CTRL	Control gating of HSDIVIDER CLKOUT1 0x0: Automatically gate this clock when there is no dependency for it 0x1: Force this clock to stay enabled even if there is no request	RW	0
7:6	RESERVED		R	0x0
5	HSDIVIDER_CLKOUT1_DIVCHACK	Toggle on this status bit after changing HSDIVIDER_CLKOUT1_DIV indicates that the change in divider value has taken effect	R	0
4:0	HSDIVIDER_CLKOUT1_DIV	DPLL (M4+1) post-divider factor (1 to 31). 0x0: Reserved	RW	0x04

Table 3.35. Register Call Summary for Register CM_DIV_M4_DPLL_CORE

Power Management Functional Description
• Power Management Functional Description:[0]
PRCM Register Manual
• RESTORE_CM1 Register Description:[1]

Table 3.36. CM_DIV_M5_DPLL_CORE

Address Offset	0x0000 003C		
Physical Address	See Table 3.33	**Instance**	CKGEN_CM1
Description	This register provides controls over the CLKOUT2 o/p of the HSDIVIDER.		
Type	RW		

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
RESERVED			

15	14	13	12	11	10	9	8
HSDIVIDER_CLKOUT2_PWDN	RESERVED	ST_HSDIVIDER_CLKOUT2	HSDIVIDER_CLKOUT2_GATE_CTRL				

7	6	5	4	3	2	1	0
RESERVED		HSDIVIDER_CLKOUT2_DIVCHACK	HSDIVIDER_CLKOUT2_DIV				

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12	HS-DIVIDER_CLKOUT2_PWDN	~~Automatic power down for HSDIVIDER M5 divider and hence CLKOUT2 output when the o/p clock is gated.~~Direct power down control for HSDIVIDER M5 divider and CLKOUT2 output. Power down should be enabled only when clock is first gated. ~~Read 0x0: Keep M5 divider powered on even when CLKOUT2 is gated.~~ 0x0: Divider is powered up 0x1: Divider is powered down	RW	0
11:10	RESERVED		R	0x0
9	ST_HSDIVIDER_CLKOUT2	HSDIVIDER CLKOUT2 status Read 0x0: The clock output is gated Read 0x1: The clock output is enabled	R	0
8	HSDIVIDER_CLKOUT2 _GATE_CTRL	Control gating of HSDIVIDER CLKOUT2 0x0: Automatically gate this clock when there is no dependency for it 0x1: Force this clock to stay enabled even if there is no request	RW	0
7:6	RESERVED		R	0x0
5	HSDIVIDER_CLKOUT2 _DIVCHACK	Toggle on this status bit after changing HSDIVIDER_CLKOUT2_DIV indicates that the change in divider value has taken effect	R	0
4:0	HSDIVIDER_CLKOUT2_DIV	DPLL (M5+1) post-divider factor (1 to 31). 0x0: Reserved	RW	0x04

Table 3.37. Register Call Summary for Register CM_DIV_M5_DPLL_CORE

Power Management Functional Description
• Power Management Functional Description:[0]
PRCM Register Manual
• RESTORE_CM1 Register Description:[1]

Table 3.38. CM_DIV_M6_DPLL_CORE

Address Offset	0x0000 0040		
Physical Address	See Table 3.33	**Instance**	CKGEN_CM1
Description	This register provides controls over the CLKOUT3 o/p of the HSDIVIDER.		
Type	RW		

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
RESERVED		HSDIVIDER_CLKOUT3_PWDN, RESERVED, ST_HSDIVIDER_CLKOUT3, HSDIVIDER_CLKOUT3_GATE_CTRL	RESERVED, HSDIVIDER_CLKOUT3_DIVCHACK, HSDIVIDER_CLKOUT3_DIV

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12	HS-DIVIDER_CLKOUT3_PWDN	~~Automatic power down for HSDIVIDER M6 divider and hence CLKOUT3 output when the o/p clock is gated.~~Direct power down control for HSDIVIDER M6 divider and CLKOUT3 output. Power down should be enabled only when clock is first gated. ~~Read 0x0: Keep M6 divider powered on even when CLKOUT3 is gated.~~ 0x0: Divider is powered up 0x1: Divider is powered down	RW	0
11:10	RESERVED		R	0x0
9	ST_HSDIVIDER_CLKOUT3	HSDIVIDER CLKOUT3 status Read 0x0: The clock output is gated Read 0x1: The clock output is enabled	R	0
8	HSDIVIDER_CLKOUT3 _GATE_CTRL	Control gating of HSDIVIDER CLKOUT3 0x0: Automatically gate this clock when there is no dependency for it 0x1: Force this clock to stay enabled even if there is no request	RW	0
7:6	RESERVED		R	0x0
5	HSDIVIDER_CLKOUT3 _DIVCHACK	Toggle on this status bit after changing HSDIVIDER_CLKOUT3_DIV indicates that the change in divider value has taken effect	R	0
4:0	HSDIVIDER_CLKOUT3_DIV	DPLL (M6+1) post-divider factor (1 to 31). 0x0: Reserved	RW	0x08

Table 3.39. Register Call Summary for Register CM_DIV_M6_DPLL_CORE

Power Management Functional Description
• Power Management Functional Description:[0]
PRCM Register Manual
• RESTORE_CM1 Register Description:[1]

Table 3.40. CM_DIV_M7_DPLL_CORE

Address Offset	0x0000 0044		
Physical Address	See Table 3.33	**Instance**	CKGEN_CM1
Description	This register provides controls over the CLKOUT4 o/p of the HSDIVIDER.		
Type	RW		

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
RESERVED			

15	14	13	12	11	10	9	8
HSDIVIDER_CLKOUT4_PWDN	RESERVED	ST_HSDIVIDER_CLKOUT4	HSDIVIDER_CLKOUT4_GATE_CTRL				

7	6	5	4	3	2	1	0
RESERVED		HSDIVIDER_CLKOUT4_DIVCHACK	HSDIVIDER_CLKOUT4_DIV				

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12	HS-DIVIDER_CLKOUT4_PWDN	~~Automatic power down for HSDIVIDER M7 divider and hence CLKOUT4 output when the o/p clock is gated.~~Direct power down control for HSDIVIDER M7 divider and CLKOUT4 output. Power down should be enabled only when clock is first gated. ~~Read 0x0: Keep M7 divider powered on even when CLKOUT4 is gated.~~ 0x0: Divider is powered up 0x1: Divider is powered down	RW	0
11:10	RESERVED		R	0x0
9	ST_HSDIVIDER_CLKOUT4	HSDIVIDER CLKOUT4 status Read 0x0: The clock output is gated Read 0x1: The clock output is enabled	R	0
8	HSDIVIDER_CLKOUT4 _GATE_CTRL	Control gating of HSDIVIDER CLKOUT4 0x0: Automatically gate this clock when there is no dependency for it 0x1: Force this clock to stay enabled even if there is no request	RW	0
7:6	RESERVED		R	0x0
5	HSDIVIDER_CLKOUT4 _DIVCHACK	Toggle on this status bit after changing HSDIVIDER_CLKOUT4_DIV indicates that the change in divider value has taken effect[1]	R	0
4:0	HSDIVIDER_CLKOUT4_DIV	DPLL (M7+1) post-divider factor (1 to 31). 0x0: Reserved	RW	0x04

1. It is toggled only if the programmed divider value differs from the previous one.

Table 3.41. Register Call Summary for Register CM_DIV_M7_DPLL_CORE

Power Management Functional Description

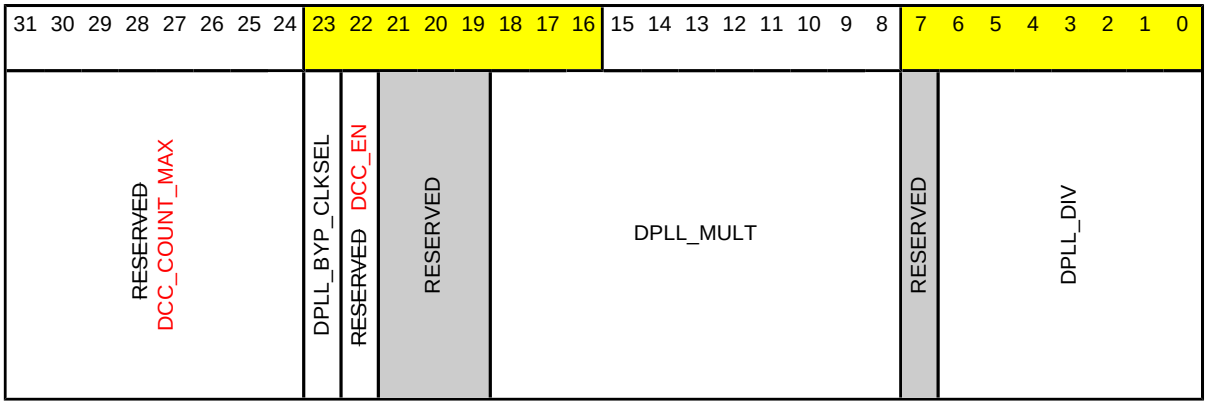
- Power Management Functional Description:[0]

PRCM Register Manual

- RESTORE_CM1 Register Description:[1]

Table 3.42. CM_CLKSEL_DPLL_MPU

Address Offset	0x0000 006C		
Physical Address	SeeTable 3.33	**Instance**	CKGEN_CM1
Description	This register provides controls over the DPLL.		
Type	RW		



Bits	Field Name	Description	Type	Reset
~~31:24~~	~~RESERVED~~	-	R	~~0x00~~

Bits	Field Name	Description	Type	Reset
31:24	DCC_COUNT_MAX	The value "NbCycles" set in this field determines the duration of the clock ramp step during which output frequency is Fdpll/(2*M2). The duration is computed as 32 x NbCycles of L4 clock cycles (100MHz). Duration should be > 1.5us to allow enough time for DCC to lock. This bit-field is only relevant when DCC_EN=1.	RW	0x05
23	DPLL_BYP_CLKSEL	Only CLKINPULOW bypass clock supported for this PLL	R Rreturns1s	1
22	DCC_EN	Enable or disable Duty Cycle Correction. Must be enabled only for frequency > 1GHz. When enabled, the CLKOUTHIF output of the DPLL is used after duty cycle correction instead of CLKOUT. M3 divider is hard-wired to 1 so the lock frequency Fdpll is directly provided to MPU. 0x1: DCC disabled 0x1: DCC enabled	RW	0
~~22~~21:19	RESERVED		R	0x0
18:8	DPLL_MULT	DPLL multiplier factor (2 to 2047). This register is automatically cleared to 0 when the DPLL_EN field in the *CLKMODE_DPLL* register is set to select MN Bypass mode. (equal to input M of DPLL; M=2 to 2047 => DPLL multiplies by M). 0x0: Reserved 0x1: Reserved	RW	0x000
7	RESERVED		R	0
6:0	DPLL_DIV	DPLL divider factor (0 to 127) (equal to input N of DPLL; actual division factor is N+1).	RW	0x00

Table 3.43. Register Call Summary for Register CM_CLKSEL_DPLL_MPU

Clock Management Functional Description
• Clock Management Functional Description:[0]

Table 3.44. CM_DIV_M4_DPLL_IVA

Address Offset	0x0000 00B8		
Physical Address	SeeTable 3.33	**Instance**	CKGEN_CM1
Description	This register provides controls over the CLKOUT1 o/p of the HSDIVIDER.		
Type	RW		

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
RESERVED		HSDIVIDER_CLKOUT1_PWDN, RESERVED, ST_HSDIVIDER_CLKOUT1, HSDIVIDER_CLKOUT1_GATE_CTRL	RESERVED, HSDIVIDER_CLKOUT1_DIVCHACK, HSDIVIDER_CLKOUT1_DIV

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12	HS-DIVIDER_CLKOUT1_PWDN	~~Automatic power down for HSDIVIDER M4 divider and hence CLKOUT1 output when the o/p clock is gated.~~Direct power down control for HSDIVIDER M4 divider and CLKOUT1 output. Power down should be enabled only when clock is first gated. ~~Read 0x0: Keep M4 divider powered on even when CLKOUT1 is gated.~~ 0x0: Divider is powered up 0x1: Divider is powered down	RW	0
11:10	RESERVED		R	0x0
9	ST_HSDIVIDER_CLKOUT1	HSDIVIDER CLKOUT1 status Read 0x0: The clock output is gated Read 0x1: The clock output is enabled	R	0
8	HSDIVIDER_CLKOUT1 _GATE_CTRL	Control gating of HSDIVIDER CLKOUT1 0x0: Automatically gate this clock when there is no dependency for it 0x1: Force this clock to stay enabled even if there is no request	RW	0
7:6	RESERVED		R	0x0
5	HSDIVIDER_CLKOUT1 _DIVCHACK	Toggle on this status bit after changing HSDIVIDER_CLKOUT1_DIV indicates that the change in divider value has taken effect	R	0
4:0	HSDIVIDER_CLKOUT1_DIV	DPLL (M4+1) post-divider factor (1 to 31). 0x00: Reserved	RW	0x04

Table 3.45. Register Call Summary for Register CM_DIV_M4_DPLL_IVA

Power Management Functional Description

- Power Management Functional Description:[0]

Table 3.46. CM_CLKMODE_DPLL_IVA

Address Offset	0x0000 00A0		
Physical Address	SeeTable 3.33	**Instance**	CKGEN_CM1
Description	This register allows controlling the DPLL modes		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																DPLL_SSC_DOWNSPREAD	DPLL_SSC_ACK	DPLL_SSC_EN	DPLL_REGM4XEN	DPLL_LPMODE_EN	DPLL_RELOCK_RAMP_EN	DPLL_DRIFTGUARD_EN	DPLL_RAMP_RATE			DPLL_RAMP_LEVEL			DPLL_EN	

Bits	Field Name	Description	Type	Reset
31:15	RESERVED		R	0x00000
14	DPLL_SSC_DOWNSPREAD	Control if only low frequency spread is required 0x0: When SSC is enabled, clock frequency is spr ead on both sides of the programmed frequency	RW	0

Bits	Field Name	Description	Type	Reset
		0x1: When SSC is enabled, clock frequency is spread only on the lower side of the programmed frequency		
13	DPLL_SSC_ACK	Acknowledgement from the DPLL regarding start and stop of Spread Spectrum Clocking feature Read 0x0: SSC has been turned off on PLL o/ps Read 0x1: SSC has been turned on on PLL o/ps	R	0
12	DPLL_SSC_EN	Enable or disable Spread Spectrum Clocking 0x0: SSC disabled 0x1: SSC enabled	RW	0
11	DPLL_REGM4XEN	Enable the REGM4XEN mode of the DPLL. Please check the DPLL documentation to check when this mode can be enabled. Read 0x0: REGM4XEN mode of the DPLL is disab led	R	0
10	DPLL_LPMODE_EN	Set the DPLL in low-power mode. Check the DPLL documentation to see when this can be enabled. 0x0: Low-power mode of the DPLL is disabled 0x1: Low-power mode of the DPLL is enabled	RW	0
9	DPLL_RELOCK_RAMP_EN	If enabled, the clock ramping feature is used applie d during the lock process, as well as the relock pro cess. If disabled, the clock ramping feature is used only during the first lock.	RW	0
8	DPLL_DRIFTGUARD_EN	This bit allows to enable or disable the automatic recalibration feature of the DPLL. The DPLL will automatically start a recalibration process upon assertion of the DPLL's RECAL flag if this bit is set. 0x0: DRIFTGUARD feature is disabled 0x1: DRIFTGUARD feature is enabled	RW	0
7:5	DPLL_RAMP_RATE	Selects the time in terms of DPLL REFCLKs spent at each stage of the clock ramping process 0x0: 2 REFCLKs 0x1: 4 REFCLKs 0x2: 8 REFCLKs 0x3: 16 REFCLKs 0x4: 32 REFCLKs 0x5: 64 REFCLKs 0x6: 128 REFCLKs 0x7: 512 REFCLKs	RW	0x0
4:3	DPLL_RAMP_LEVEL	The DPLL provides an output clock frequency ramping feature when switching from bypass clock to normal clock during lock and re-lock. The frequency ramping will happen in a maximum of 4 steps in frequency before the DPLL's frequen- cy lock indicator is asserted. This register is used to enable/disable the DPLL ramping feature. If enabled, it is also used to select the algorithm used for clock ramping 0x0: CLKOUT = No ramping CLKOUTX2 = No r amping 0x1: CLKOUT = Bypass clk - Fout/8 - Fout/4 - Fout/ 2 - Fout CLKOUTX2 = Bypass clk - Foutx2/8 - Foutx2/4 - Foutx2/2 - Foutx2 0x2: CLKOUT = Bypass clk - Fout/4 - Fout/2 - Fout/ 1.5 - Fout CLKOUTX2 = Bypass clk - Foutx2/4 - Foutx2/2 - Foutx2/1.5 - Foutx2 0x3: Reserved	RW	0x0
2:0	DPLL_EN	DPLL control. Upon Warm Reset, the PRCM DPLL control state machine updates this register to re- flect MN bypass mode. 0x0: Reserved 0x1: Reserved 0x2: Reserved 0x3: Reserved	RW	0x4

Bits	Field Name	Description	Type	Reset
		0x4: Put the DPLL in MN bypass mode. The DPLL_MULT register bits are reset to 0 automatically by putting the DPLL in this mode. 0x5:Put the DPLL in idle bypass low-power mode. 0x6:~~Put the DPLL in idle bypass fast-relock mode.~~ Reserved 0x7: Enables the DPLL in lock mode		

Table 3.47. Register Call Summary for Register CM_CLKMODE_DPLL_IVA

Power Management Functional Description

- Power Management Functional Description:[0]

Table 3.48. CM_DIV_M5_DPLL_IVA

Address Offset	0x0000 00BC		
Physical Address	SeeTable 3.33	**Instance**	CKGEN_CM1
Description	This register provides controls over the CLKOUT2 o/p of the HSDIVIDER.		
Type	RW		

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
RESERVED		HSDIVIDER_CLKOUT2_PWDN, RESERVED, ST_HSDIVIDER_CLKOUT2, HSDIVIDER_CLKOUT2_GATE_CTRL	RESERVED, HSDIVIDER_CLKOUT2_DIVCHACK, HSDIVIDER_CLKOUT2_DIV

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12	HS-DIVIDER_CLKOUT2_PWDN	~~Automatic power down for HSDIVIDER M5 divider and hence CLKOUT2 output when the o/p clock is gated.~~Direct power down control for HSDIVIDER M5 divider and CLKOUT2 output. Power down should be enabled only when clock is first gated. ~~Read 0x0: Keep M5 divider powered on even when CLKOUT5 is gated.~~ 0x0: Divider is powered up 0x1: Divider is powered down	RW	0
11:10	RESERVED		R	0x0
9	ST_HSDIVIDER_CLKOUT2	HSDIVIDER CLKOUT2 status Read 0x0: The clock output is gated Read 0x1: The clock output is enabled	R	0
8	HSDIVIDER_CLKOUT2 _GATE_CTRL	Control gating of HSDIVIDER CLKOUT2 0x0: Automatically gate this clock when there is no dependency for it 0x1: Force this clock to stay enabled even if there is no request	RW	0

Bits	Field Name	Description	Type	Reset
7:6	RESERVED		R	0x0
5	HSDIVIDER_CLKOUT2_DIVCHACK	Toggle on this status bit after changing HSDIVIDER_CLKOUT2_DIV indicates that the change in divider value has taken effect	R	0
4:0	HSDIVIDER_CLKOUT2_DIV	DPLL (M5+1) post-divider factor (1 to 31). 0x00: Reserved	RW	0x04

3.11.24. MPU_CM1 Registers

3.11.24.1. MPU_CM1 Register Summary

Table 3.49. MPU_CM1 Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	MPU_CM1 L4 Base Address
CM_MPU_CLKSTCTRL	RW	32	0x0000 0000	0x4A00 4300
CM_MPU_STATICDEP	RW	32	0x0000 0004	0x4A00 4304
CM_MPU_DYNAMICDEP	RW	32	0x0000 0008	0x4A00 4308
CM_MPU_MPU_CLKCTRL	R	32	0x0000 0020	0x4A00 4320

3.11.24.2. MPU_CM1 Register Description

Note

This section contains only modified registers.

Table 3.50. CM_MPU_MPU_CLKCTRL

Address Offset	0x0000 0020		
Physical Address	SeeTable 3.49	**Instance**	MPU_CM1
Description	This register manages the MPU clocks.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								RESERVED	CLKSEL_ABE_DIV_MODE	RESERVED	CLKSEL_EMIF_DIV_MODE	RESERVED				STBYST	IDLEST	RESERVED												MODULEMODE	

Bits	Field Name	Description	Type	Reset
31:~~19~~26	RESERVED		R	0x0000
25	CLKSEL_ABE_DIV_MODE	Selects the ratio for MPU->ABE async bridge versus MPU DPLL clock.	R	0

Bits	Field Name	Description	Type	Reset
		Read 0x0: MPU DPLL clock divided by 4 Read 0x1: MPU DPLL clock divided by 8		
24	CLKSEL_EMIF_DIV_MODE	Selects the ratio for memory adapter clock (MA_EOCP_ICLK) versus MPU DPLL clock. Read 0x0: MPU DPLL clock divided by 2 Read 0x1: MPU DPLL clock divided by 4	R	0
23:19	RESERVED		R	0x00
18	STBYST	Module standby status. [warm reset insensitive] Read 0x0: Module is functional (not in standby) Read 0x1: Module is in standby	R	1
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including IN-TRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion Read 0x2: Module is in Idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be acces sed	R	0x3
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. Read 0x1: Module is managed automatically by HW according to clock domain transition. A clock domain sleep transition put module into idle. A wakeup domain transition put it back into function. Module clocks may be gated according to the clock domain state.	R Rr eturns	0x1

Table 3.51. Register Call Summary for Register CM_MPU_MPU_CLKCTRL

Clock Management Functional Description

- Clock Management Functional Description:[0]

3.11.25. DSP_CM1 Registers

Refer to OMAP4460 Silicon Revision 1.x TRM.

3.11.26. ABE_CM1 Registers

3.11.26.1. ABE_CM1 Register Summary

Table 3.52. ABE_CM1 Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	ABE_CM1 L4 Base Address
CM1_ABE_CLKSTC-TRL	RW	32	0x0000 0000	0x4A00 4500
CM1_ABE_L4ABE_CLKC-TRL	R	32	0x0000 0020	0x4A00 4520
CM1_ABE_AESS_CLK CTRL	RW	32	0x0000 0028	0x4A00 4528
CM1_ABE_PDM_CLKC TRL	RW	32	0x0000 0030	0x4A00 4530
CM1_ABE_DMIC_CLK CTRL	RW	32	0x0000 0038	0x4A00 4538

Register Name	Type	Register Width (Bits)	Address Offset	ABE_CM1 L4 Base Address
CM1_ABE_MCASP_CLKC-TRL	RW	32	0x0000 0040	0x4A00 4540
CM1_ABE_MCBSP1_CLKCTRL	RW	32	0x0000 0048	0x4A00 4548
CM1_ABE_MCBSP2_CLKCTRL	RW	32	0x0000 0050	0x4A00 4550
CM1_ABE_MCBSP3_CLKCTRL	RW	32	0x0000 0058	0x4A00 4558
CM1_ABE_SLIMBUS_CLKCTRL	RW	32	0x0000 0060	0x4A00 4560
CM1_ABE_GP-TIMER5_CLKCTRL	RW	32	0x0000 0068	0x4A00 4568
CM1_ABE_GP-TIMER6_CLKCTRL	RW	32	0x0000 0070	0x4A00 4570
CM1_ABE_GP-TIMER7_CLKCTRL	RW	32	0x0000 0078	0x4A00 4578
CM1_ABE_GP-TIMER8_CLKCTRL	RW	32	0x0000 0080	0x4A00 4580
CM1_ABE_WDTIMER3_CLKCTRL	RW	32	0x0000 0088	0x4A00 4588

3.11.26.2. ABE_CM1 Register Description

Note

This section contains only modified registers.

Table 3.53. CM1_ABE_GPTIMER5_CLKCTRL

Address Offset	0x0000 0068		
Physical Address	See Table 3.52	**Instance**	ABE_CM1
Description	This register manages the TIMER5 clocks.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								CLKSEL	RESERVED							IDLEST	RESERVED														MODULE-MODE

Bits	Field Name	Description	Type	Reset
31:25	RESERVED		R	0x00
24	CLKSEL	Selects between ABE_SYSCLK and ABE_ALWON_32K_CLK as the timer functional clock 0x0: Selects ABE_SYSCLK as the functional clock 0x1: Selects ABE_ALWON_32K_CLK as the functional clock	RW	0
23:18	RESERVED		R	0x00
17:16	IDLEST	Module idle status. [warm reset insensitive] Read 0x0: Module is fully functional, including INTRCONN Read 0x1: Module is performing transition: wakeup, or sleep, or sleep abortion	R	0x3

Bits	Field Name	Description	Type	Reset
		Read 0x2: Module is in Idle mode (only INTRCONN part). It is functional if using separate functional clock Read 0x3: Module is disabled and cannot be acces sed		
15:2	RESERVED		R	0x0000
1:0	MODULEMODE	Control the way mandatory clocks are managed. 0x0: Module is disable by SW. Any INTRCONN access to module results in an error, except if resulting from a module wakeup (asynchronous wakeup). Read 0x1: Reserved 0x2: Module is explicitly enabled. Interface clock (if not used for functions) may be gated according to the clock domain state. Functional clocks are guarantied to stay present. As long as in this configuration, power domain sleep transition can- not happen. Read 0x3: Reserved	RW	0x0

Table 3.54. Register Call Summary for Register CM1_ABE_GPTIMER5_CLKCTRL

Reset Management Functional Description

- Reset Management Functional Description:[0]

3.11.27. RESTORE_CM1 Registers

3.11.27.1. RESTORE_CM1 Register Summary

Table 3.55. RESTORE_CM1 Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	RESTORE_CM1 L4 Base Address
CM_CLKSEL_CORE_RES- TORE	RW	32	0x0000 0000	0x4A00 4E00
CM_DIV_M2_DPLL_C ORE_RESTORE	RW	32	0x0000 0004	0x4A00 4E04
CM_DIV_M3_DPLL_C ORE_RESTORE	RW	32	0x0000 0008	0x4A00 4E08
CM_DIV_M4_DPLL_C ORE_RESTORE	RW	32	0x0000 000C	0x4A00 4E0C
CM_DIV_M5_DPLL_C ORE_RESTORE	RW	32	0x0000 0010	0x4A00 4E10
CM_DIV_M6_DPLL_C ORE_RESTORE	RW	32	0x0000 0014	0x4A00 4E14
CM_DIV_M7_DPLL_C ORE_RESTORE	RW	32	0x0000 0018	0x4A00 4E18
CM_CLKSEL_DPLL_C ORE_RESTORE	RW	32	0x0000 001C	0x4A00 4E1C
CM_SSC_DELTA MSTEP_DPLL _CORE_RESTORE	RW	32	0x0000 0020	0x4A00 4E20
CM_SSC_MODFREQ- DIV_DPLL _CORE_RESTORE	RW	32	0x0000 0024	0x4A00 4E24
CM_CLKMODE_DPLL_CORE_RESTORE	RW	32	0x0000 0028	0x4A00 4E28
CM_SHA- DOW_FREQ_CON- FIG2_RESTORE	RW	32	0x0000 002C	0x4A00 4E2C

Register Name	Type	Register Width (Bits)	Address Offset	RESTORE_CM1 L4 Base Address
CM_SHA-DOW_FREQ_CON-FIG1_RESTORE	RW	32	0x0000 0030	0x4A00 4E30
CM_AUTOIDLE_DPLL _CORE_RESTORE	RW	32	0x0000 0034	0x4A00 4E34
CM_MPU_CLKST CTRL_RESTORE	RW	32	0x0000 0038	0x4A00 4E38
CM_CM1_PROFILING _CLKCTRL_RESTORE	RW	32	0x0000 003C	0x4A00 4E3C
CM_DYN_DEP_PRESCAL_RES-TORE	RW	32	0x0000 0040	0x4A00 4E40
RESERVED	RW	32	0x0000 0044	0x4A00 4E44
RESERVED	RW	32	0x0000 0048	0x4A00 4E48
RESERVED	RW	32	0x0000 004C	0x4A00 4E4C
RESERVED	RW	32	0x0000 0050	0x4A00 4E50
RESERVED	RW	32	0x0000 0054	0x4A00 4E54
RESERVED	RW	32	0x0000 0058	0x4A00 4E58

3.11.27.2. RESTORE_CM1 Register Description

Note

This section contains only modified registers.

Table 3.56. CM_DIV_M4_DPLL_CORE_RESTORE

Address Offset	0x0000 000C		
Physical Address	SeeTable 3.55	**Instance**	RESTORE_CM1
Description	Second address map for registerCM_DIV_M4_DPLL_CORE. Used only by automatic restore upon wakeup from device OFF mode.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																			HSDIVIDER_CLKOUT1_PWDN	RESERVED		ST_HSDIVIDER_CLKOUT1	HSDIVIDER_CLKOUT1_GATE_CTRL	RESERVED					HSDIVIDER_CLKOUT1_DIVCHACK	HSDIVIDER_CLKOUT1_DIV								

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12	HS-DIVIDER_CLKOUT1_PWDN	~~Automatic power down for HSDIVIDER M4 divider and hence CLKOUT1 output when the o/p clock is gated.~~Direct power down control for HSDIVIDER M4 divider and CLKOUT1 output. Power down should be enabled only when clock is first gated.	RW	0

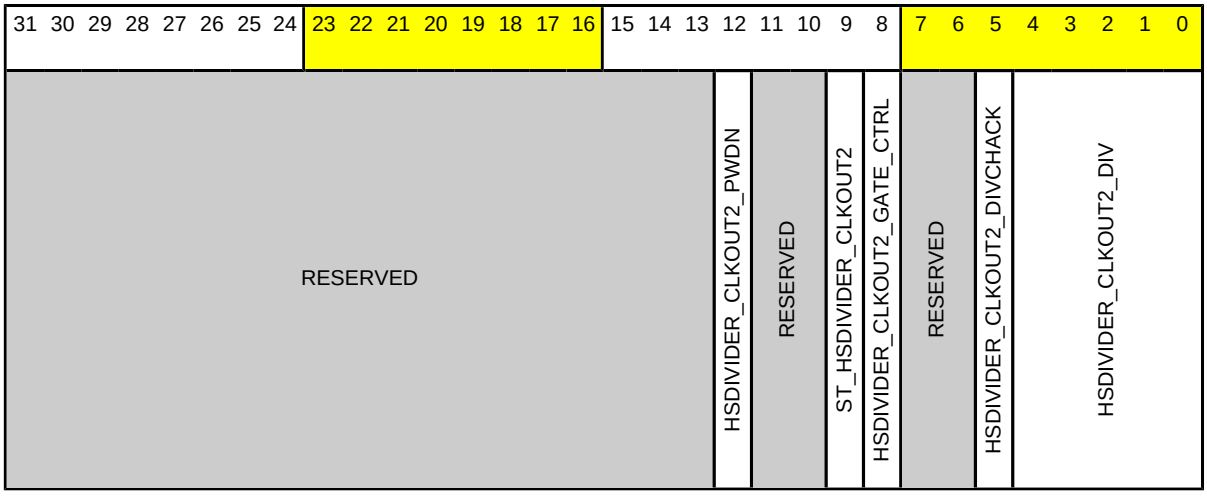
Bits	Field Name	Description	Type	Reset
		~~Read 0x0: Keep M4 divider powered on even when CLKOUT1 is gated.~~ 0x0: Divider is powered up 0x1: Divider is powered down		
11:10	RESERVED		R	0x0
9	ST_HSDIVIDER_CLKOUT1	HSDIVIDER CLKOUT1 status Read 0x0: The clock output is gated Read 0x1: The clock output is enabled	R	0
8	HSDIVIDER_CLKOUT1_GATE_CTRL	Control gating of HSDIVIDER CLKOUT1 0x0: Automatically gate this clock when there is no dependency for it 0x1: Force this clock to stay enabled even if there is no request	RW	0
7:6	RESERVED		R	0x0
5	HSDIVIDER_CLKOUT1_DIVCHACK	Toggle on this status bit after changing HSDIVIDER_CLKOUT1_DIV indicates that the change in divider value has taken effect	R	0
4:0	HSDIVIDER_CLKOUT1_DIV	DPLL (M4+1) post-divider factor (1 to 31). 0x0: Reserved	RW	0x01

Table 3.57. Register Call Summary for Register CM_DIV_M4_DPLL_CORE_RESTORE

Power Management Functional Description
• Power Management Functional Description:[0]

Table 3.58. CM_DIV_M5_DPLL_CORE_RESTORE

Address Offset	0x0000 0010		
Physical Address	See Table 3.55	**Instance**	RESTORE_CM1
Description	Second address map for register CM_DIV_M5_DPLL_CORE. Used only by automatic restore upon wakeup from device OFF mode.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12	HS-DIVIDER_CLKOUT2_PWDN	~~Automatic power down for HSDIVIDER M5 divider and hence CLKOUT2 output when the o/p clock is gated.~~Direct power down control for HSDIVIDER	RW	0

Bits	Field Name	Description	Type	Reset
		M5 divider and CLKOUT2 output. Power down should be enabled only when clock is first gated. ~~Read 0x0: Keep M5 divider powered on even when CLKOUT2 is gated.~~ 0x0: Divider is powered up 0x1: Divider is powered down		
11:10	RESERVED		R	0x0
9	ST_HSDIVIDER_CLKOUT2	HSDIVIDER CLKOUT2 status Read 0x0: The clock output is gated Read 0x1: The clock output is enabled	R	0
8	HSDIVIDER_CLKOUT2 _GATE_CTRL	Control gating of HSDIVIDER CLKOUT2 0x0: Automatically gate this clock when there is no dependency for it 0x1: Force this clock to stay enabled even if there is no request	RW	0
7:6	RESERVED		R	0x0
5	HSDIVIDER_CLKOUT2 _DIVCHACK	Toggle on this status bit after changing HSDIVIDER_CLKOUT2_DIV indicates that the change in divider value has taken effect	R	0
4:0	HSDIVIDER_CLKOUT2_DIV	DPLL (M5+1) post-divider factor (1 to 31). 0x0: Reserved	RW	0x01

Table 3.59. Register Call Summary for Register CM_DIV_M5_DPLL_CORE_RESTORE

Power Management Functional Description
• Power Management Functional Description:[0]

Table 3.60. CM_DIV_M6_DPLL_CORE_RESTORE

Address Offset	0x0000 0014		
Physical Address	See Table 3.55	**Instance**	RESTORE_CM1
Description	Second address map for register CM_DIV_M6_DPLL_CORE. Used only by automatic restore upon wakeup from device OFF mode.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								HSDIVIDER_CLKOUT3_PWDN	RESERVED	ST_HSDIVIDER_CLKOUT3	HSDIVIDER_CLKOUT3_GATE_CTRL	RESERVED						HSDIVIDER_CLKOUT3_DIVCHACK	HSDIVIDER_CLKOUT3_DIV		

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12	HS-DIVIDER_CLKOUT3_PWDN	~~Automatic power down for HSDIVIDER M6 divider and hence CLKOUT3 output when the o/p clock is~~	RW	0

Bits	Field Name	Description	Type	Reset
		~~gated.~~Direct power down control for HSDIVIDER M6 divider and CLKOUT3 output. Power down should be enabled only when clock is first gated. ~~Read 0x0: Keep M6 divider powered on even when CLKOUT3 is gated.~~ 0x0: Divider is powered up 0x1: Divider is powered down		
11:10	RESERVED		R	0x0
9	ST_HSDIVIDER_CLKOUT3	HSDIVIDER CLKOUT3 status Read 0x0: The clock output is gated Read 0x1: The clock output is enabled	R	0
8	HSDIVIDER_CLKOUT3 _GATE_CTRL	Control gating of HSDIVIDER CLKOUT3 0x0: Automatically gate this clock when there is no dependency for it 0x1: Force this clock to stay enabled even if there is no request	RW	0
7:6	RESERVED		R	0x0
5	HSDIVIDER_CLKOUT3 _DIVCHACK	Toggle on this status bit after changing HSDIVIDER_CLKOUT3_DIV indicates that the change in divider value has taken effect	R	0
4:0	HSDIVIDER_CLKOUT3_DIV	DPLL (M6+1) post-divider factor (1 to 31). 0x0: Reserved	RW	0x01

Table 3.61. Register Call Summary for Register CM_DIV_M6_DPLL_CORE_RESTORE

Power Management Functional Description
• Power Management Functional Description:[0]

Table 3.62. CM_DIV_M7_DPLL_CORE_RESTORE

Address Offset	0x0000 0018		
Physical Address	See Table 3.55	**Instance**	RESTORE_CM1
Description	Second address map for register CM_DIV_M7_DPLL_CORE. Used only by automatic restore upon wakeup from device OFF mode.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								HSDIVIDER_CLKOUT4_PWDN	RESERVED	ST_HSDIVIDER_CLKOUT4	HSDIVIDER_CLKOUT4_GATE_CTRL	RESERVED							
																										HSDIVIDER_CLKOUT4_DIVCHACK	HSDIVIDER_CLKOUT4_DIV				

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12			RW	0

Bits	Field Name	Description	Type	Reset
	HS-DIVIDER_CLKOUT4_PWDN	~~Automatic power down for HSDIVIDER M7 divider and hence CLKOUT4 output when the o/p clock is gated.~~Direct power down control for HSDIVIDER M7 divider and CLKOUT4 output. Power down should be enabled only when clock is first gated. ~~Read 0x0: Keep M7 divider powered on even when CLKOUT4 is gated.~~ 0x0: Divider is powered up 0x1: Divider is powered down		
11:10	RESERVED		R	0x0
9	ST_HSDIVIDER_CLKOUT4	HSDIVIDER CLKOUT4 status Read 0x0: The clock output is gated Read 0x1: The clock output is enabled	R	0
8	HSDIVIDER_CLKOUT4_GATE_CTRL	Control gating of HSDIVIDER CLKOUT4 0x0: Automatically gate this clock when there is no dependency for it 0x1: Force this clock to stay enabled even if there is no request	RW	0
7:6	RESERVED		R	0x0
5	HSDIVIDER_CLKOUT4_DIVCHACK	Toggle on this status bit after changing HSDIVIDER_CLKOUT4_DIV indicates that the change in divider value has taken effect	R	0
4:0	HSDIVIDER_CLKOUT4_DIV	DPLL (M7+1) post-divider factor (1 to 31). 0x0: Reserved	RW	0x01

Table 3.63. Register Call Summary for Register CM_DIV_M7_DPLL_CORE_RESTORE

Power Management Functional Description

- Power Management Functional Description:[0]

3.11.28. INSTR_CM1 Registers

Refer to OMAP4460 Silicon Revision 1.x TRM.

3.11.29. CM2 Instance Summary

Table 3.64. CM2 Instance Summary

Module Name	L4 Base Address	Size
INTRCONN_SOCKET_CM2	0x4A00 8000	256Bytes
CKGEN_CM2	0x4A00 8100	256Bytes
ALWAYS_ON_CM2	0x4A00 8600	256Bytes
CORE_CM2	0x4A00 8700	2KBytes
IVAHD_CM2	0x4A00 8F00	256Bytes
CAM_CM2	0x4A00 9000	256Bytes
DSS_CM2	0x4A00 9100	256Bytes
SGX_CM2	0x4A00 9200	256Bytes
L3INIT_CM2	0x4A00 9300	256Bytes
L4PER_CM2	0x4A00 9400	512Bytes
RESTORE_CM2	0x4A00 9E00	256Bytes
INSTR_CM2	0x4A00 9F00	256Bytes

3.11.30. INTRCONN_SOCKET_CM2 Registers

Refer to OMAP4460 Silicon Revision 1.x TRM.

3.11.31. CKGEN_CM2 Registers

3.11.31.1. CKGEN_CM2 Register Summary

Table 3.65. CKGEN_CM2 Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	CKGEN_CM2 L4 Base Address
CM_CLKSEL_MPU_M3	RW	32	0x0000 0000	0x4A00 8100
CM_CLKSEL_USB_60 MHZ	RW	32	0x0000 0004	0x4A00 8104
CM_SCALE_FCLK	RW	32	0x0000 0008	0x4A00 8108
CM_CORE_DVFS _PERF1	RW	32	0x0000 0010	0x4A00 8110
CM_CORE_DVFS _PERF2	RW	32	0x0000 0014	0x4A00 8114
CM_CORE_DVFS _PERF3	RW	32	0x0000 0018	0x4A00 8118
CM_CORE_DVFS _PERF4	RW	32	0x0000 001C	0x4A00 811C
CM_CORE_DVFS _CURRENT	RW	32	0x0000 0024	0x4A00 8124
CM_IVA_DVFS_PERF _DSP	RW	32	0x0000 0028	0x4A00 8128
CM_IVA_DVFS_PERF _IVAHD	RW	32	0x0000 002C	0x4A00 812C
CM_IVA_DVFS_PERF _ABE	RW	32	0x0000 0030	0x4A00 8130
CM_IVA_DVFS_CURR ENT	RW	32	0x0000 0038	0x4A00 8138
CM_CLK-MODE_DPLL_PER	RW	32	0x0000 0040	0x4A00 8140
CM_IDLEST_DPLL_P ER	R	32	0x0000 0044	0x4A00 8144
CM_AUTOIDLE_DPLL _PER	RW	32	0x0000 0048	0x4A00 8148
CM_CLKSEL_DPLL_P ER	RW	32	0x0000 004C	0x4A00 814C
CM_DIV_M2_DPLL_P ER	RW	32	0x0000 0050	0x4A00 8150
CM_DIV_M3_DPLL_P ER	RW	32	0x0000 0054	0x4A00 8154
CM_DIV_M4_DPLL_P ER	RW	32	0x0000 0058	0x4A00 8158
CM_DIV_M5_DPLL_P ER	RW	32	0x0000 005C	0x4A00 815C
CM_DIV_M6_DPLL_P ER	RW	32	0x0000 0060	0x4A00 8160
CM_DIV_M7_DPLL_P ER	RW	32	0x0000 0064	0x4A00 8164
CM_SSC_DELTA MSTEP_DPLL_PER	RW	32	0x0000 0068	0x4A00 8168
CM_SSC_MODFREQ-DIV_DPLL_PER	RW	32	0x0000 006C	0x4A00 816C
RESERVED	RW	32	0x0000 0070	0x4A00 8170
CM_CLK-MODE_DPLL_USB	RW	32	0x0000 0080	0x4A00 8180
	R	32	0x0000 0084	0x4A00 8184

Register Name	Type	Register Width (Bits)	Address Offset	CKGEN_CM2 L4 Base Address
CM_IDLEST_DPLL_USB				
CM_AUTOIDLE_DPLL_USB	RW	32	0x0000 0088	0x4A00 8188
CM_CLKSEL_DPLL_USB	RW	32	0x0000 008C	0x4A00 818C
CM_DIV_M2_DPLL_USB	RW	32	0x0000 0090	0x4A00 8190
CM_SSC_DELTAMSTEP_DPLL_USB	RW	32	0x0000 00A8	0x4A00 81A8
CM_SSC_MODFREQ-DIV_DPLL_USB	RW	32	0x0000 00AC	0x4A00 81AC
CM_CLKDCOL-DO_DPLL_USB	RW	32	0x0000 00B4	0x4A00 81B4
RESERVED	RW	32	0x0000 00C0	0x4A00 81C0
RESERVED	R	32	0x0000 00C4	0x4A00 81C4
RESERVED	RW	32	0x0000 00C8	0x4A00 81C8
RESERVED	RW	32	0x0000 00CC	0x4A00 81CC
RESERVED	RW	32	0x0000 00D0	0x4A00 81D0
RESERVED	RW	32	0x0000 00E8	0x4A00 81E8
RESERVED	RW	32	0x0000 00EC	0x4A00 81EC

3.11.31.2. CKGEN_CM2 Register Description

Note

This section contains only modified registers.

Table 3.66. CM_DIV_M4_DPLL_PER

Address Offset	0x0000 0058		
Physical Address	SeeTable 3.65	**Instance**	CKGEN_CM2
Description	This register provides controls over the CLKOUT1 o/p of the HSDIVIDER.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																			HSDIVIDER_CLKOUT1_PWDN	RESERVED	ST_HSDIVIDER_CLKOUT1	HSDIVIDER_CLKOUT1_GATE_CTRL	RESERVED							HSDIVIDER_CLKOUT1_DIVCHACK	HSDIVIDER_CLKOUT1_DIV							

Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000
12			RW	0

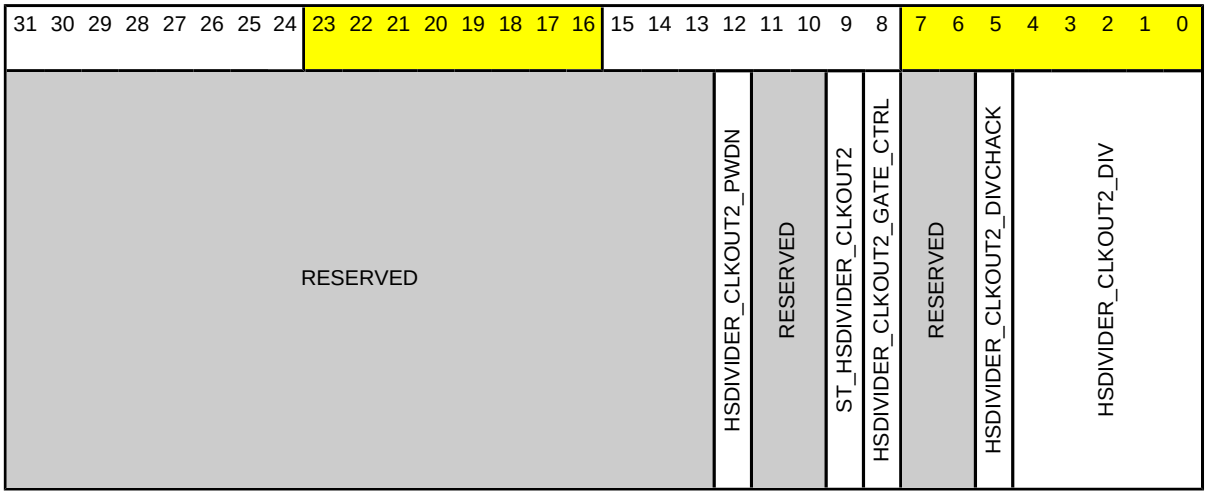
Bits	Field Name	Description	Type	Reset
	HS-DIVIDER_CLKOUT1_PWDN	~~Automatic power down for HSDIVIDER M4 divider and hence CLKOUT1 output when the o/p clock is gated.~~Direct power down control for HSDIVIDER M4 divider and CLKOUT1 output. Power down should be enabled only when clock is first gated. ~~Read 0x0: Keep M4 divider powered on even when CLKOUT1 is gated.~~ 0x0: Divider is powered up 0x1: Divider is powered down		
11:10	RESERVED		R	0x0
9	ST_HSDIVIDER_CLKOUT1	HSDIVIDER CLKOUT1 status Read 0x0: The clock output is gated Read 0x1: The clock output is enabled	R	0
8	HSDIVIDER_CLKOUT1_GATE_CTRL	Control gating of HSDIVIDER CLKOUT1 0x0: Automatically gate this clock when there is no dependency for it 0x1: Force this clock to stay enabled even if there is no request	RW	0
7:6	RESERVED		R	0x0
5	HSDIVIDER_CLKOUT1_DIVCHACK	Toggle on this status bit after changing HSDIVIDER_CLKOUT1_DIV indicates that the change in divider value has taken effect	R	0
4:0	HSDIVIDER_CLKOUT1_DIV	DPLL (M4+1) post-divider factor (1 to 31). 0x0: Reserved	RW	0x04

Table 3.67. Register Call Summary for Register CM_DIV_M4_DPLL_PER

Power Management Functional Description
• Power Management Functional Description:[0]

Table 3.68. CM_DIV_M5_DPLL_PER

Address Offset	0x0000 005C		
Physical Address	See Table 3.65	**Instance**	CKGEN_CM2
Description	This register provides controls over the CLKOUT2 o/p of the HSDIVIDER.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000

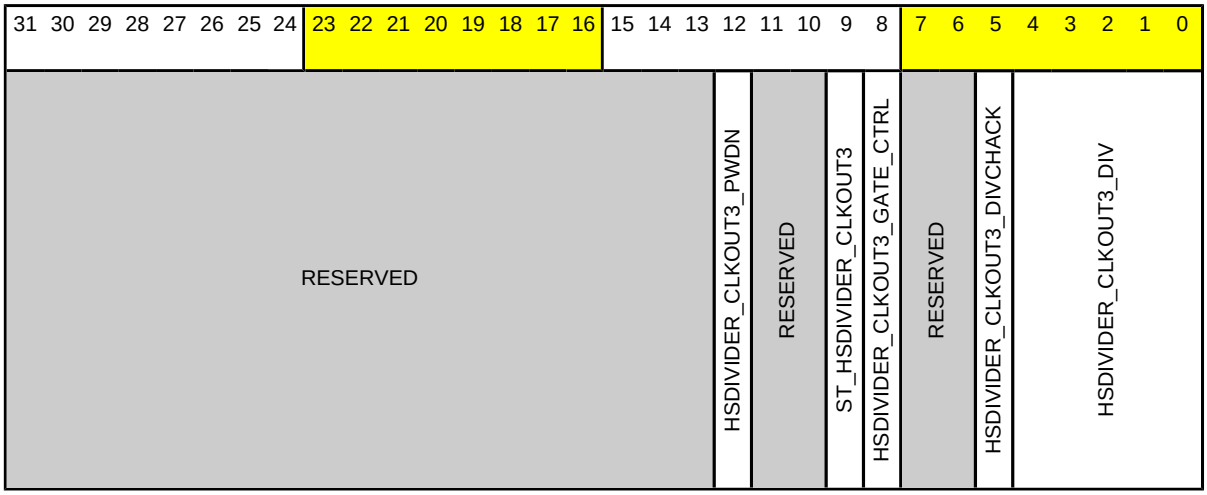
Bits	Field Name	Description	Type	Reset
12	HS-DIVIDER_CLKOUT2_PWDN	~~Automatic power down for HSDIVIDER M5 divider and hence CLKOUT2 output when the o/p clock is gated.~~Direct power down control for HSDIVIDER M5 divider and CLKOUT2 output. Power down should be enabled only when clock is first gated. ~~Read 0x0: Keep M5 divider powered on even when CLKOUT2 is gated.~~ 0x0: Divider is powered up 0x1: Divider is powered down	RW	0
11:10	RESERVED		R	0x0
9	ST_HSDIVIDER_CLKOUT2	HSDIVIDER CLKOUT2 status Read 0x0: The clock output is gated Read 0x1: The clock output is enabled	R	0
8	HSDIVIDER_CLKOUT2_GATE_CTRL	Control gating of HSDIVIDER CLKOUT2 0x0: Automatically gate this clock when there is no dependency for it 0x1: Force this clock to stay enabled even if there is no request	RW	0
7:6	RESERVED		R	0x0
5	HSDIVIDER_CLKOUT2_DIVCHACK	Toggle on this status bit after changing HSDIVIDER_CLKOUT2_DIV indicates that the change in divider value has taken effect	R	0
4:0	HSDIVIDER_CLKOUT2_DIV	DPLL (M5+1) post-divider factor (1 to 31). 0x0: Reserved	RW	0x04

Table 3.69. Register Call Summary for Register CM_DIV_M5_DPLL_PER

Power Management Functional Description
• Power Management Functional Description:[0]

Table 3.70. CM_DIV_M6_DPLL_PER

Address Offset	0x0000 0060		
Physical Address	SeeTable 3.65	**Instance**	CKGEN_CM2
Description	This register provides controls over the CLKOUT3 o/p of the HSDIVIDER.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000

Bits	Field Name	Description	Type	Reset
12	HS-DIVIDER_CLKOUT3_PWDN	~~Automatic power down for HSDIVIDER M6 divider and hence CLKOUT3 output when the o/p clock is gated.~~Direct power down control for HSDIVIDER M6 divider and CLKOUT3 output. Power down should be enabled only when clock is first gated. ~~Read 0x0: Keep M6 divider powered on even when CLKOUT3 is gated.~~ 0x0: Divider is powered up 0x1: Divider is powered down	RW	0
11:10	RESERVED		R	0x0
9	ST_HSDIVIDER_CLKOUT3	HSDIVIDER CLKOUT3 status Read 0x0: The clock output is gated Read 0x1: The clock output is enabled	R	0
8	HSDIVIDER_CLKOUT3_GATE_CTRL	Control gating of HSDIVIDER CLKOUT3 0x0: Automatically gate this clock when there is no dependency for it 0x1: Force this clock to stay enabled even if there is no request	RW	0
7:6	RESERVED		R	0x0
5	HSDIVIDER_CLKOUT3_DIVCHACK	Toggle on this status bit after changing HSDIVIDER_CLKOUT3_DIV indicates that the change in divider value has taken effect	R	0
4:0	HSDIVIDER_CLKOUT3_DIV	DPLL (M6+1) post-divider factor (1 to 31). 0x0: Reserved	RW	0x04

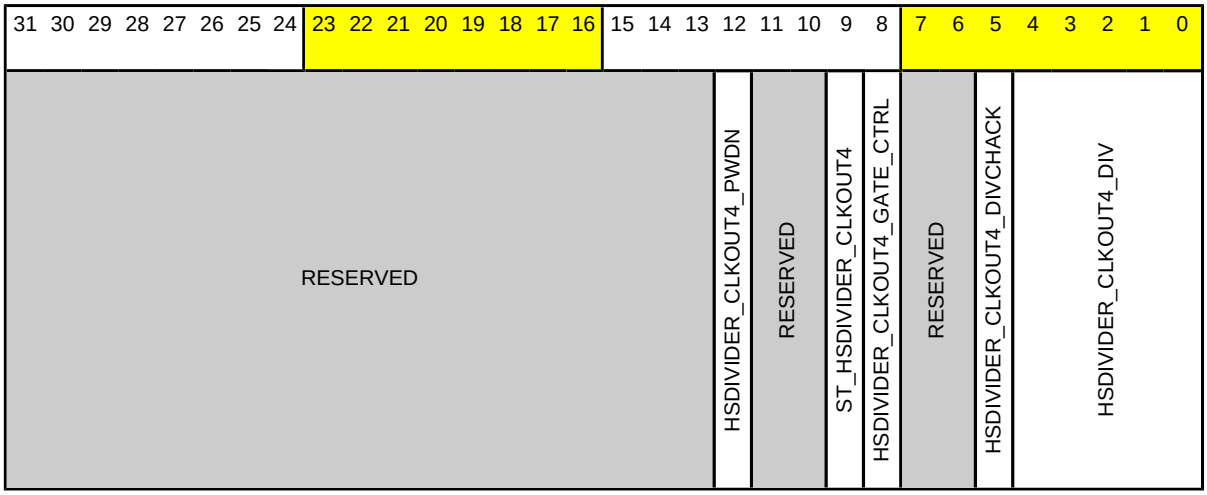
Table 3.71. Register Call Summary for Register CM_DIV_M6_DPLL_PER

Power Management Functional Description

- Power Management Functional Description:[0]

Table 3.72. CM_DIV_M7_DPLL_PER

Address Offset	0x0000 0064		
Physical Address	SeeTable 3.65	**Instance**	CKGEN_CM2
Description	This register provides controls over the CLKOUT4 o/p of the HSDIVIDER.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:13	RESERVED		R	0x00000

Bits	Field Name	Description	Type	Reset
12	HS-DIVIDER_CLKOUT4_PWDN	~~Automatic power down for HSDIVIDER M7 divider and hence CLKOUT4 output when the o/p clock is gated.~~Direct power down control for HSDIVIDER M7 divider and CLKOUT4 output. Power down should be enabled only when clock is first gated. ~~Read 0x0: Keep M7 divider powered on even when CLKOUT4 is gated.~~ 0x0: Divider is powered up 0x1: Divider is powered down	RW	0
11:10	RESERVED		R	0x0
9	ST_HSDIVIDER_CLKOUT4	HSDIVIDER CLKOUT4 status Read 0x0: The clock output is gated Read 0x1: The clock output is enabled	R	0
8	HSDIVIDER_CLKOUT4_GATE_CTRL	Control gating of HSDIVIDER CLKOUT4 0x0: Automatically gate this clock when there is no dependency for it 0x1: Force this clock to stay enabled even if there is no request	RW	0
7:6	RESERVED		R	0x0
5	HSDIVIDER_CLKOUT4_DIVCHACK	Toggle on this status bit after changing HSDIVIDER_CLKOUT4_DIV indicates that the change in divider value has taken effect	R	0
4:0	HSDIVIDER_CLKOUT4_DIV	DPLL (M7+1) post-divider factor (1 to 31). 0x0: Reserved	RW	0x04

Table 3.73. Register Call Summary for Register CM_DIV_M7_DPLL_PER

Power Management Functional Description

- Power Management Functional Description:[0]

Table 3.74. CM_CLKSEL_DPLL_USB

Address Offset	0x0000 008C		
Physical Address	See Table 3.65	**Instance**	CKGEN_CM2
Description	This register provides controls over the DPLL.		
Type	RW		

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
DPLL_SD_DIV	DPLL_BYP_CLKSEL / RESERVED	DPLL_MULT	DPLL_DIV

Bits	Field Name	Description	Type	Reset
31:24	DPLL_SD_DIV	Sigma-Delta divider select (2-255). This factor must be set by s/w to ensure optimum jitter performance. DPLL_SD_DIV = CEILING ([DPLL_MULT/(DPLL_DIV+1)] * CLKINP / 250), where CLKINP is the input clock of the DPLL in MHz). Must be set with M and N factors, and must not be changed once DPLL is locked.	RW	0x0~~0~~4

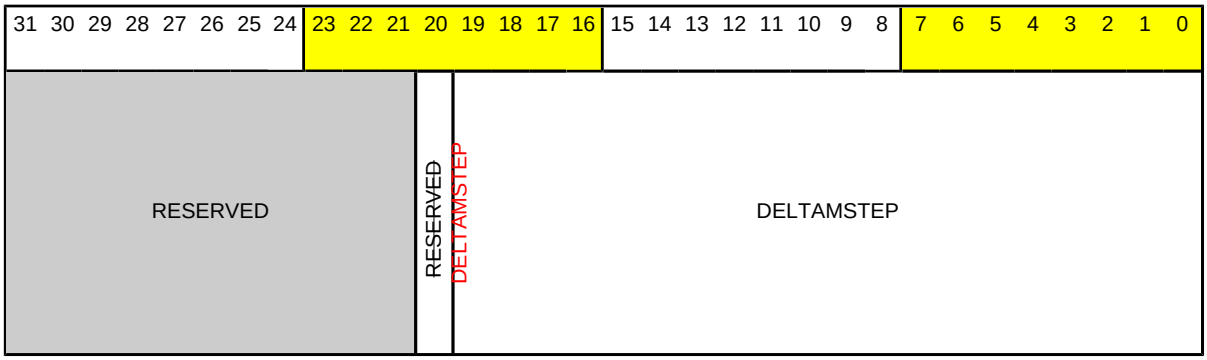
Bits	Field Name	Description	Type	Reset
		0x0: Reserved 0x1: Reserved		
23	DPLL_BYP_CLKSEL	Allows control of the BYPASS clock of the PLL and the associated HSDIVIDER. Same as ULOWCLKEN on DPLL. In DPLL Locked mode, 0 - No impact 1 - No impact In DPLL Bypass mode, 0 - CLKINP is selected as the BYPASS clock for CLKOUT 1 - CLKINPULOW is selected as the BYPASS clock for CLKOUT	RW	0
22:20	RESERVED		R	0x0
19:8	DPLL_MULT	DPLL multiplier factor (2 to 4095). This register is automatically cleared to 0 when the DPLL_EN field in the *CLKMODE_DPLL* register is set to select MN Bypass mode. (equal to input M of DPLL; M=2 to 4095 => DPLL multiplies by M). 0x0: Reserved 0x1: Reserved	RW	0x000
7:0	DPLL_DIV	DPLL divider factor (0 to 255) (equal to input N of DPLL; actual division factor is N+1).	RW	0x00

Table 3.75. Register Call Summary for Register CM_CLKSEL_DPLL_USB

Clock Management Functional Description
• Clock Management Functional Description:[0]

Table 3.76. CM_SSC_DELTAMSTEP_DPLL_USB

Address Offset	0x0000 00A8		
Physical Address	SeeTable 3.65	**Instance**	CKGEN_CM2
Description	Control the DeltaMStep parameter for Spread Spectrum Clocking. [warm reset insensitive]		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:~~20~~21	RESERVED		R	0x000
~~19~~20:0	DELTAMSTEP	DeltaMStep is split into fractional and integer part. For Triangular Spread Spectrum: [~~19~~20:18] for integer part, [17:0] for fractional part For Square Wave Spread Spectrum [19:14] for integer part, [13:0] for fractional part	RW	0x00000

Table 3.77. Register Call Summary for Register CM_SSC_DELTAMSTEP_DPLL_USB

Clock Management Functional Description
• Clock Management Functional Description:[0]

3.11.32. ALWAYS_ON_CM2 Registers

Refer to OMAP4460 Silicon Revision 1.x TRM.

3.11.33. CORE_CM2 Registers

3.11.33.1. CORE_CM2 Register Summary

Table 3.78. CORE_CM2 Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	CORE_CM2 L4 Base Address
CM_L3_1_CLKSTC-TRL	RW	32	0x0000 0000	0x4A00 8700
CM_L3_1_DY-NAMICDEP	RW	32	0x0000 0008	0x4A00 8708
CM_L3_1_L3_1_CLK CTRL	R	32	0x0000 0020	0x4A00 8720
CM_L3_2_CLKSTC-TRL	RW	32	0x0000 0100	0x4A00 8800
CM_L3_2_DY-NAMICDEP	RW	32	0x0000 0108	0x4A00 8808
CM_L3_2_L3_2_CLK CTRL	R	32	0x0000 0120	0x4A00 8820
CM_L3_2_GPMC_CLK CTRL	RW	32	0x0000 0128	0x4A00 8828
CM_L3_2_OCMC _RAM_CLKCTRL	R	32	0x0000 0130	0x4A00 8830
CM_MPU_M3_CL KSTCTRL	RW	32	0x0000 0200	0x4A00 8900
CM_MPU_M3_STAT-ICDEP	RW	32	0x0000 0204	0x4A00 8904
CM_MPU_M3_DYNA-MICDEP	RW	32	0x0000 0208	0x4A00 8908
CM_MPU_M3_MP U_M3_CLKCTRL	RW	32	0x0000 0220	0x4A00 8920
CM_SDMA_CLKSTC-TRL	RW	32	0x0000 0300	0x4A00 8A00
CM_SDMA_STATICDE P	RW	32	0x0000 0304	0x4A00 8A04
CM_SDMA_DY-NAMICDEP	R	32	0x0000 0308	0x4A00 8A08
CM_SDMA_SD-MA_CLKCTRL	R	32	0x0000 0320	0x4A00 8A20
CM_MEMIF_CLKSTCT RL	RW	32	0x0000 0400	0x4A00 8B00
CM_MEMIF_DMM _CLKCTRL	R	32	0x0000 0420	0x4A00 8B20
CM_MEMIF_EMIF_FW _CLKCTRL	R	32	0x0000 0428	0x4A00 8B28
CM_MEMIF_EMIF_1_ CLKCTRL	RW	32	0x0000 0430	0x4A00 8B30
CM_MEMIF_EMIF_2_ CLKCTRL	RW	32	0x0000 0438	0x4A00 8B38
CM_MEMIF_DLL_CLK CTRL	RW	32	0x0000 0440	0x4A00 8B40
RESERVED	RW	32	0x0000 0450	0x4A00 8B50
RESERVED	RW	32	0x0000 0458	0x4A00 8B58

Register Name	Type	Register Width (Bits)	Address Offset	CORE_CM2 L4 Base Address
RESERVED	RW	32	0x0000 0460	0x4A00 8B60
CM_C2C_CLKSTCTRL	RW	32	0x0000 0500	0x4A00 8C00
CM_C2C_STATICDEP	RW	32	0x0000 0504	0x4A00 8C04
CM_C2C_DYNAMICDEP	RW	32	0x0000 0508	0x4A00 8C08
CM_C2C_C2C_CLKCTRL	R	32	0x0000 0520	0x4A00 8C20
RESERVED	R	32	0x0000 0528	0x4A00 8C28
CM_C2C_C2C_FW_CLKC-TRL	R	32	0x0000 0530	0x4A00 8C30
CM_L4CFG_CLKSTCTRL	RW	32	0x0000 0600	0x4A00 8D00
CM_L4CFG_DYNAM-ICDEP	RW	32	0x0000 0608	0x4A00 8D08
CM_L4CFG_L4_CFG_CLKCTRL	R	32	0x0000 0620	0x4A00 8D20
CM_L4CFG_SPINLOCK_CLKC-TRL	R	32	0x0000 0628	0x4A00 8D28
CM_L4CFG_MAILBOX_CLKCTRL	R	32	0x0000 0630	0x4A00 8D30
CM_L4CFG_SAR_ROM_CLKCTRL	R	32	0x0000 0638	0x4A00 8D38
CM_L3INSTR_CLKSTCTRL	R	32	0x0000 0700	0x4A00 8E00
CM_L3INSTR_L3_3_CLKCTRL	RW	32	0x0000 0720	0x4A00 8E20
CM_L3INSTR_L3_INSTR_CLKCTRL	RW	32	0x0000 0728	0x4A00 8E28
CM_L3INSTR_OCP_WP1_CLKCTRL	RW	32	0x0000 0740	0x4A00 8E40

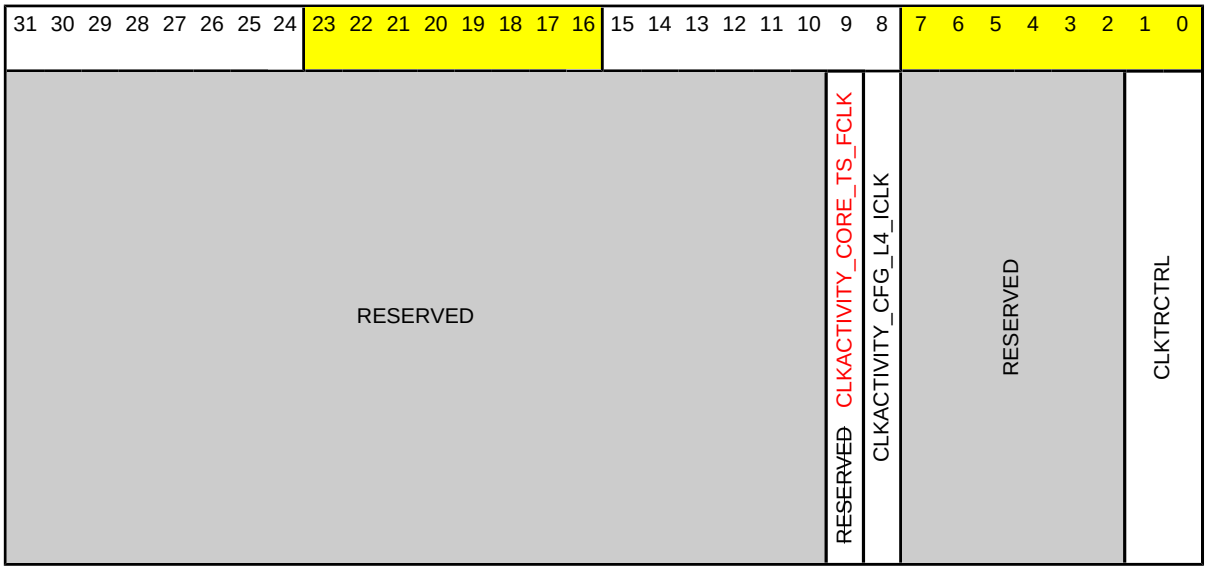
3.11.33.2. CORE_CM2 Register Description

Note

This section contains only modified registers.

Table 3.79. CM_L4CFG_CLKSTCTRL

Address Offset	0x0000 0600		
Physical Address	See Table 3.78	**Instance**	CORE_CM2
Description	This register enables the domain power state transition. It controls the HW supervised domain power state transition between ON-ACTIVE and ON-INACTIVE states. It also hold one status bit per clock input of the domain.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:910	RESERVED		R	0x000000
9	CLKACTIVITY_CORE_TS_FCLK	This field indicates the state of the CORE_TS_FCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0
8	CLKACTIVITY_CFG_L4_ICLK	This field indicates the state of the CFG_L4_ICLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0
7:2	RESERVED		R	0x00
1:0	CLKTRCTRL	Controls the clock state transition of the L4CFG clock domain. 0x0: NO_SLEEP: Sleep transition cannot be initiated. Wakeup transition may however occur. Read 0x1: Reserved Read 0x2: Reserved 0x3: HW_AUTO: Automatic transition is enabled. Sleep and wakeup transition are based upon hardware conditions.	RW	0x0

Table 3.80. Register Call Summary for Register CM_L4CFG_CLKSTCTRL

Clock Management Functional Description
• Clock Management Functional Description:[1]
PRCM Register Manual
• RESTORE_CM2 Register Description:[2]

Table 3.81. CM_L4CFG_DYNAMICDEP

Address Offset	0x0000 0608		
Physical Address	SeeTable 3.78	**Instance**	CORE_CM2
Description	This register controls the dynamic domain depedencies from L4_CFG domain towards 'target' domains. It is relevant only for domain having INTRCONN master port(s).		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				WINDOWSIZE				RESERVED				RESERVED MPU_DYNDEP	C2C_DYNDEP	RESERVED	ALWONCORE_DYNDEP	L4WKUP_DYNDEP	RESERVED			SDMA_DYNDEP	RESERVED	CAM_DYNDEP	DSS_DYNDEP	L3_INIT_DYNDEP	L3_2_DYNDEP	L3_1_DYNDEP	MEMIF_DYNDEP	RESERVED		DSP_DYNDEP	RESERVED

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:24	WINDOWSIZE	Size of sliding window used to monitor INTRCONN interface activity for determination of auto-sleep feature. Time unit defined by CM_DYN_DEP_PRESCAL register.	RW	0x4
23:~~19~~20	RESERVED		R	0x0~~0~~
19	MPU_DYNDEP	Dynamic dependency towards MPU clock domain Read 0x1: Dependency is enabled	R Rreturns1s	1
18	C2C_DYNDEP	Dynamic dependency towards C2C clock domain Read 0x1: Dependency is enabled	R Rreturns1s	1
17	RESERVED		R	1
16	ALWONCORE_DYNDEP	Dynamic dependency towards ALWONCORE clock domain Read 0x1: Dependency is enabled	R Rreturns1s	1
15	L4WKUP_DYNDEP	Dynamic dependency towards L4WKUP clock domain Read 0x1: Dependency is enabled	R Rreturns1s	1
14:12	RESERVED		R	0x0
11	SDMA_DYNDEP	Dynamic dependency towards SDMA clock domain Read 0x1: Dependency is enabled	R Rreturns1s	1
10	RESERVED		R	0
9	CAM_DYNDEP	Dynamic dependency towards ISS clock domain Read 0x0: Dependency is disabled	R	0
8	DSS_DYNDEP	Dynamic dependency towards DSS clock domain Read 0x1: Dependency is enabled	R Rreturns1s	1
7	L3_INIT_DYNDEP	Dynamic dependency towards L3INIT clock domain Read 0x1: Dependency is enabled	R Rreturns1s	1
6	L3_2_DYNDEP	Dynamic dependency towards L3_2 clock domain Read 0x1: Dependency is enabled	R Rreturns1s	1
5	L3_1_DYNDEP	Dynamic dependency towards L3_1 clock domain Read 0x1: Dependency is enabled	R Rreturns1s	1
4	MEMIF_DYNDEP	Dynamic dependency towards MEMIF clock domain Read 0x1: Dependency is enabled	R Rreturns1s	1
3:2	RESERVED		R	0x0
1	DSP_DYNDEP	Dynamic dependency towards DSP clock domain Read 0x1: Dependency is enabled	R Rreturns1s	1
0	RESERVED		R	0

Table 3.82. Register Call Summary for Register CM_L4CFG_DYNAMICDEP

Power Management Functional Description
• Power Management Functional Description:[0]
PRCM Register Manual
• RESTORE_CM2 Register Description:[1]

3.11.34. IVAHD_CM2 Registers

Refer to OMAP4460 Silicon Revision 1.x TRM.

3.11.35. CAM_CM2 Registers

Refer to OMAP4460 Silicon Revision 1.x TRM.

3.11.36. DSS_CM2 Registers

The Video DAC (VDAC) functionality is not supported

3.11.37. SGX_CM2 Registers

Refer to OMAP4460 Silicon Revision 1.x TRM.

3.11.38. L3INIT_CM2 Registers

Refer to OMAP4460 Silicon Revision 1.x TRM.

3.11.39. L4PER_CM2 Registers

Refer to OMAP4460 Silicon Revision 1.x TRM.

3.11.40. RESTORE_CM2 Registers

3.11.40.1. RESTORE_CM2 Register Summary

Table 3.83. RESTORE_CM2 Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	RESTORE_CM2 L4 Base Address
CM_L3_1_CLKSTC-TRL_RESTORE	RW	32	0x0000 0000	0x4A00 9E00
CM_L3_2_CLKSTC-TRL_RESTORE	RW	32	0x0000 0004	0x4A00 9E04
CM_L4CFG_CLKSTCTRL_RES-TORE	RW	32	0x0000 0008	0x4A00 9E08
CM_MEMIF_CLKSTCTRL_RES-TORE	RW	32	0x0000 000C	0x4A00 9E0C
CM_L4PER_CLKSTCTRL_RES-TORE	RW	32	0x0000 0010	0x4A00 9E10
CM_L3INIT_CLKSTC TRL_RESTORE	RW	32	0x0000 0014	0x4A00 9E14
CM_L3INSTR_L3_3_ CLKCTRL_RESTORE	RW	32	0x0000 0018	0x4A00 9E18

Register Name	Type	Register Width (Bits)	Address Offset	RESTORE_CM2 L4 Base Address
CM_L3INSTR_L3_INSTR_CLKCTRL_RESTORE	RW	32	0x0000 001C	0x4A00 9E1C
CM_L3INSTR_OCP_WP1 _CLKCTRL_RESTORE	RW	32	0x0000 0020	0x4A00 9E20
CM_CM2_PROFILING _CLKCTRL_RESTORE	RW	32	0x0000 0024	0x4A00 9E24
CM_C2C_STATICDEP _RESTORE	RW	32	0x0000 0028	0x4A00 9E28
CM_L3_1_DY-NAMICDEP_RESTORE	RW	32	0x0000 002C	0x4A00 9E2C
CM_L3_2_DY-NAMICDEP_RESTORE	RW	32	0x0000 0030	0x4A00 9E30
CM_C2C_DYNAMICDEP_RESTORE	RW	32	0x0000 0034	0x4A00 9E34
CM_L4CFG_DYNAM-ICDEP_RESTORE	RW	32	0x0000 0038	0x4A00 9E38
CM_L4PER_DYNAM-ICDEP_RESTORE	RW	32	0x0000 003C	0x4A00 9E3C
CM_L4PER_GPIO2 _CLKCTRL_RESTORE	RW	32	0x0000 0040	0x4A00 9E40
CM_L4PER_GPIO3 _CLKCTRL_RESTORE	RW	32	0x0000 0044	0x4A00 9E44
CM_L4PER_GPIO4 _CLKCTRL_RESTORE	RW	32	0x0000 0048	0x4A00 9E48
CM_L4PER_GPIO5 _CLKCTRL_RESTORE	RW	32	0x0000 004C	0x4A00 9E4C
CM_L4PER_GPIO6 _CLKCTRL_RESTORE	RW	32	0x0000 0050	0x4A00 9E50
CM_L3INIT_HSUS-BHOST _CLKCTRL_RESTORE	RW	32	0x0000 0054	0x4A00 9E54
CM_L3INIT_HSUS-BTLL_CLKCTRL_RES-TORE	RW	32	0x0000 0058	0x4A00 9E58
CM_SDMA_STATICDEP_RESTORE	RW	32	0x0000 005C	0x4A00 9E5C

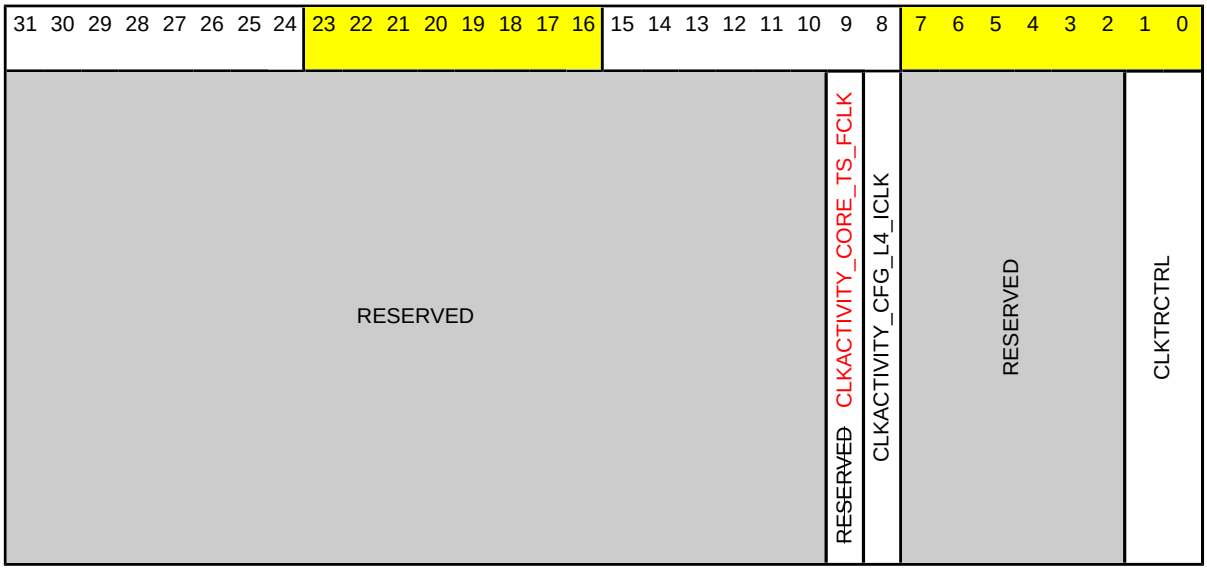
3.11.40.2. RESTORE_CM2 Register Description

Note

This section contains only modified registers.

Table 3.84. CM_L4CFG_CLKSTCTRL_RESTORE

Address Offset	0x0000 0008		
Physical Address	See Table 3.83	**Instance**	RESTORE_CM2
Description	Second address map for register CM_L4CFG_CLKSTCTRL. Used only by automatic restore upon wakeup from device OFF mode.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:910	RESERVED		R	0x000000
9	CLKACTIVITY_CORE_TS_FCLK	This field indicates the state of the CORE_TS_FCLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0
8	CLKACTIVITY_CFG_L4_ICLK	This field indicates the state of the L4_CFG_GICLK clock in the domain. [warm reset insensitive] Read 0x0: Corresponding clock is definitely gated Read 0x1: Corresponding clock is running or gating/ungating transition is on-going	R	0
7:2	RESERVED		R	0x00
1:0	CLKTRCTRL	Controls the clock state transition of the L4CFG clock domain. 0x0: NO_SLEEP: Sleep transition cannot be initiated. Wakeup transition may however occur. Read 0x1: Reserved Read 0x2: Reserved 0x3: HW_AUTO: Automatic transition is enabled. Sleep and wakeup transition are based upon hardware conditions.	RW	0x0

Table 3.85. CM_L4CFG_DYNAMICDEP_RESTORE

Address Offset	0x0000 0038		
Physical Address	See Table 3.83	**Instance**	RESTORE_CM2
Description	Second address map for register CM_L4CFG_DYNAMICDEP. Used only by automatic restore upon wakeup from device OFF mode.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								WINDOWSIZE				RESERVED	MPU_DYNDEP C2C_DYNDEP	RESERVED	ALWONCORE_DYNDEP	L4WKUP_DYNDEP	RESERVED			SDMA_DYNDEP	RESERVED	ISS_DYNDEP	DSS_DYNDEP	L3INIT_DYNDEP	L3_2_DYNDEP	L3_1_DYNDEP	MEMIF_DYNDEP	RESERVED		DSP_DYNDEP	RESERVED

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:24	WINDOWSIZE	Size of sliding window used to monitor OCP interface activity for determination of auto-sleep feature. Time unit defined by CM_DYN_DEP_PRESCAL register.	RW	0x4
23:~~19~~20	RESERVED		R	0x0~~0~~
19	MPU_DYNDEP	Dynamic dependency towards MPU clock domain Read 0x1: Dependency is enabled	R Rreturns1s	1
18	C2C_DYNDEP	Dynamic dependency towards D2D clock domain Read 0x1: Dependency is enabled	R Rreturns1s	1
17	RESERVED		R	1
16	ALWONCORE_DYNDEP	Dynamic dependency towards ALWONCORE clock domain Read 0x1: Dependency is enabled	R Rreturns1s	1
15	L4WKUP_DYNDEP	Dynamic dependency towards L4WKUP clock domain Read 0x1: Dependency is enabled	R Rreturns1s	1
14:12	RESERVED		R	0x0
11	SDMA_DYNDEP	Dynamic dependency towards SDMA clock domain Read 0x1: Dependency is enabled	R Rreturns1s	1
10	RESERVED		R	0
9	ISS_DYNDEP	Dynamic dependency towards ISS clock domain Read 0x0: Dependency is disabled	R	0
8	DSS_DYNDEP	Dynamic dependency towards DSS clock domain Read 0x1: Dependency is enabled	R Rreturns1s	1
7	L3INIT_DYNDEP	Dynamic dependency towards L3INIT clock domain Read 0x1: Dependency is enabled	R Rreturns1s	1
6	L3_2_DYNDEP	Dynamic dependency towards L3_2 clock domain Read 0x1: Dependency is enabled	R Rreturns1s	1
5	L3_1_DYNDEP	Dynamic dependency towards L3_1 clock domain Read 0x1: Dependency is enabled	R Rreturns1s	1
4	MEMIF_DYNDEP	Dynamic dependency towards MEMIF clock domain Read 0x1: Dependency is enabled	R Rreturns1s	1
3:2	RESERVED		R	0x0
1	DSP_DYNDEP	Dynamic dependency towards DSP clock domain Read 0x1: Dependency is enabled	R Rreturns1s	1
0	RESERVED		R	0

Table 3.86. Register Call Summary for Register CM_L4CFG_DYNAMICDEP_RESTORE

Power Management Functional Description
• Power Management Functional Description:[0]

3.12. SCRM Register Manual

3.12.2. SCRM Registers

Refer to OMAP4460 Silicon Revision 1.x TRM.

3.13. SR Register Manual

3.13.2. SR Registers

Refer to OMAP4460 Silicon Revision 1.x TRM.

Chapter 4. Dual Cortex-A9 MPU Subsystem

This chapter describes differences in Dual Cortex-A9 MPU Subsystem between the OMAP4430 Silicon Revision 2.x and OMAP4460 Silicon Revision 1.x multimedia devices.

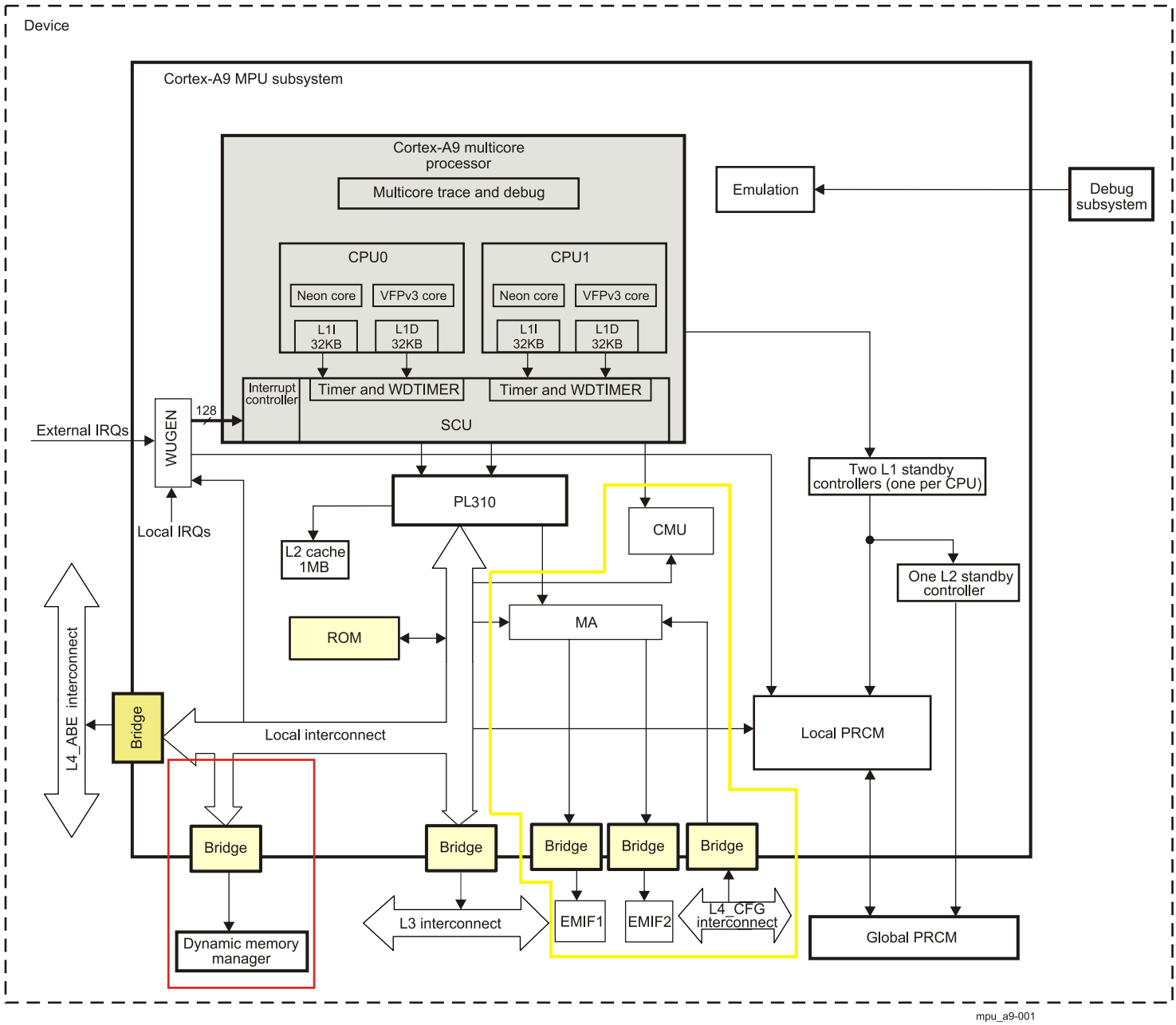
4.1. Dual Cortex-A9 MPU Subsystem Overview

4.1.1. Introduction

Two new modules are added to the Cortex-A9 MPU subsystem - the Memory Adapter and the Cache Management Unit (CMU). The port to the Dynamic Memory Manager (DMM) module is removed.

Figure 4.5 shows a high-level block diagram of the MPU subsystem.

Figure 4.1. Cortex-A9 MPU Subsystem Overview



4.1.2. Features

The Cortex-A9 MPU subsystem integrates the following:

- ARM subchip
  - Cortex-A9 core revision ~~r1p2~~ r2p10
- PL310 L2 cache controller (revision ~~r2p0~~ r3p1-50rel0) with 1 MB cache size
  - 16-way set associative
  - 32-byte line size
  - PL310 address filtering function used to splite accesses between MA and Local interconnect
  - Two slave ports and two master ports
  - Includes four 256-bit line-fill-buffers (LFBs) shared by the master ports
  - Each slave port includes two 256-bit line-read-buffers (LRBs)
  - Includes four 256-bit store buffers with merge capability
  - Support for 64-byte linefills issued to L3
- Program trace macrocell (PTM)
- Emulation logic (cross-triggers)
- AMBA advanced trace bus (ATB) trace port
- Advanced peripheral bus (APB) port
- ROM memory
- Wake-up generator (WUGEN) module – Responsible for waking up the CPUs
- Standby controllers – The Cortex-A9 MPU implements a two-level standby controller consisting of two L1 standby controllers (one per CPU) and one L2 standby controller. The standby controllers handle the power transitions inside the Cortex-A9 MPU subsystem.
- Interface to audio back-end (ABE) subsystem: Enables direct connection between the Cortex-A9 multicore processor and the ABE module to reduce power consumption during long audio playback.
- Power, clock, and reset manager: The Cortex-A9 MPU subsystem implements a local PRCM to handle CPU power domains.
- Memory Adapter (MA)
- Cache Management Unit (CMU)

4.2. Dual Cortex-A9 MPU Subsystem Integration

4.2.1. Clock Distribution

New clock signals to the CMU and MA are described.

The clock generator generates the following clocks from the MPU DPLL output clock:

- ARM_FCLK – ARM Cortex-A9 MPCore functional clock
- LOCAL_INTCNT_FCLK – Local interconnect functional clock
- CACHE_CTRL_FCLK – PL310 cache controller functional clock
- CMU_CLK1 and CMU_CLK2 - CMU functional clocks
- MA_CLK1, MA_CLK2 and MA_CLK3 - MA functional clocks

The following clocks have the same frequency:

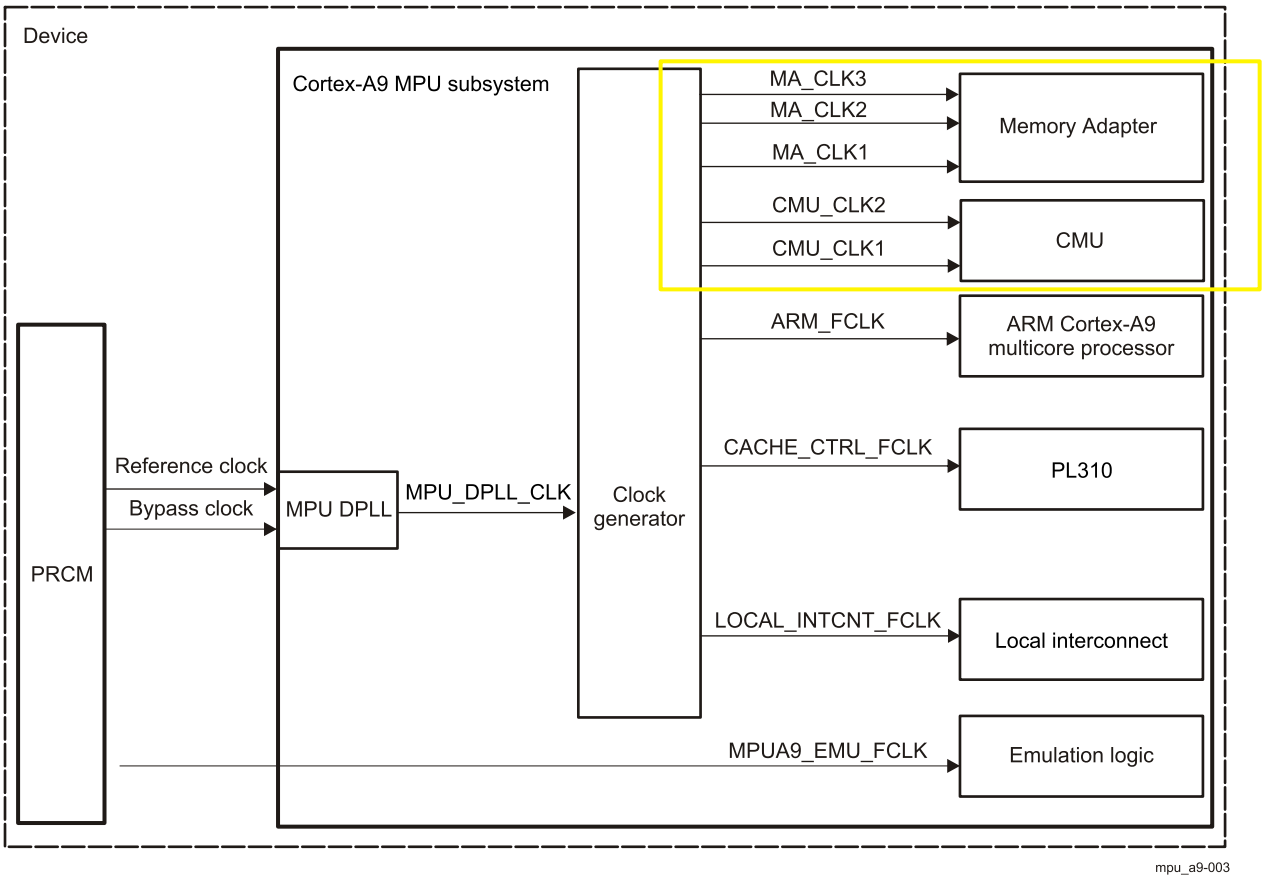
- ARM_FCLK
- CACHE_CTRL_FCLK
- CMU_CLK1
- MA_CLK1

The frequency of the following clocks is half of ARM_FCLK:

- LOCAL_INTCNT_FCLK
- CMU_CLK2
- MA_CLK2

The frequency of MA_CLK3 is software-configurable (through the CM_MPU_MPU_CLKCTRL[24] CLKSEL_EMIF_DIV_MODE bit) and can be half of the ARM_FCLK and one fourth of the ARM_FCLK frequency.

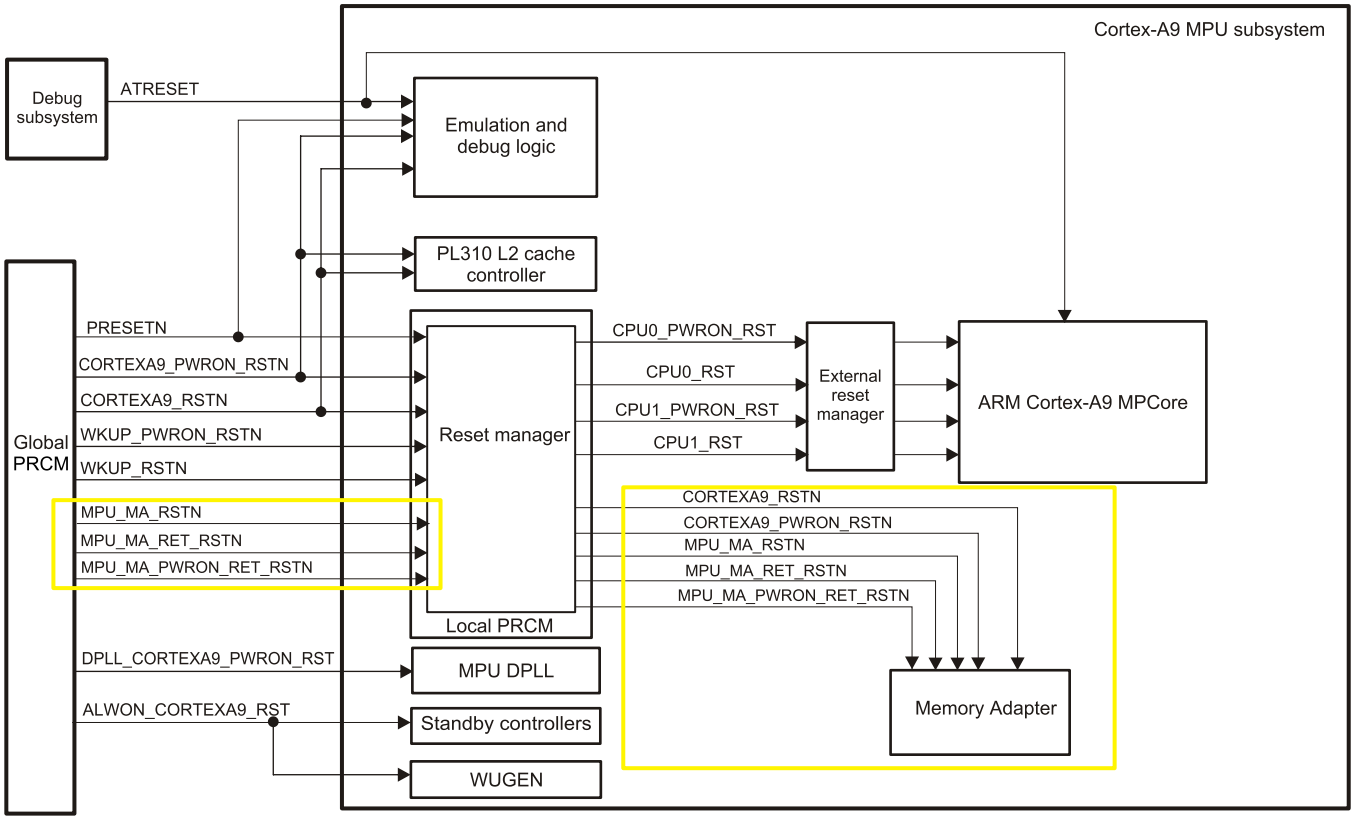
Figure 4.2. Cortex-A9 MPU Subsystem Clocking Scheme



4.2.2. Reset Distribution

New reset signals to the MA are described.

Figure 4.3. Cortex-A9 MPU Subsystem Reset Scheme



All ~~five~~ eight external resets which are input to the local PRCM signals are active low. All ~~eight~~ eleven external reset input signals are driven by the global PRCM, except the ATRESETN reset signal which is driven by the device debug subsystem. There are four internal reset signals, generated by the local PRCM.

The MA has five incoming reset signals:

- CORTEXA9_RSTN
- CORTEXA9_PWRON_RSTN
- MPU_MA_RSTN
- MPU_MA_RET_RSTN
- MPU_MA_PWRON_RET_RSTN

4.3. Dual Cortex-A9 MPU Subsystem Functional Description

4.3.1. Cortex-A9 MPU Subsystem Block Diagram

The port to the dynamic memory manager (DMM) module is removed from the Local interconnect. The Memory adapter and CMU modules are attached to the Local interconnect. The on-chip ROM memory start/end address is changed (but the size is not impacted).

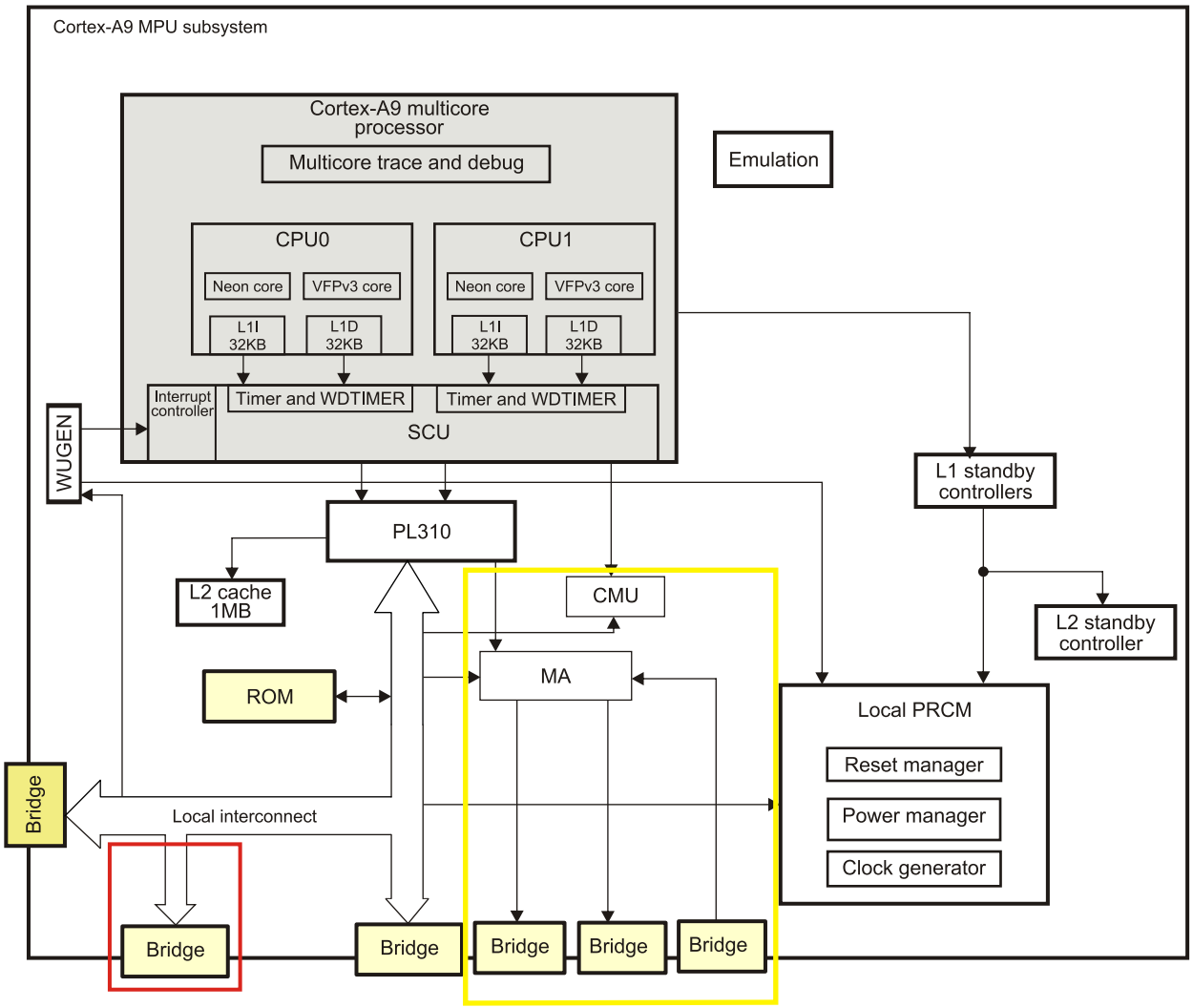
The Cortex-A9 MPU subsystem integrates the following group of submodules:

- Local interconnect: Connects the ARM Cortex-A9 multicore processor to:
  - Level 3 (L3) interconnect
  - ~~dynamic memory manager~~
  - ABE interconnect
  - local PRCM
  - PL310 L2 cache controller
  - on-chip ROM memory
  - WUGEN
  - CMU
  - MA
- Power, clock and reset manager
- On-chip ROM memory – CPU0 (the master CPU) can boot from this memory. The ROM memory size is 48KB, the address range is from ~~0x4002 0000~~ 0x4003 0000 to ~~0x4003 3FFF~~ 0x4003 BFFF. For more information, see Initialization chapter.

- MA
- CMU

Figure 4.4 is the Cortex-A9 MPU block diagram.

Figure 4.4. Cortex-A9 MPU Block Diagram



4.3.2. ARM Core

The PL310 master ports are updated. One of the 64-bit master ports to the L3 interconnect (through the Local interconnect) is replaced with 128-bit master port to the EMIF controller (through the Memory adapter module). Also address filtering is added to the PL310 features.

Table 4.1. ARM Core Key Features

Feature	Comment
L2 cache (PL310)	Main characteristics are: • Physically addressed and physically tagged • 16-way associative • 32-byte line length • Critical word first transactions • Prefetching capability • Pseudo-random victim selection policy • Two 256-bit LFBs in each master port • Two 256-bit LRBs in each slave port • Three 256-bit write buffers (merging capable) • Three 256-bit eviction buffers • Two 64-bit slave ports from SCU • Two master ports, one 64-bit port to L3 (through the Local interconnect) and one 128-bit port to EMIF (through the MA) • PL310 address filtering function used to split accesses between MA and Local interconnect • Support for 64-byte line fills issued to L3

4.3.3. Local Interconnect

Only one of the 64-bit buses of the PL310 L2 cache controller connects the Local interconect to the L3 interconnect. The EMIF ports are connected through the MA, not through the Local interconnect. The L3 and ABE interface frequencies are configurable in a device PRCM register. Connection to CMU and MA added. The Local interconnect contains internal configuartion register related to MA functionality. . The write transactions coming from the ARM Cortex-A9 processor can be software configurable by programming a dedicated register in the Control Module.

Main features:

- ~~Connects to the EMIF through a 128-bit interconnect port~~
- Connects to the L3 interconnect through a 64-bit port. The interface frequency is configurable between 1/2 (default value) and 1/4 of the MPU_DPLL_CLK clock signal frequency. This is programmable in the CM_MPU_MPU_CLKCTRL[24] CLKSEL_EMIF_DIV_MODE bit.
- Connects to the ABE through a 32-bit port. The interface frequency is configurable between 1/4 (default value) and 1/8 of the MPU_DPLL_CLK clock signal frequency. This is programmable in the CM_MPU_MPU_CLKCTRL[25] CLKSEL_ABE_DIV_MODE bit.
- Connection to the CMU for registers configuration
- Connection to the MA for registers configuration
- Contains internal configuartion register related to the MA function.
- Supports single-request-multiple-data (data handshaking) burst mode to pipeline requests
- Supports multiple outstanding requests
- Supports posted and non-posted write transactions, based on the attributes of the transactions coming from the ARM Cortex-A9 processor - ~~this is hardcoded, can not be software configurable~~ Software can override all writes from the local interconnect to the L3 interconnect to be nonposted, regardless of the attributes of the transactions coming from the ARM Cortex-A9 processor, by setting the FORCEWRNP[0] MPUFORCEWRNP bit to 0x1. For the register description, see chapter 18, Control Module.

Note

For the register description of the CM_MPU_MPU_CLKCTRL, see chapter 3 Power Reset and Clock Management.

4.3.4. Memory Adapter (MA)

The whole section is new, and explains the MA functionality and integration.

4.3.5. Cache Management Unit (CMU)

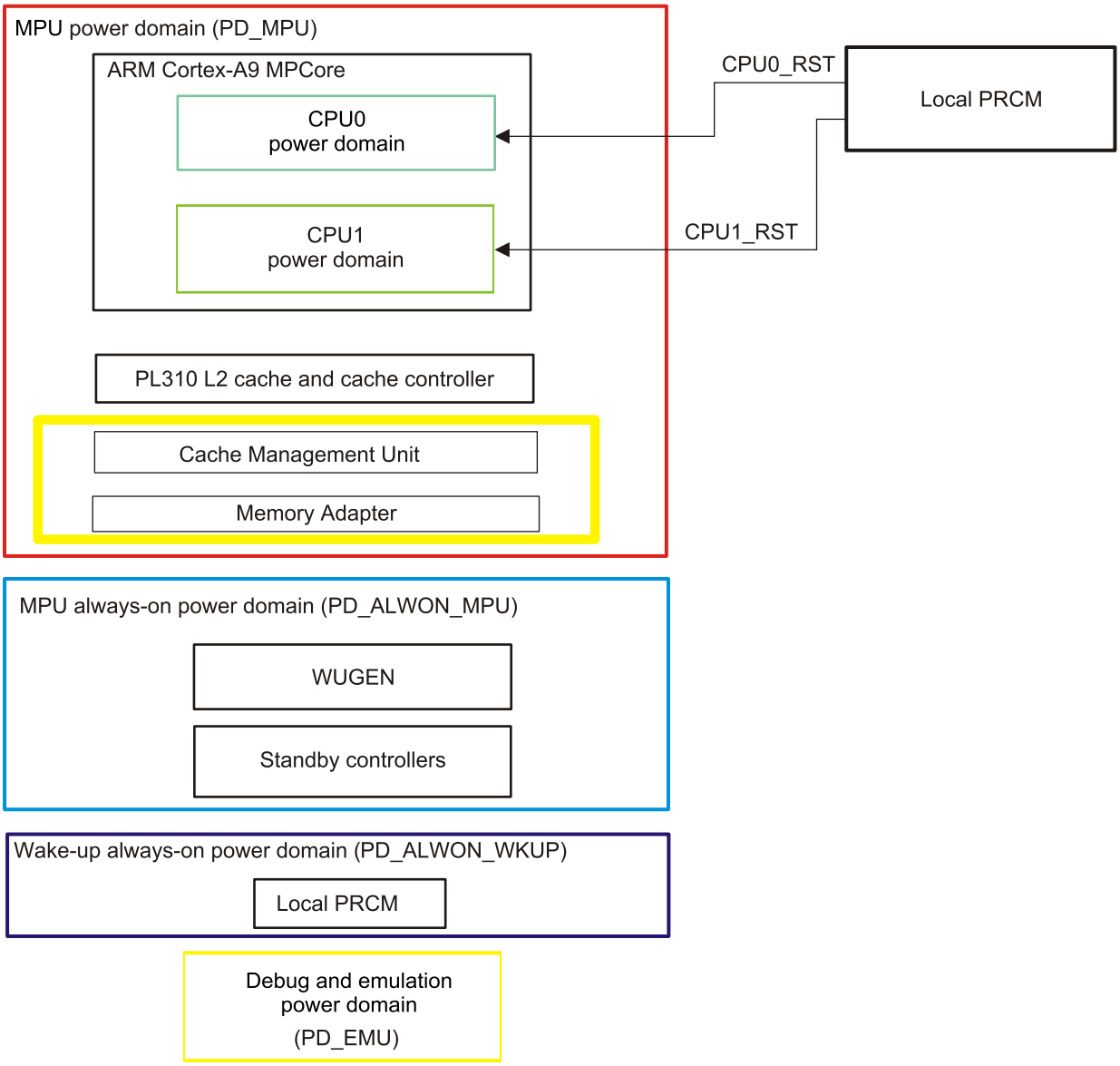
The whole section is new, and explains the CMU functionality and integration.

4.3.6. Power Management

4.3.6.1. Power Domains

The two new modules (CMU and MA) are added in the Cortex-A9 MPU Subsystem Power Domain Overview figure, they belong to the PD_MPU.

Figure 4.5. Cortex-A9 MPU Subsystem Power Domain Overview



4.3.6.2. Power States of CPU0 and CPU1

Refer to OMAP4460 Silicon Revision 1.x TRM.

4.3.6.3. WUGEN

Refer to OMAP4460 Silicon Revision 1.x TRM.

4.3.6.4. Power Transition Sequence

Refer to OMAP4460 Silicon Revision 1.x TRM.

4.3.6.5. CPU0 and CPU1 Power Domains Description

Refer to OMAP4460 Silicon Revision 1.x TRM.

4.4. Dual Cortex-A9 MPU Subsystem Register Manual

4.4.1. Cortex-A9 MPU Subsystem Instance Summary

Table 4.2. Cortex-A9 MPU Instance Summary

Module Name	Base Address	Size
SCU	0x4824 0000	128 bytes
GIC_Proc_Interface[1]	0x4824 0100	256 bytes
Timer	0x4824 0600	256 bytes
GIC_Intr_Distributor[2]	0x4824 1000	4KB
PL310	0x4824 2000	4KB
CORTEXA9_SOCKET_PRCM	0x4824 3000	512 bytes
CORTEXA9_PRM	0x4824 3200	512 bytes
CORTEXA9_CPU0	0x4824 3400	1KB
CORTEXA9_CPU1	0x4824 3800	1KB
CORTEXA9_WUGEN	0x4828 1000	4KB
CMU	0x4829 0000	64KB
Local interconnect	0x482A 0000	4KB
MA	0x482A F000	4KB

1. Processor interfaces – handles interrupt acknowledgement, interrupt masking, and interrupt completion acknowledgement.
2. Interrupt distributor – handles interrupt detection, interrupt prioritization, and distribution of interrupts to the CPUs.

4.4.2. SCU Registers

Refer to OMAP4460 Silicon Revision 1.x TRM.

4.4.3. Interrupt Controller Registers

Refer to OMAP4460 Silicon Revision 1.x TRM.

4.4.4. Timer Registers

Refer to OMAP4460 Silicon Revision 1.x TRM.

4.4.5. PL310 Registers

Refer to OMAP4460 Silicon Revision 1.x TRM.

4.4.6. Local PRCM Revision Register

Refer to OMAP4460 Silicon Revision 1.x TRM.

4.4.7. Local PRCM Registers

Refer to OMAP4460 Silicon Revision 1.x TRM.

4.4.8. Local PRCM CPU0 and CPU1 Registers

Refer to OMAP4460 Silicon Revision 1.x TRM.

4.4.9. Wake-Up Generator Registers

Due to new interrupt request signal (MA_IRQ_6), the WKG_ENB_A_0[6] and WKG_ENB_A_1[6] bits are impacted as follows:

4.4.9.1. CORTEXA9_WUGEN Register Summary

Table 4.3. CORTEXA9_WUGEN Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	VEYRON-SS_WKUPGEN Base Address
WKG_CONTROL_0	R	32	0x0000 0000	0x4828 1000
WKG_ENB_A_0	RW	32	0x0000 0010	0x4828 1010
WKG_ENB_B_0	RW	32	0x0000 0014	0x4828 1014
WKG_ENB_C_0	RW	32	0x0000 0018	0x4828 1018
WKG_ENB_D_0	RW	32	0x0000 001C	0x4828 101C
RESERVED	R	32	0x0000 0020	0x4828 1020
RESERVED	R	32	0x0000 0024	0x4828 1024
RESERVED	R	32	0x0000 0028	0x4828 1028
RESERVED	R	32	0x0000 002C	0x4828 102C
WKG_CONTROL_1	R	32	0x0000 0400	0x4828 1400
WKG_ENB_A_1	RW	32	0x0000 0410	0x4828 1410
WKG_ENB_B_1	RW	32	0x0000 0414	0x4828 1414
WKG_ENB_C_1	RW	32	0x0000 0418	0x4828 1418
WKG_ENB_D_1	RW	32	0x0000 041C	0x4828 141C
RESERVED	R	32	0x0000 0420	0x4828 1420
RESERVED	R	32	0x0000 0424	0x4828 1424
RESERVED	R	32	0x0000 0428	0x4828 1428
RESERVED	R	32	0x0000 042C	0x4828 142C
AUX_CORE_BOOT_0	RW	32	0x0000 0800	0x4828 1800
AUX_CORE_BOOT_1	RW	32	0x0000 0804	0x4828 1804
RESERVED	R	32	0x0000 0C00	0x4828 1C00
RESERVED	R	32	0x0000 0C04	0x4828 1C04
RESERVED	R	32	0x0000 0C08	0x4828 1C08
RESERVED	R	32	0x0000 0C0C	0x4828 1C0C

4.4.9.2. CORTEXA9_WUGEN Register Description

Note

This section contains only modified registers.

Table 4.4. WKG_ENB_A_0

Address Offset	0x0000 0010		
Physical Address	See Table 4.3	**Instance**	CORTEXA9_WUGEN
Description	This register enables the interrupts (for CPU0) from MA_IRQ_0 to MA_IRQ_31 write 0x0: disable interrupt write 0x1: enable interrupt		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WKG_ENB_FOR_INTR31	WKG_ENB_FOR_INTR30	WKG_ENB_FOR_INTR29	WKG_ENB_FOR_INTR28	WKG_ENB_FOR_INTR27	WKG_ENB_FOR_INTR26	WKG_ENB_FOR_INTR25	WKG_ENB_FOR_INTR24	WKG_ENB_FOR_INTR23	WKG_ENB_FOR_INTR22	WKG_ENB_FOR_INTR21	WKG_ENB_FOR_INTR20	WKG_ENB_FOR_INTR19	WKG_ENB_FOR_INTR18	WKG_ENB_FOR_INTR17	WKG_ENB_FOR_INTR16	WKG_ENB_FOR_INTR15	WKG_ENB_FOR_INTR14	WKG_ENB_FOR_INTR13	WKG_ENB_FOR_INTR12	WKG_ENB_FOR_INTR11	WKG_ENB_FOR_INTR10	WKG_ENB_FOR_INTR9	RESERVED	WKG_ENB_FOR_INTR7	~~RESERVED~~ WKG_ENB_FOR_INTR6	RESERVED	WKG_ENB_FOR_INTR4	RESERVED	WKG_ENB_FOR_INTR2	WKG_ENB_FOR_INTR1	WKG_ENB_FOR_INTR0

Bits	Field Name	Description	Type	Reset
31	WKG_ENB_FOR_INTR31		RW	1
30	WKG_ENB_FOR_INTR30		RW	1
29	WKG_ENB_FOR_INTR29		RW	1
28	WKG_ENB_FOR_INTR28		RW	1
27	WKG_ENB_FOR_INTR27		RW	1
26	WKG_ENB_FOR_INTR26		RW	1
25	WKG_ENB_FOR_INTR25		RW	1
24	WKG_ENB_FOR_INTR24		RW	1
23	WKG_ENB_FOR_INTR23		RW	1
22	WKG_ENB_FOR_INTR22		RW	1
21	WKG_ENB_FOR_INTR21		RW	1
20	WKG_ENB_FOR_INTR20		RW	1
19	WKG_ENB_FOR_INTR19		RW	1
18	WKG_ENB_FOR_INTR18		RW	1
17	WKG_ENB_FOR_INTR17		RW	1
16	WKG_ENB_FOR_INTR16		RW	1
15	WKG_ENB_FOR_INTR15		RW	1
14	WKG_ENB_FOR_INTR14		RW	1
13	WKG_ENB_FOR_INTR13		RW	1
12	WKG_ENB_FOR_INTR12		RW	1
11	WKG_ENB_FOR_INTR11		RW	1
10	WKG_ENB_FOR_INTR10		RW	1
9	WKG_ENB_FOR_INTR9		RW	1
8	RESERVED		RW	0[1]
7	WKG_ENB_FOR_INTR7		RW	1
6	~~RESERVED~~ WKG_ENB_FOR_INTR6		RW	1
5	RESERVED		RW	1
4	WKG_ENB_FOR_INTR4		RW	1
3	RESERVED		RW	1
2	WKG_ENB_FOR_INTR2		RW	1
1	WKG_ENB_FOR_INTR1		RW	1

Bits	Field Name	Description	Type	Reset
0	WKG_ENB_FOR_INTR0		RW	1

1. The reset value is 0x0 by safety reasons.

Table 4.5. Register Call Summary for Register WKG_ENB_A_0

Dual Cortex-A9 MPU Subsystem Register Manual

- Wake-Up Generator Registers:[0]
- CORTEXA9_WUGEN Register Summary:[1]

Table 4.6. WKG_ENB_A_1

Address Offset	0x0000 0410		
Physical Address	SeeTable 4.3	**Instance**	CORTEXA9_WUGEN
Description	This register enables the interrupts (for CPU1) from MA_IRQ_0 to MA_IRQ_31 write 0x0: disable interrupt write 0x1: enable interrupt		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WKG_ENB_FOR_INTR31	WKG_ENB_FOR_INTR30	WKG_ENB_FOR_INTR29	WKG_ENB_FOR_INTR28	WKG_ENB_FOR_INTR27	WKG_ENB_FOR_INTR26	WKG_ENB_FOR_INTR25	WKG_ENB_FOR_INTR24	WKG_ENB_FOR_INTR23	WKG_ENB_FOR_INTR22	WKG_ENB_FOR_INTR21	WKG_ENB_FOR_INTR20	WKG_ENB_FOR_INTR19	WKG_ENB_FOR_INTR18	WKG_ENB_FOR_INTR17	WKG_ENB_FOR_INTR16	WKG_ENB_FOR_INTR15	WKG_ENB_FOR_INTR14	WKG_ENB_FOR_INTR13	WKG_ENB_FOR_INTR12	WKG_ENB_FOR_INTR11	WKG_ENB_FOR_INTR10	WKG_ENB_FOR_INTR9	RESERVED	WKG_ENB_FOR_INTR7	RESERVED WKG_ENB_FOR_INTR6	RESERVED	WKG_ENB_FOR_INTR4	RESERVED	WKG_ENB_FOR_INTR2	WKG_ENB_FOR_INTR1	WKG_ENB_FOR_INTR0

Bits	Field Name	Description	Type	Reset
31	WKG_ENB_FOR_INTR31		RW	1
30	WKG_ENB_FOR_INTR30		RW	1
29	WKG_ENB_FOR_INTR29		RW	1
28	WKG_ENB_FOR_INTR28		RW	1
27	WKG_ENB_FOR_INTR27		RW	1
26	WKG_ENB_FOR_INTR26		RW	1
25	WKG_ENB_FOR_INTR25		RW	1
24	WKG_ENB_FOR_INTR24		RW	1
23	WKG_ENB_FOR_INTR23		RW	1
22	WKG_ENB_FOR_INTR22		RW	1
21	WKG_ENB_FOR_INTR21		RW	1
20	WKG_ENB_FOR_INTR20		RW	1
19	WKG_ENB_FOR_INTR19		RW	1
18	WKG_ENB_FOR_INTR18		RW	1
17	WKG_ENB_FOR_INTR17		RW	1
16	WKG_ENB_FOR_INTR16		RW	1

Bits	Field Name	Description	Type	Reset
15	WKG_ENB_FOR_INTR15		RW	1
14	WKG_ENB_FOR_INTR14		RW	1
13	WKG_ENB_FOR_INTR13		RW	1
12	WKG_ENB_FOR_INTR12		RW	1
11	WKG_ENB_FOR_INTR11		RW	1
10	WKG_ENB_FOR_INTR10		RW	1
9	WKG_ENB_FOR_INTR9		RW	1
8	RESERVED		RW	0[1]
7	WKG_ENB_FOR_INTR7		RW	1
6	~~RESERVED~~ WKG_ENB_FOR_INTR6		RW	1
5	RESERVED		RW	1
4	WKG_ENB_FOR_INTR4		RW	1
3	RESERVED		RW	1
2	WKG_ENB_FOR_INTR2		RW	1
1	WKG_ENB_FOR_INTR1		RW	1
0	WKG_ENB_FOR_INTR0		RW	1

1. The reset value is 0x0 by safety reasons.

Table 4.7. Register Call Summary for Register WKG_ENB_A_1

Dual Cortex-A9 MPU Subsystem Register Manual

- Wake-Up Generator Registers:[0]
- CORTEXA9_WUGEN Register Summary:[1]

4.4.10. CMU registers

4.4.10.1. CMU Register Summary

Table 4.8. CMU Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	CMU Base Address
CMUCONFIGREG	RW	32	0x0000 0000	0x4829 0000
CMUSTATUSREG	R	32	0x0000 0004	0x4829 0004
RESERVED	R	32	0x0000 0008	0x4829 0008
CMUINTRACK	R	32	0x0000 000C	0x4829 000C
CMUALLOCATE	R	32	0x0000 0010	0x4829 0010
CMUDEALLOCATE	RW	32	0x0000 0014	0x4829 0014
RESERVED	RW	32	0x0000 0018	0x4829 0018
CMUDEBUG	RW	32	0x0000 001C	0x4829 001C
CMUOPERATION_i[1]	RW	32	0x0000 1000 + (0x10 * i)	0x4829 1000 + (0x10 * i)
CMUSTARTPA_i[1]	RW	32	0x0000 1004 + (0x10 * i)	0x4829 1004 + (0x10 * i)
CMULENGTH_i[1]	RW	32	0x0000 1008 + (0x10 * i)	0x4829 1008 + (0x10 * i)
CMURANGESTATE_i[1]	R	32	0x0000 100C + (0x10 * i)	0x4829 100C + (0x10 * i)

1. i = 0 to 63

4.4.10.2. CMU Register Description

Table 4.9. CMUCONFIGREG

Address Offset	0x0000 0000		
Physical Address	Please refer toTable 4.8	**Instance**	CMU
Description	CMU Configuration Register		
Type	RW		

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
THREADS	QENTRIES	RESERVED	DISABLEPIPELINING, DISABLEPARALLEL, INTEN, RESERVED, ENNSWR, LINESTEP

Bits	Field Name	Description	Type	Reset
31:28	THREADS	Number of parallel CMO threads that can be simul taneously processed.	R	0x1
27:16	QENTRIES	Number of Queue Entries Configured	R	0x040
15:11	RESERVED	Reserved.	R	0x00
10	DISABLEPIPELINING	Disable pipelining of requests.	RW	1
9	DISABLEPARALLEL	Force sequential operation by disabling any parallelism between RangeSets.	RW	1
8	INTEN	Enable Interrupt on Set Completion. 0b0 = Don't interrupt. 0b1 = Interrupt on Completion.	RW	0
7:4	RESERVED	Reserved	R	0x0
3	ENNSWR	This enables Non-Safe programs to write this register. Out of reset - this bit is 0 which will prevent Non-Safe programs from writing it. Reading is always allowed. This bit can be set to 0x1 only through a Special Safe Monitor API. For more information about the API, see the Initialization chapter. The ROM Code will set this bit to 1 at boot time. The API can be used at runtime by the NS SW to enable/disable when necessary.	RW	0
2:0	LINESTEP	Size of smallest cache line size, log2 - 2. 0x0: Line Step = 4 bytes. 0x1: Line Step = 8 bytes. 0x2: Line Step = 16 bytes. 0x3: Line Step = 32 bytes. 0x4: Line Step = 64 bytes. 0x5: Line Step = 128 bytes. 0x6: Line Step = 256 bytes. 0x7: Line Step = 512 bytes.	RW	0x3

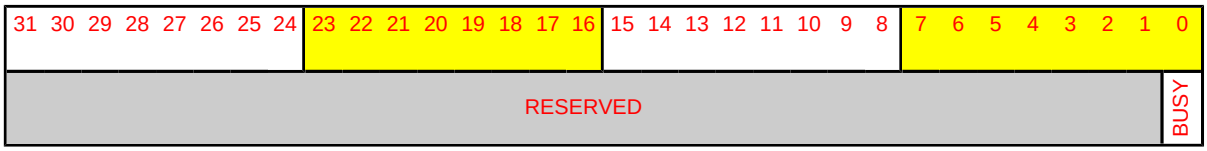
Table 4.10. Register Call Summary for Register CMUCONFIGREG

Dual Cortex-A9 MPU Subsystem Register Manual

- CMU Register Summary:[0]

Table 4.11. CMUSTATUSREG

Address Offset	0x0000 0004		
Physical Address	Please refer toTable 4.8	**Instance**	CMU
Description	CMU Status.		
Type	R		



Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved.	R	0x0000 0000
0	BUSY	Indicates that at least one set is active. 0b0 = CMU is idle. 0b1 = At least one set is active.	R	0

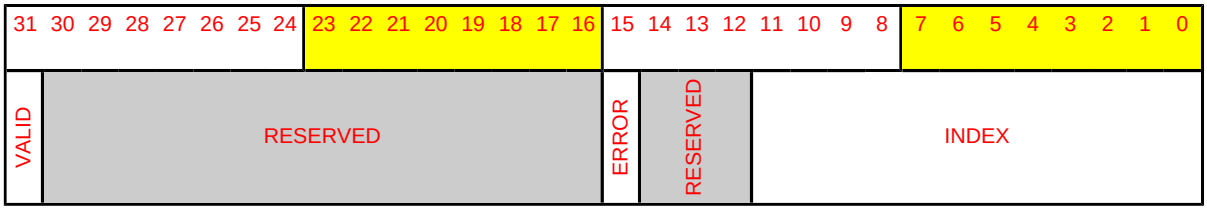
Table 4.12. Register Call Summary for Register CMUSTATUSREG

Dual Cortex-A9 MPU Subsystem Register Manual

- CMU Register Summary:[0]

Table 4.13. CMUINTRACK

Address Offset	0x0000 000C		
Physical Address	Please refer toTable 4.8	**Instance**	CMU
Description	Interrupt Acknowledgement Register. Returns the index of the RangeSet that caused the interrupt. An error bit indicates an error completion. Since there is a queue of interrupt acknowledgements, there is also a valid bit that indicates t hat there were no more interrupts on the queue.		
Type	R		



Bits	Field Name	Description	Type	Reset
31	VALID	Indicates that the label field is valid. Can read the entire queue of entries by reading until get Valid = 0.	R	0
30:16	RESERVED	Reserved	R	0x0000
15	ERROR	Indicates that the RangeSet operation completed with an error.	R	-
14:12	RESERVED	Reserved	R	0x0
11:0	INDEX	The index of the RangeSet that caused the interr upt.	R	0x---

Table 4.14. Register Call Summary for Register CMUINTRACK

Dual Cortex-A9 MPU Subsystem Register Manual

- CMU Register Summary:[0]

Table 4.15. CMUALLOCATE

Address Offset	0x0000 0010		
Physical Address	Please refer toTable 4.8	**Instance**	CMU
Description	Returns the index of a RangeSet in the Free state.		
Type	R		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NONE	RESERVED																							INDEX							

Bits	Field Name	Description	Type	Reset
31	NONE	Returns 0b0 if Index is valid or 0b1 if no RangeSets available for allocation	R	0
30:8	RES	Reserved.	R	0x000000
7:0	INDEX	Returns the Index of a RangeSet if one is available or zero.	R	0x00

Table 4.16. Register Call Summary for Register CMUALLOCATE

Dual Cortex-A9 MPU Subsystem Register Manual

- CMU Register Summary:[0]

Table 4.17. CMUDEALLOCATE

Address Offset	0x0000 0014		
Physical Address	Please refer toTable 4.8	**Instance**	CMU
Description	An index stored to this register frees the RangeSet with that index.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								INDEX							

Bits	Field Name	Description	Type	Reset
31:8	RESERVED	Reserved	R	0x000000
7:0	INDEX	RangeSet Index writen here is deallocated (set to the Free state).	RW	0x00

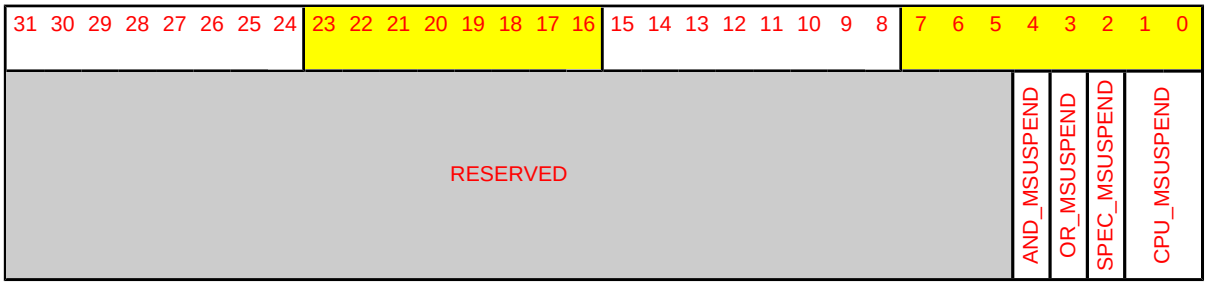
Table 4.18. Register Call Summary for Register CMUDEALLOCATE

Dual Cortex-A9 MPU Subsystem Register Manual

- CMU Register Summary:[0]

Table 4.19. CMUDEBUG

Address Offset	0x0000 001C		
Physical Address	Please refer toTable 4.8	**Instance**	CMU
Description	Debug register to configure how MSuspend from the various CPU's need to be looked at by CMU to either send or not send traffic during debug session.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:5	RESERVED		R	0x0000000
4	AND_MSUSPEND	This bit can be set so that only if all the MSuspend's of all the CPU's present are enabled, CMU will suspend activity to ACP port. Bits 3 and 2 need to be set to 0.	RW	0
3	OR_MSUSPEND	This bit can be set so that if any of the MSuspend's of CPUs present are enabled, then CMU will suspend activity to ACP port. Bits 4 and 2 need to be 0.	RW	0
2	SPEC_MSUSPEND	This bit enables CMU to look at specific CPU's MSuspend to suspend CMU activity to ACP port. Bits 4, 3 need to be 0 when bit 2 is 1.	RW	0
1:0	CPU_MSUSPEND	This field allows CMU to look at specific CPU's MSuspend to suspend traffic to ACP. When bit 4:2 = 3'b001, bits 1:0 indicates which CPU's MSuspend needs to be looked at. If the appropriate CPU's MSuspend is 1, then CMU will not generate any more activity to ACP and rest of system to have a non-intrusive debug session. When Bit 2 = 0, specific CPU's MSuspend cannot be used to control CMU's activity.	RW	0x0

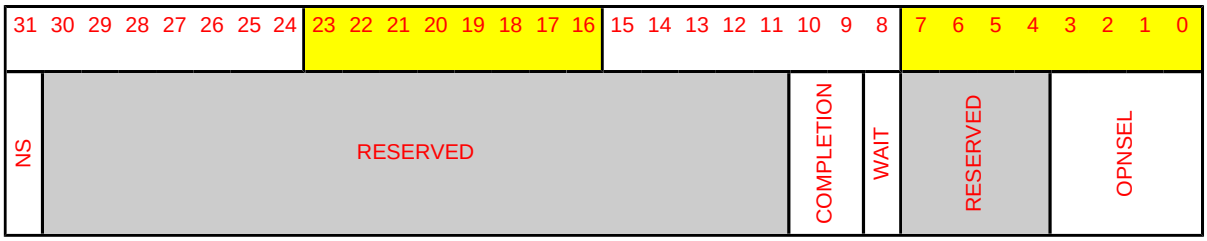
Table 4.20. Register Call Summary for Register CMUDEBUG

Dual Cortex-A9 MPU Subsystem Register Manual

- CMU Register Summary:[0]

Table 4.21. CMUOPERATION_i

Address Offset	0x0000 1000 + (0x10 * i)	**Index**	i = 0 to 63
Physical Address	Please refer toTable 4.8	**Instance**	CMU
Description	Controls the operation of one RangeSet of the CMU. Storing this register enqueues or activates the RangeSet. Note: must not write to any of the rangeset registers if State != 0b00. That indicates that previous values have not yet been transferred to the queue!		
Type	RW		



Bits	Field Name	Description	Type	Reset
31	NS	Not Safe. Set to NS used to access StartPA register. Writing one to this bit will perform the	RW W 1toSet	0

Bits	Field Name	Description	Type	Reset
		operation as non-safe. The software can not clear this bit to 0x0 after.		
30:11	RESERVED	Reserved.	R	0x00000
10:9	COMPLETION	Completion Signaling Options: 0x0: No notification of normal or error completion. 0x1: Interrupt on normal or error completion. 0x3: Reserved. 0x2: Interrupt on error but not normal completion.	RW	0x0
8	WAIT	Wait to start. 0b1 = Wait until all previous requests are complete. 0b0 = may proceed in parallel with previous requests.	RW	0
7:4	RESERVED	Reserved.	R	0x0
3:0	OPNSEL	Selects the Cache Management Operation. If an operation is started with a reserved OpnSel, the RangeSet is immediately moved to the Error state. 0x0: No operation is performed. A RangeSet activated with this OpnSel is immediately moved to the completed state. 0x1: Invalidate. 0x2: Clean. 0x3: Clean and Invalidate. 0x4: Reserved. 0x5: Reserved. 0x6: Reserved. 0x7: Reserved. 0x8: Reserved 0x9: Reserved. 0xA: Reserved. 0xB: Reserved. 0xC: Reserved. 0xD: Reserved. 0xE: Reserved. 0xF: Always moves the RangeSet to the Error State.	RW	0x0

Table 4.22. Register Call Summary for Register CMUOPERATION_i

Dual Cortex-A9 MPU Subsystem Register Manual

- CMU Register Summary:[0]

Table 4.23. CMUSTARTPA_i

Address Offset	0x0000 1004 + (0x10 * i)	**Index**	i = 0 to 63
Physical Address	Please refer toTable 4.8	**Instance**	CMU
Description	Starting (lower, inclusive) 32-bit physical address.		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STARTPA																															

Bits	Field Name	Description	Type	Reset
31:0	STARTPA	Start of range for cache operations.	RW	0x0000 0000

Table 4.24. Register Call Summary for Register CMUSTARTPA_i

Dual Cortex-A9 MPU Subsystem Register Manual

- CMU Register Summary:[0]

Table 4.25. CMULENGTH_i

Address Offset	0x0000 1008 + (0x10 * i)	**Index**	i = 0 to 63
Physical Address	Please refer toTable 4.8	**Instance**	CMU
Description	Length in bytes of the range - 1, giving a representable range of 1 byte to 4k bytes.		
Type	RW		

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
RESERVED			LEN

Bits	Field Name	Description	Type	Reset
31:12	RESERVED	Reserved	R	0x000
11:0	LEN	Length of range minus 1.	RW	0x000

Table 4.26. Register Call Summary for Register CMULENGTH_i

Dual Cortex-A9 MPU Subsystem Register Manual

- CMU Register Summary:[0]

Table 4.27. CMURANGESTATE_i

Address Offset	0x0000 100C + (0x10 * i)	**Index**	i = 0 to 63
Physical Address	Please refer toTable 4.8	**Instance**	CMU
Description	State of the Range Operation. Used to poll RangeSet for error or completion.		
Type	R		

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
STATE	RESERVED		

Bits	Field Name	Description	Type	Reset
31:29	STATE	State of the RangeSet Request. Read 0x0: RangeSet is unallocated. Read 0x1: RangeSet allocated but not yet activated. Read 0x2: Reserved. Read 0x3: RangeSet is active, either sequencing through cache lines, awaiting completion of earlier RangeSets or awaiting processing resources. Read 0x4: Reserved	R	0x0

Bits	Field Name	Description	Type	Reset
		Read 0x5: Reserved Read 0x6: RangeSet operation completed without errors Read 0x7: RangeSet encountered an error. Processing of the RangeSet stops with the first error. It is reported as complete with error.		
28:0	RESERVED	Reserved	R	0x0000 0000

Table 4.28. Register Call Summary for Register CMURANGESTATE_i

Dual Cortex-A9 MPU Subsystem Register Manual
• CMU Register Summary:[0]

4.4.11. Local interconnect registers

4.4.11.1. Local interconnect Register Summary

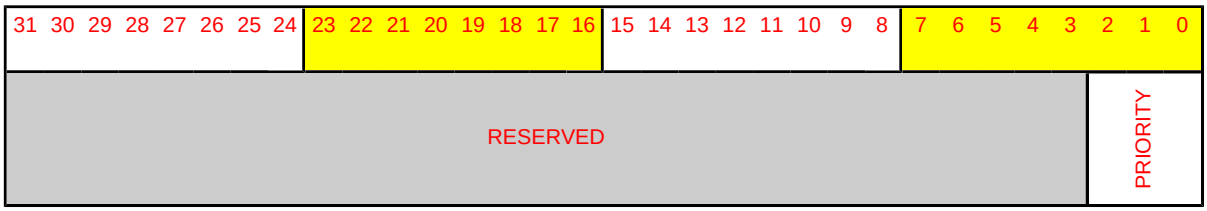
Table 4.29. Local interconnect Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	Local interconnect Base Address
MA_PRIORITY	RW	32	0x0000 0000	0x482A 2000

4.4.11.2. Local interconnect Register Description

Table 4.30. MA_PRIORITY

Address Offset	0x0000 0000		
Physical Address	Please refer toTable 4.29	**Instance**	Local interconnect
Description	Memory Adapter Priority Register. This register indicates the priority of memory access from MA to EMIF. This priority is used by EMIF in scheduling MA access to EMIF. 0x0 is lowest priority and 0x7 highest priority.		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:3	RESERVED	Reserved	RW	0x0000 0000
2:0	PRIORITY	MA priority value	RW	0x0

Table 4.31. Register Call Summary for Register MA_PRIORITY

Dual Cortex-A9 MPU Subsystem Register Manual
• Local interconnect Register Summary:[0]

4.4.12. MA registers

4.4.12.1. MA Register Summary

Table 4.32. MA Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	MA Base Address
RESERVED	R	32	0x0000 0010	0x482A F010
MA_LISA_LOCK	RW	32	0x0000 001C	0x482A F01C
MA_LISA_MAP_i[1]	RW	32	0x0000 0040 + (0x4 * i)	0x482A F040 + (0x4 * i)

1. i = 0 to 63

4.4.12.2. MA Register Description

For the registers description, see chapter 15.2 Dynamic Memory Manager, subsection 15.2.6 DMM Register Manual, where MA_LISA_LOCK corresponds to the DMM_LISA_LOCK register description, and MA_LISA_MAP_i corresponds to the DMM_LISA_MAP_i register description.

Chapter 5. DSP Subsystem

This chapter describes differences in the DSP Subsystem between the OMAP4430 Silicon Revision 2.x and OMAP4460 Silicon Revision 1.x multimedia devices.

Note

This chapter has not changed. Refer to OMAP4460 Silicon Revision 1.x TRM.

Chapter 6. IVA-HD Subsystem

This chapter describes the differences in the IVA-HD subsystem between the OMAP4430 Silicon Revision 2.x and OMAP4460 Silicon Revision 1.x multimedia devices.

Note

This chapter has not changed. Refer to OMAP4460 Silicon Revision 1.x TRM.

Chapter 7. Dual Cortex-M3 MPU Subsystem

This chapter describes the differences in the Dual Cortex-M3 MPU Subsystem between the OMAP4430 Silicon Revision 2.x and OMAP4460 Silicon Revision 1.x multimedia devices.

Note

This chapter has not changed. Refer to OMAP4460 Silicon Revision 1.x TRM.

Chapter 8. Imaging Subsystem

This chapter describes the differences in the Imaging Subsystem between the OMAP4430 Silicon Revision 2.x and OMAP4460 Silicon Revision 1.x multimedia devices.

8.1. ISS Overview

8.1.1. ISS Integration

- New 16 bit wide Parallel interface(CPI) along with PCLK, WEN, FLD, HS, and VS signals added to the ISS Interfaces.
  - List of registers impacted:
    - ISS_CTRL
    - ISS_CLKCTRL
    - ISS_CLKSTAT
- ISS SIMCOP Noise filter (NSF 2.0) throughput increased up to 120 Mpix/s;
- imaging accelerators (iMXs) clock frequency increased up to 400 MHz;
- Lens distortion correction (LDC) throughput increased up to 200 Mpix/s.

8.1.2. ISS Functional Description

Refer to OMAP4460 Silicon Revision 1.x TRM

8.1.3. ISS Register Manual

8.1.3.1. ISS Instance Summary

Table 8.1 is the ISS instance.

Table 8.1. ISS Instance Summary

Module Name	Module Base Address	Size
ISS_TOP	0x5200 0000	256 bytes

Note

This section contains only the ISS TOP registers. For more submodule register details, see the register manual of the particular submodule.

8.1.3.2. ISS Registers

8.1.3.2.1. ISS TOP Register Summary

Table 8.2 summarizes the ISS TOP register mapping.

Table 8.2. ISS TOP Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	ISS_TOP Base Address
ISS_HL_REVISION	R	32	0x0000 0000	0x5200 0000
RESERVED	R	32	0x0000 0004	0x5200 0004
ISS_HL_SYSCONFIG	RW	32	0x0000 0010	0x5200 0010
RESERVED	RW	32	0x0000 001C	0x5200 001C
ISS_HL_IRQSTATUS_RAW_i[1]	RW	32	0x0000 0020 + (0x10 * i)	0x5200 0020 + (0x10 * i)
ISS_HL_IRQSTATUS_i[1]	RW	32	0x0000 0024 + (0x10 * i)	0x5200 0024 + (0x10 * i)
ISS_HL_IRQENABLE_SET_i[1]	RW	32	0x0000 0028 + (0x10 * i)	0x5200 0028 + (0x10 * i)
ISS_HL_IRQENABLE_CLR_i[1]	RW	32	0x0000 002C + (0x10 * i)	0x5200 002C + (0x10 * i)

Register Name	Type	Register Width (Bits)	Address Offset	ISS_TOP Base Address
ISS_CTRL	RW	32	0x0000 0080	0x5200 0080
ISS_CLKCTRL	W	32	0x0000 0084	0x5200 0084
ISS_CLKSTAT	R	32	0x0000 0088	0x5200 0088
ISS_PM_STATUS	R	32	0x0000 008C	0x5200 008C

1. i = 0 to 5

8.1.3.2.2. ISS TOP Register Description

Note

This section contains only modified registers.

Table 8.3. ISS_CTRL

Address Offset	0x0000 0080		
Physical Address	SeeTable 8.2.	**Instance**	ISS_TOP
Description	ISS control register		
Type	RW		

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
CSI2_B_TAG_CNT	CSI2_A_TAG_CNT	CCP2W_TAG_CNT	CCP2R_TAG_CNT	RESERVED	ISS_CLK_DIV	INPUT_SEL	SYNC_DETECT

Bits	Field Name	Description	Type	Reset
31:28	CSI2_B_TAG_CNT	Defines the maximum number of tags that could be used by the CSI2 b write bridge. Note: Tag count must be set to 16 for best performance.	RW	0x0
27:24	CSI2_A_TAG_CNT	Defines the maximum number of tags that could be used by the CSI2 a write bridge. Note: Tag count must be set to 16 for best performance.	RW	0x0
23:20	CCP2W_TAG_CNT	Defines the maximum number of tags that could be used by the CCP2 write bridge Note: Tag count must be set to 16 for best performance.	RW	0x0
19:16	CCP2R_TAG_CNT	Defines the maximum number of tags that could be used by the CCP2 read bridge Note: Tag count must be set to 16 for best performance.	RW	0x0
15:6	RESERVED		R	0x000
5:4	ISS_CLK_DIV	ISS functional clock division CLK refers to the input clock provided to the ISS. FCLK is the functional clock provided to ISS top level and submodules. CFGCLK is the clock used for the configuration network. 0x0: FCLK=CLK CFGCLK=CLK/2 0x1: FCLK=CLK/2 CFGCLK=CLK/4 0x3: Reserved 0x2: FCLK=CLK/4 CFGCLK=CLK/8	RW	0x0

Bits	Field Name	Description	Type	Reset
3:2	INPUT_SEL	Selects ISP input 0x0: CSI2-A 0x1: CSI2-B 0x2: CCP2 0x3: Parallel interface	RW	0x0
1:0	SYNC_DETECT	Chooses among rising and falling edge for the HS_VS_IRQ synchronization event 0x0: HS falling edge 0x1: HS raising edge 0x3: VS raising edge 0x2: VS falling edge	RW	0x0

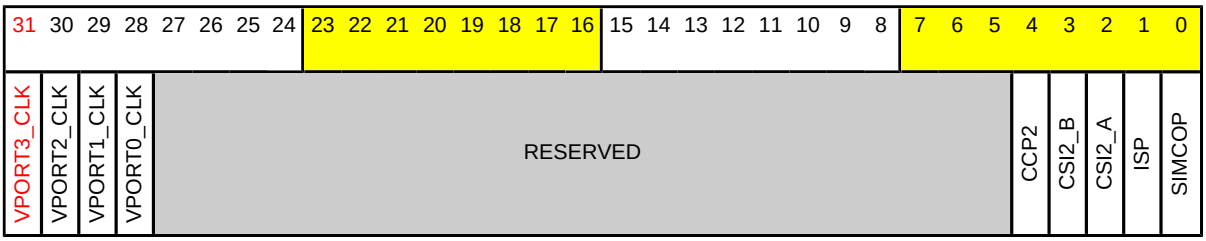
Table 8.4. Register Call Summary for Register ISS_CTRL

ISS Integration

- ISS Integration:[0]

Table 8.5. ISS_CLKCTRL

Address Offset	0x0000 0084		
Physical Address	SeeTable 8.2.	**Instance**	ISS_TOP
Description	ISS clock control register. Use to enable/disable the interface and functional clock of ISS submodules.		
Type	W		



Bits	Field Name	Description	Type	Reset
31	VPORT3_CLK	Enables the pixel clock from the parallel interface 0x0: Disabled 0x1: Enabled	RW	1
30	VPORT2_CLK	Enables the pixel clock from the CCP2 protocol engine 0x0: Disabled 0x1: Enabled	RW	1
29	VPORT1_CLK	Enables the pixel clock from the CSI2_B protocol engine 0x0: Disabled 0x1: Enabled	RW	1
28	VPORT0_CLK	Enables the pixel clock from the CSI2_A protocol engine 0x0: Disabled 0x1: Enabled	RW	1
27:5	RESERVED		R	0x000000
4	CCP2	CCP2 Write 0x0: Request shutdown of the submodule. No effect if the submodule clock is already off. Write 0x1: Request enable of the submodule.	W	0

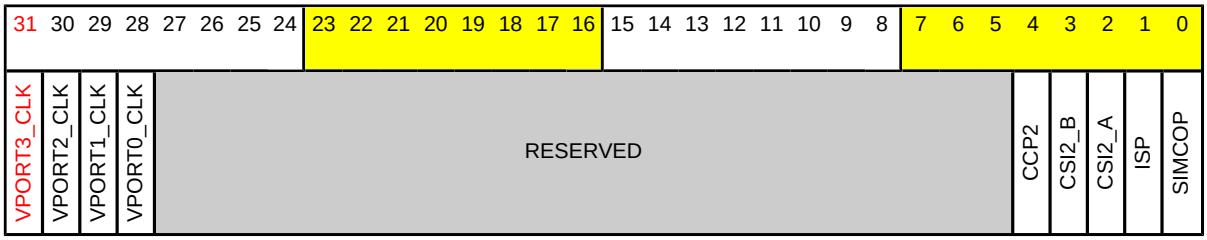
Bits	Field Name	Description	Type	Reset
		No effect if the submodule clock is already off.		
3	CSI2_B	CSI2_B Write 0x0: Request shutdown of the submodule. No effect if the submodule clock is already off. Write 0x1: Request enable of the submodule. No effect if the submodule clock is already off.	W	0
2	CSI2_A	CSI2_A Write 0x0: Request shutdown of the submodule. No effect if the submodule clock is already off. Write 0x1: Request enable of the submodule. No effect if the submodule clock is already off.	W	0
1	ISP	ISP Write 0x0: Request shutdown of the submodule. No effect if the submodule clock is already off. Write 0x1: Request enable of the submodule. No effect if the submodule clock is already off.	W	0
0	SIMCOP	SIMCOP Write 0x0: Request shutdown of the submodule. No effect if the submodule clock is already off. Write 0x1: Request enable of the submodule. No effect if the submodule clock is already off.	W	0

Table 8.6. Register Call Summary for Register ISS_CLKCTRL

ISS Integration
• ISS Integration:[0]

Table 8.7. ISS_CLKSTAT

Address Offset	0x0000 0088		
Physical Address	See Table 8.2.	**Instance**	ISS_TOP
Description	ISS clock status register.		
Type	R		



Bits	Field Name	Description	Type	Reset
31	VPORT3_CLK	Status of the pixel clock from the parallel interface Read 0x1: Enabled Read 0x0: Disabled	R	1
30	VPORT2_CLK	Status of the pixel clock from the CCP2 protocol engine Read 0x1: Enabled Read 0x0: Disabled	R	1
29	VPORT1_CLK	Status of the pixel clock from the CSI2_B protocol engine Read 0x1: Enabled Read 0x0: Disabled	R	1
28	VPORT0_CLK	Status of the pixel clock from the CSI2_A protocol engine	R	1

Bits	Field Name	Description	Type	Reset
		Read 0x1: Enabled Read 0x0: Disabled		
27:5	RESERVED		R	0x000000
4	CCP2	CCP2 Read 0x1: The submodule is on. Read 0x0: The submodule is off.	R	0
3	CSI2_B	CSI2_B Read 0x1: The submodule is on. Read 0x0: The submodule is off.	R	0
2	CSI2_A	CSI2_A Read 0x1: The submodule is on. Read 0x0: The submodule is off.	R	0
1	ISP	ISP Read 0x1: The submodule is on. Read 0x0: The submodule is off.	R	0
0	SIMCOP	SIMCOP Read 0x1: The submodule is on. Read 0x0: The submodule is off.	R	0

Table 8.8. Register Call Summary for Register ISS_CLKSTAT

ISS Integration

- ISS Integration:[0]

8.2. ISS Interfaces

8.2.1. ISS Interfaces Overview

Refer to OMAP4460 Silicon Revision 1.x TRM

8.2.2. ISS Interfaces Environment

Refer to OMAP4460 Silicon Revision 1.x TRM

8.2.3. ISS CSI2 PHY

Refer to OMAP4460 Silicon Revision 1.x TRM

8.2.4. ISS CCP2

Refer to OMAP4460 Silicon Revision 1.x TRM

8.2.5. ISS CSI2

8.2.5.1. ISS CSI2 Environment

- CSI2-B data lanes inreased from one to two in addition to the clock lane.
  - List of registers impacted:
    - CSI2_COMPLEXIO_CFG

8.2.5.2. ISS CSI2 Integration

Refer to OMAP4460 Silicon Revision 1.x TRM

8.2.5.3. ISS CSI2 Functional Description

Refer to OMAP4460 Silicon Revision 1.x TRM

8.2.5.4. ISS CSI2 Programming Model

Refer to OMAP4460 Silicon Revision 1.x TRM

8.2.5.5. ISS CSI2 Register Manual

8.2.5.5.1. ISS CSI2 Instance Summary

Table 8.9 summarizes the CSI2 instance.

Table 8.9. ISS CSI2 Instance Summary

Module Name	L3 Base Address	Size
ISS_CSI2_A_REGS1	0x5200 1000	368 bytes
ISS_CSI2_A_REGS2	0x5200 11C0	64 bytes
ISS_CSI2_B_REGS1	0x5200 1400	368 bytes
ISS_CSI2_B_REGS2	0x5200 15C0	64 bytes

8.2.5.5.2. ISS CSI2 REGS1 Registers

8.2.5.5.2.1. ISS CSI2 REGS1 Register Summary

Table 8.10 summarizes the CSI2 REGS1 registers.

Table 8.10. ISS CSI2 REGS1 Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	ISS_CSI2_A_REGS1 Base Address	ISS_CSI2_B_REGS1 Base Address
CSI2_REVISION	R	32	0x0000 0000	0x5200 1000	0x5200 1400
CSI2_SYSCONFIG	RW	32	0x0000 0010	0x5200 1010	0x5200 1410
CSI2_SYSSTATUS	R	32	0x0000 0014	0x5200 1014	0x5200 1414
CSI2_IRQSTATUS	RW	32	0x0000 0018	0x5200 1018	0x5200 1418
CSI2_IRQENABLE	RW	32	0x0000 001C	0x5200 101C	0x5200 141C
CSI2_CTRL	RW	32	0x0000 0040	0x5200 1040	0x5200 1440
CSI2_DBG_H	W	32	0x0000 0044	0x5200 1044	0x5200 1444
RESERVED	R	32	0x0000 0048	0x5200 1048	0x5200 1448
RESERVED	RW	32	0x0000 004C	0x5200 104C	0x5200 144C
CSI2_COMPLEXIO_CFG	RW	32	0x0000 0050	0x5200 1050	0x5200 1450
CSI2_COMPLEXIO_IRQSTATUS	RW	32	0x0000 0054	0x5200 1054	0x5200 1454
RESERVED	RW	32	0x0000 0058	0x5200 1058	0x5200 1458
CSI2_SHORT_PACKET	R	32	0x0000 005C	0x5200 105C	0x5200 145C
CSI2_COMPLEXIO_IRQENABLE	RW	32	0x0000 0060	0x5200 1060	0x5200 1460
RESERVED	RW	32	0x0000 0064	0x5200 1064	0x5200 1464
CSI2_DBG_P	W	32	0x0000 0068	0x5200 1068	0x5200 1468
CSI2_TIMING	RW	32	0x0000 006C	0x5200 106C	0x5200 146C
CSI2_CTX_CTRL1_i[1]	RW	32	0x0000 0070 + (0x20 * i)	0x5200 1070 + (0x20 * i)	0x5200 1470 + (0x20 * i)
CSI2_CTX_CTRL2_i[1]	RW	32	0x0000 0074 + (0x20 * i)	0x5200 1074 + (0x20 * i)	0x5200 1474 + (0x20 * i)

Register Name	Type	Register Width (Bits)	Address Offset	ISS_CSI2_A_REGS1 Base Address	ISS_CSI2_B_REGS1 Base Address
CSI2_CTX_DAT_OFST_i[1]	RW	32	0x0000 0078 + (0x20 * i)	0x5200 1078 + (0x20 * i)	0x5200 1478 + (0x20 * i)
CSI2_CTX_DAT_PING_ADDR_i[1]	RW	32	0x0000 007C + (0x20 * i)	0x5200 107C + (0x20 * i)	0x5200 147C + (0x20 * i)
CSI2_CTX_DAT_PONG_ADDR_i[1]	RW	32	0x0000 0080 + (0x20 * i)	0x5200 1080 + (0x20 * i)	0x5200 1480 + (0x20 * i)
CSI2_CTX_IRQENABLE_i[1]	RW	32	0x0000 0084 + (0x20 * i)	0x5200 1084 + (0x20 * i)	0x5200 1484 + (0x20 * i)
CSI2_CTX_IRQSTATUS_i[1]	RW	32	0x0000 0088 + (0x20 * i)	0x5200 1088 + (0x20 * i)	0x5200 1488 + (0x20 * i)
CSI2_CTX_CTRL3_i[1]	RW	32	0x0000 008C + (0x20 * i)	0x5200 108C + (0x20 * i)	0x5200 148C + (0x20 * i)

1. i = 0 to 7

8.2.5.5.2.2. ISS CSI2 REGS1 Register Description

Note

This section contains only modified registers.

Table 8.11. CSI2_COMPLEXIO_CFG

Address Offset	0x0000 0050
Physical Address	SeeTable 8.10.
Description	COMPLEXIO CONFIGURATION REGISTER for the complex I/O This register contains the lane configuration for the order and position of the lanes (clock and data) and the polarity order for the control of the PHY differential signals in addition to the control bit for the power FSM.
Type	RW

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	RESET_CTRL	RESET_DONE	PWR_CMD		PWR_STATUS		PWR_AUTO	RESERVED				DATA4_POL	DATA4_POSITION			DATA3_POL	DATA3_POSITION			DATA2_POL	DATA2_POSITION			DATA1_POL	DATA1_POSITION			CLOCK_POL	CLOCK_POSITION		

Bits	Field Name	Description	Type	Reset
31	RESERVED		R	0
30	RESET_CTRL	Controls the reset of the complex I/O 0x0: Complex I/O reset active. 0x1: Complex I/O reset deasserted.	RW	0
29	RESET_DONE	Internal reset monitoring of the power domain using the byte clock provided by the associated CSIPHY (see ,*ISS Clock Domains*. Read 0x1: Reset completed. Read 0x0: Internal module reset is on going.	R	0
28:27	PWR_CMD	Command for power control of the complex I/O 0x0: Command to change to OFF state 0x1: Command to change to ON state 0x2: Command to change to Ultralow-Power state	RW	0x0

Bits	Field Name	Description	Type	Reset
26:25	PWR_STATUS	Status of the power control of the complex I/O Read 0x2: Complex I/O in Ultralow-Power state Read 0x1: Complex I/O in ON state Read 0x0: Complex I/O in OFF state	R	0x0
24	PWR_AUTO	Automatic switch between ULP and ON states based on ULPM signals from complex I/O 0x0: Disable 0x1: Enable	RW	0
23:20	RESERVED		R	0x0
19	DATA4_POL	+/- differential pin order of data lane 4. 0x0: +/- pin order 0x1: -/+ pin order	RW	0
18:16	DATA4_POSITION	Position and order of the data lane 4. The values 6 and 7 are reserved. This lane is not available for C SI2-B receiver. 0x0 : This data lane is not used. 0x1 : Data lane 4 is at the position 1. This position is not available to the CSI2-B receiver 0x2 : Data lane 4 is at the position 2. This position is not available to the CSI2-B receiver. 0x3 : Data lane 4 is at the position 3. This position is not available to the CSI2-B receiver. 0x4 : Data lane 4 is at the position 4. This position is not available to the CSI2-B receiver. 0x5 : Data lane 4 is at the position 5. This position is not available to the CSI2-B receiver. 0x6 : RESERVED 0x7 : RESERVED	RW	0x0
15	DATA3_POL	+/- differential pin order of data lane 3. 0x0: +/- pin order 0x1: -/+ pin order	RW	0
14:12	DATA3_POSITION	Position and order of the data lane 3. The values 6 and 7 are reserved. This lane is not available for C SI2-B receiver. 0x0 : This data lane is not used. 0x1 : Data lane 3 is at the position 1. This position is not available to the CSI2-B receiver. 0x2 : Data lane 3 is at the position 2. This position is not available to the CSI2-B receiver. 0x3 : Data lane 3 is at the position 3. This position is not available to the CSI2-B receiver. 0x4 : Data lane 3 is at the position 4. This position is not available to the CSI2-B receiver. 0x5 : Data lane 3 is at the position 5. This position is not available to the CSI2-B receiver. 0x6 : RESERVED 0x7 : RESERVED	RW	0x0
11	DATA2_POL	+/- differential pin order of DATA lane 2. 0x0: +/- pin order (csi2_dx=+ and csi2_dy=-) 0x1: -/+ pin order (csi2_dx=- and csi2_dy=+)	RW	0
10:8	DATA2_POSITION	Position and order of the data lane 2. The values 6 and 7 are reserved.~~This lane is not available for C SI2-B receiver.~~ 0x0 : This data lane is not used.	RW	0x0

Bits	Field Name	Description	Type	Reset
		0x1 : Data lane 2 is at the position 1.~~This position is not available to the CSI2-B receiver.~~ 0x2 : Data lane 2 is at the position 2.~~This position is not available to the CSI2-B receiver.~~ 0x3 : Data lane 2 is at the position 3.~~This position is not available to the CSI2-B receiver.~~ 0x4 : Data lane 2 is at the position 4. This position is not available to the CSI2-B receiver. 0x5 : Data lane 2 is at the position 5. This position is not available to the CSI2-B receiver. 0x6 : RESERVED 0x7 : RESERVED		
7	DATA1_POL	+/- differential pin order of data lane 1. 0x0: +/- pin order (csi2_dx=+ and csi2_dy=-) 0x1: -/+ pin order (csi2_dx=- and csi2_dy=+)	RW	0
6:4	DATA1_POSITION	Position and order of the DATA lane 1. The values 6 and 7 are reserved. When CSI2 is used, data lane 1 position must be different from 0, 6, 7. 0x0 : This data lane is not used. 0x1 : Data lane 1 is at the position 1. 0x2 : Data lane 1 is at the position 2. 0x3 : Data lane 1 is at the position 3.~~This position is not available to the CSI2-B receiver.~~ 0x4 : Data lane 1 is at the position 4. This position is not available to the CSI2-B receiver. 0x5 : Data lane 1 is at the position 5. This position is not available to the CSI2-B receiver. 0x6 : RESERVED 0x7 : RESERVED	RW	0x0
3	CLOCK_POL	+/- differential pin order of clock lane. 0x0: +/- pin order (csi2_dx=+ and csi2_dy=-) 0x1: -/+ pin order (csi2_dx=- and csi2_dy=+)	RW	0
2:0	CLOCK_POSITION	Position and order of the clock lane. The values 5, 6 and 7 are reserved. When CSI2 is used, clock l ane position must be different from 0, 5, 6, 7. 0x0 : This data lane is not used. 0x1 : Clock lane is at position 1. 0x2 : Clock lane is at position 2. 0x3 : Clock lane is at position 3.~~This position is not available to the CSI2-B receiver.~~ 0x4 : Clock lane is at position 4. This position is not available to the CSI2-B receiver. 0x5 : RESERVED 0x6 : RESERVED 0x7 : RESERVED	RW	0x0

Table 8.12. Register Call Summary for Register CSI2_COMPLEXIO_CFG

ISS CSI2 Environment

- ISS CSI2 Environment:[0]

8.2.5.5.3. ISS CSI2 REGS2 Registers

Refer to OMAP4460 Silicon Revision 1.x TRM

8.2.6. ISS TCTRL

8.2.6.1. ISS TCTRL Environment

Refer to OMAP4460 Silicon Revision 1.x TRM

8.2.6.2. ISS TCTRL Integration

- VS signal from the Parallel interface (CPI) added to the mux input (CAMEVT2)
  - List of registers impacted:
    - TCTRL_CTRL

8.2.6.3. ISS TCTRL Functional Description

Refer to OMAP4460 Silicon Revision 1.x TRM

8.2.6.4. ISS TCTRL Programming Model

Refer to OMAP4460 Silicon Revision 1.x TRM

8.2.6.5. ISS TCTRL Register Manual

8.2.6.5.1. ISS TCTRL Instance Summary

Table 8.13 summarizes the TCTRL instance

Table 8.13. ISS TCTRL Instance Summary

Module Name	L3 Base Address	Size
ISS_TCTRL	0x5200 0400	256 bytes

8.2.6.5.2. ISS TCTRL Registers

8.2.6.5.2.1. ISS TCTRL Register Summary

Table 8.14 summarizes the TCTRL registers.

Table 8.14. ISS TCTRL Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	ISS_TCTRL Base Address
TCTRL_REVISION	R	32	0x0000 0000	0x5200 0400
TCTRL_SYSCONFIG	RW	32	0x0000 0004	0x5200 0404
TCTRL_SYSSTATUS	R	32	0x0000 0008	0x5200 0408
TCTRL_STRB_LEN-GTH	RW	32	0x0000 0010	0x5200 0410
TC-TRL_PSTRB_LENGTH	RW	32	0x0000 0014	0x5200 0414
TCTRL_SHUT_LEN-GTH	RW	32	0x0000 0018	0x5200 0418
TCTRL_GRES-ET_LENGTH	RW	32	0x0000 001C	0x5200 041C
TCTRL_STRB_DELAY	RW	32	0x0000 0020	0x5200 0420
TC-TRL_PSTRB_DELAY	RW	32	0x0000 0024	0x5200 0424
TCTRL_SHUT_DELAY	RW	32	0x0000 0028	0x5200 0428
TCTRL_CTRL	RW	32	0x0000 0030	0x5200 0430
TCTRL_PSTRB_RE-PLAY	RW	32	0x0000 0034	0x5200 0434
TCTRL_FRAME	RW	32	0x0000 0038	0x5200 0438

8.2.6.5.2.2. ISS TCTRL Register Description

Note

This section contains only modified registers.

Table 8.15. TCTRL_CTRL

Address Offset	0x0000 0030		
Physical Address	See Table 8.14.	**Instance**	ISS_TCTRL
Description	TIMING CONTROL - CONTROL REGISTER		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GRESETDIR	GRESETPOL	GRESETEN	INSEL		STRBPSTRBPOL	RESERVED	SHUTPOL	STRBEN	PSTRBEN	SHUTEN	RESERVED					DIVC								RESERVED							

Bits	Field Name	Description	Type	Reset
31	GRESETDIR	Sets the direction of the GLOBAL_RESET signal. 0x0: INPUT - GLOBAL_RESET is an input to the TIMING CONTROL module. GLOBAL_RESET is externally generated. 0x1: OUTPUT - GLOBAL_RESET is an output of the TIMING CONTROL module. GLOBAL_RESET is internally generated. If GRESETEN is set to 1, the internally generated GLOBAL_RESET will trigger the generation of the PRESTROBE, STROBE and SHUTTER signals. The frame counters are ignored.	RW	0
30	GRESETPOL	Sets the polarity of the global reset signal: CAM_GLOBAL_RESET. It applies whatever the direction of the GLOBAL_RESET signal: input or output. 0x0: active high 0x1: active low	RW	0
29	GRESETEN	Triggers the generation of the CAM_GLOBAL_RESET signal. The signal is asserted immediately. If enabled, the CAM_GLOBAL_RESET signal will be asserted for TCTRL_GRESET_LENGTH cycles. After the signal assertion, the enable bit is automatically cleared to 0. The polarity of the GLOBAL_RESET signal is set with TCTRL_CTRL.GRESETPOL. Enabling this bit triggers the generation of the CAM_SHUTTER and CAM_STROBE signals (if previously enabled). The frame counters shall be set to 0 when this bit is set to 1 and GRESETDIR is set a OUTPUT.	RW	0
28:27	INSEL	Sets the mode that will trigger the SHUTTER, PRE STROBE and STROBE signals. 0x0: Synchronization event from camera 0 0x1: Synchronization event from camera 1 0x3: GRESET - The CAM_GLOBAL_RESET input signal will trigger the SHUTTER, PRESTROBE and STROBE signals. In this mode, there are no frame	RW	0x0

Bits	Field Name	Description	Type	Reset
		counters. The delay counters start decrementing as soon as the GLOBAL_RESET signal is asserted. The polarity of the GLOBAL_RESET signal is set withTCTRL_CTRL.GRESETPOL. 0x2: Synchronization event from camera 2(serial interfaces muxed with the camera Parallel interface (CPI))		
26	STRBPSTRBPOL	Sets the polarity of the strobe and prestrobe signals. 0x0: Active high 0x1: Active low	RW	0
25	RESERVED		R	0
24	SHUTPOL	Sets the polarity of the mechanical shutter signal: CAM_SHUTTER 0x0: Active high 0x1: Active low	RW	0
23	STRBEN	Flash strobe signal enable. If enabled, the STROBE signal will be asserted after TCTRL_FRAME.STRB frames have been received and a delay of TCTRL_STRB_DELAY cycles have passed. The STROBE signal is asserted for TCTRL_STRB_LENGTH cycles. After the signal assertion, the enable bit is automatically cleared to 0. This signal shall not be disabled by software.	RW	0
22	PSTRBEN	Flash prestrobe signal enable. If enabled, the PRESTROBE signal will be asserted after TCTRL_FRAME.PSTRB frames have been received and a delay of TCTRL_PSTRB_DELAY cycles have passed. The PRESTROBE signal is asserted for TCTRL_PSTRB_LENGTH cycles. After the signal assertion, the enable bit is automatically cleared to 0. This signal shall not be disabled by software.	RW	0
21	SHUTEN	Mechanical shutter signal enable. If enabled, the SHUTTER signal will be asserted after TCTRL_FRAME.SHUT frames have been received and a delay of TCTRL_SHUT_DELAY cycles have passed. The SHUTTER signal is asserted for TCTRL_SHUT_LENGTH cycles. After the signal assertion, the enable bit is automatically cleared to 0. This signal shall not be disabled by software.	RW	0
20:19	RESERVED		R	0x0
18:10	DIVC	Sets the clock divisor value for the CNTCLK clock generation based on the CLK input clock. CNTCLK is an internal clock used by the TIMING CTRL module counters. Usually, CNTCLK = CLK / DIVC, except for some particular values shown hereafter. 0x0: No clock. CNTCLK is gated.	RW	0x000
9:0	RESERVED		R	0x000

Table 8.16. Register Call Summary for Register TCTRL_CTRL

ISS TCTRL Integration
• ISS TCTRL Integration:[0]
ISS TCTRL Register Manual
• ISS TCTRL Register Description:[1][2]

8.2.7. ISS BTE

Refer to OMAP4460 Silicon Revision 1.x TRM

8.2.8. ISS CBUFF

Refer to OMAP4460 Silicon Revision 1.x TRM

8.3. ISS ISP

8.3.1. ISS ISP Overview

Refer to OMAP4460 Silicon Revision 1.x TRM

8.3.2. ISS ISP Integration

Refer to OMAP4460 Silicon Revision 1.x TRM

8.3.3. ISS ISP Functional Description

8.3.3.1. ISS ISP VP Functional Description

Refer to OMAP4460 Silicon Revision 1.x TRM

8.3.3.2. ISS ISP PG Functional Description

Refer to OMAP4460 Silicon Revision 1.x TRM

8.3.3.3. ISS ISP IPIPEIF Functional Description

Refer to OMAP4460 Silicon Revision 1.x TRM

8.3.3.4. ISS ISP IPIPE Functional Description

Refer to OMAP4460 Silicon Revision 1.x TRM

8.3.3.5. ISS ISP RSZ Functional Description

Refer to OMAP4460 Silicon Revision 1.x TRM

8.3.3.6. ISS ISP H3A Functional Description

Refer to OMAP4460 Silicon Revision 1.x TRM

8.3.3.7. ISS ISP ISIF Functional Description

- New functionality for Interlaced video configuration added when data received by CPI and outputted to SDRAM via ISIF.
  - List of registers impacted:
    - ISIF_SLV0
    - ISIF_SLV1
    - ISIF_SDOFST
  - ISIF_MODESET[15] MDFS
  - ISIF_MODESET[4] FIPOL

8.3.3.8. ISS ISP BL Functional Description

Refer to OMAP4460 Silicon Revision 1.x TRM

8.3.3.9. ISS ISP Memory Mapping

Refer to OMAP4460 Silicon Revision 1.x TRM

8.3.4. ISS ISP Programming Model

Refer to OMAP4460 Silicon Revision 1.x TRM

8.3.5. ISS ISP Register Manual

8.3.5.1. ISS ISP Instance Summary

Table 8.17. ISS ISP Instance Summary

Module Name	Module Base Address	Size
ISS_ISP5_SYS1	0x5201 0000	160 bytes
ISS_ISP5_SYS2	0x5201 00A0	864 bytes
ISS_RESIZER	0x5201 0400	1KB
ISS_IPIPE	0x5201 0800	2KB
ISS_ISIF	0x5201 1000	512 bytes
ISS_IPIPEIF	0x5201 1200	128 bytes
ISS_H3A	0x5201 1400	512 bytes

8.3.5.2. ISS ISP5 SYS1 Registers

Refer to OMAP4460 Silicon Revision 1.x TRM

8.3.5.3. ISS ISP5 SYS2 Registers

Refer to OMAP4460 Silicon Revision 1.x TRM

8.3.5.4. ISS RESIZER Registers

Refer to OMAP4460 Silicon Revision 1.x TRM

8.3.5.5. ISS IPIPE registers

Refer to OMAP4460 Silicon Revision 1.x TRM

8.3.5.6. ISS ISIF Registers

8.3.5.6.1. ISS ISIF Register Summary

Table 8.18. ISS ISIF Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	ISS_ISIF Base Address
ISIF_SYNCEN	RW	32	0x0000 0000	0x5201 1000
ISIF_MODESET	RW	32	0x0000 0004	0x5201 1004
ISIF_HDW	RW	32	0x0000 0008	0x5201 1008
ISIF_VDW	RW	32	0x0000 000C	0x5201 100C
ISIF_PPLN	RW	32	0x0000 0010	0x5201 1010

Register Name	Type	Register Width (Bits)	Address Offset	ISS_ISIF Base Address
ISIF_LPFR	RW	32	0x0000 0014	0x5201 1014
ISIF_SPH	RW	32	0x0000 0018	0x5201 1018
ISIF_LNH	RW	32	0x0000 001C	0x5201 101C
~~RESERVED~~ISIF_SLV0	RW	32	0x0000 0020	0x5201 1020
~~RESERVED~~ISIF_SLV1	RW	32	0x0000 0024	0x5201 1024
ISIF_LNV	RW	32	0x0000 0028	0x5201 1028
ISIF_CULH	RW	32	0x0000 002C	0x5201 102C
ISIF_CULV	RW	32	0x0000 0030	0x5201 1030
ISIF_HSIZE	RW	32	0x0000 0034	0x5201 1034
~~RESERVED~~ISIF_SDOFST	RW	32	0x0000 0038	0x5201 1038
...	...	...	...	...

8.3.5.6.2. ISS ISIF Register Description

Note

This section contains only modified registers.

Table 8.19. ISIF_MODESET

Address Offset	0x0000 0004		
Physical Address	0x5201 1004	**Instance**	ISS_ISIF
Description			
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																~~RESERVED~~MDFS	HLPF	INPMOD		OVF	CCDW			CCDMD	DPOL	SWEN	RESERVED	HDPOL	VDPOL	FIDD	HDVDD

Bits	Field Name	Description	Type	Reset
31:16	RESERVED	Reserved.	R	0x0000
15	~~RESERVED~~MDFS	~~Read returns reset value~~Field Status This bit indicates the status of the current FLD signal when the ISIF module is in interlaced mode. Read 0x1: Even field Read 0x0: Odd field	R	0
14	HLPF	Low pass filter enable. When this bit is enabled, a 3-tap (1/4 + 1/2 Z^{-2}+ 1/4 Z^{4}) filtering process is performed on the sensor data. 0x0: Disable 0x1: Enable	RW	0
13:12	INPMOD	Data input mode: 0x0: RAW data 0x1: YCbCr 16bit 0x3: Reserved 0x2: YCbCr 8bit	RW	0x2
11	OVF	ISIF module write port overflow status bit	RW	0

Bits	Field Name	Description	Type	Reset
		If the write port of the ISIF module overflows when writing data to SDRAM, this bit will toggle. 0x0: No overflow pending (r) No action (w) 0x1: Overflow pending (r) Clear overflow (w)		
10:8	CCDW	This bit enables to shift right (divide) the up-to-12-bi t RAW data value when writing out to SDRAM. The effect is that the dynamic of the output signal is d ecreased. TheISIF_MODESET.CCDW, ISIF_HSIZE.ADCR, ISIF_HSIZE.HSIZE, ISIF_CCD-CFG.BSWD, ISIF_CCDCFG.MSBINV, ISIF_CCDCFG.SDRPACK bit fields control how pixel data are stored to SDRAM. 0x6: Reserved 0x1: 1-bit right shift out[15:0] = 00000 data[11:1] 0x7: Reserved 0x0: No shift out[15:0] = 0000 data[11:0] 0x2: 2-bit right shift out[15:0] = 000000 data[11:2] 0x4: 4-bit right shift out[15:0] = 00000000 data[11:4] 0x5: Reserved 0x3: 3-bit right shift out[15:0] = 0000000 data[11:3]	RW	0x0
7	CCDMD	Field mode: This bit selects the type of image sensor: interlaced or progressive 0x0: Progressive image sensor 0x1: Interlaced image sensor	RW	0
6	DPOL	Image sensor input data polarity 0x0: No change 0x1: One's complement	RW	0
5	SWEN	External WEN selection In case this bit and SYNCEN.DWEN are set to 1, t he external WEN signal is used to store image se nsor data to memory. 0x0: WEN not used 0x1: Use external WEN	RW	0
4	~~RESERVED~~FIPOL	~~Read returns reset value~~FLD Signal Polarity 0x0: Positive 0x1: Negative	RW	0
3	HDPOL	HD Sync Signal Polarity 0x0: Positive 0x1: Negative	RW	0
2	VDPOL	VD Sync Signal Polarity 0x0: Positive 0x1: Negative	RW	0
1	FIDD	FLD Signal Direction. There must be at least three clock cycles between the time this bit is modified and the HD/VD pulse for the start of frame comes. 0x0: Input	RW	0

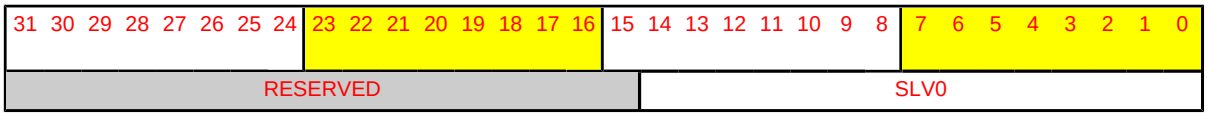
Bits	Field Name	Description	Type	Reset
		0x1: Output		
0	HDVDD	VD,HD Sync Signal Direction. There must be at least three clock cycles between the time this bit is modified and the HD/VD pulse for the start of frame comes. 0x0: Input 0x1: Output	RW	0

Table 8.20. Register Call Summary for Register ISIF_MODESET

ISS ISP Functional Description
• ISS ISP ISIF Functional Description:[0][1]
ISS ISP Register Manual
• ISS ISIF Register Description:[2]

Table 8.21. ISIF_SLV0

Address Offset	0x0000 0020		
Physical Address	0x5201 1020	**Instance**	ISS_ISIF
Description	SDRAM output vertical field 0 start line control		
Type	RW		



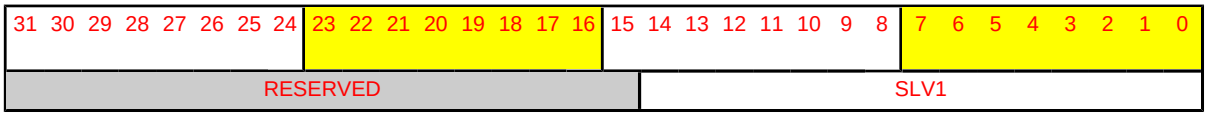
Bits	Field Name	Description	Type	Reset
31:15	RESERVED	Reserved	R	0x0000
14:0	SLV0	Start Line, Vertical (Field 0) Sets line at which data output to SDRAM will begin, measured from the start of VD *This bit field is latched by VD.	RW	0x0000

Table 8.22. Register Call Summary for Register ISIF_SLV0

ISS ISP Functional Description
• ISS ISP ISIF Functional Description:[0]

Table 8.23. ISIF_SLV1

Address Offset	0x0000 0024		
Physical Address	0x5201 1024	**Instance**	ISS_ISIF
Description	SDRAM output vertical field 1 start line control		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:15	RESERVED		R	0x0000
14:0	SLV1	Start Line, Vertical (Field 1) Sets line at which data output to SDRAM will begin, measured from the start of VD *This bit field is latched by VD.	RW	0x0000

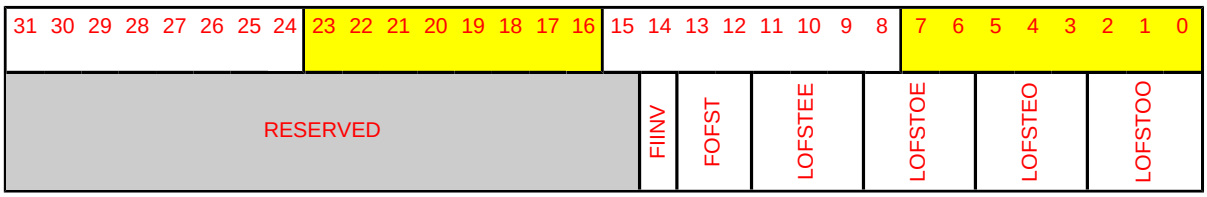
Table 8.24. Register Call Summary for Register ISIF_SLV1

ISS ISP Functional Description

- ISS ISP ISIF Functional Description:[0]

Table 8.25. ISIF_SDOFST

Address Offset	0x0000 0024		
Physical Address	0x5201 1038	**Instance**	ISS_ISIF
Description	SDRAM output control register		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:15	RESERVED	Reserved	R	0x0000
14	FIINV	FID polarity: This bit inverse a FID polarity. 0x0: No change 0x1: Inverse FID	RW	0x0
13:12	FOFST	Field line offset value in odd (FID = 1) field 0x0: +1 line 0x1: +2 lines 0x3: +4 lines 0x2: +3 lines	RW	0x0
11:9	LOFSTEE	Field line offset value in even line, even field 0x0: +1 line 0x1: +2 lines 0x2: +3 lines 0x3: +4 lines 0x4: - 1 line 0x5: - 2 lines 0x6: - 3 lines 0x7: - 4 lines	RW	0x0

Bits	Field Name	Description	Type	Reset
8:6	LOFSTOE	Field line offset value in odd line, even field 0x0: +1 line 0x1: +2 lines 0x2: +3 lines 0x3: +4 lines 0x4: - 1 line 0x5: - 2 lines 0x6: - 3 lines 0x7: - 4 lines	RW	0x0
5:3	LOFSTEO	Field line offset value in even line, odd field 0x0: +1 line 0x1: +2 lines 0x2: +3 lines 0x3: +4 lines 0x4: - 1 line 0x5: - 2 lines 0x6: - 3 lines 0x7: - 4 lines	RW	0x0
2:0	LOFSTOO	Field line offset value in odd line, odd field 0x0: +1 line 0x1: +2 lines 0x2: +3 lines 0x3: +4 lines 0x4: - 1 line 0x5: - 2 lines 0x6: - 3 lines 0x7: - 4 lines	RW	0x0

Table 8.26. Register Call Summary for Register ISIF_SDOFST

ISS ISP Functional Description

- ISS ISP ISIF Functional Description:[0]

8.3.5.7. ISS IPIPEIF Registers

Refer to OMAP4460 Silicon Revision 1.x TRM

8.3.5.8. ISS H3A Registers

Refer to OMAP4460 Silicon Revision 1.x TRM

8.4. ISS Still Image Coprocessor

8.4.1. ISS SIMCOP Overview

Increased functional clock frequency for LDS, iMX and NSF modules. This change affects the following registers:

- SIMCOP_HL_HWINFO
- SIMCOP_CLKCTRL

8.4.1.1. ISS SIMCOP Integration

Refer to OMAP4460 Silicon Revision 1.x TRM.

8.4.1.2. ISS SIMCOP Functional Description

Refer to OMAP4460 Silicon Revision 1.x TRM.

8.4.1.3. ISS SIMCOP Programming Models

Refer to OMAP4460 Silicon Revision 1.x TRM.

8.4.1.4. ISS SIMCOP Register Manual

8.4.1.4.1. SIMCOP Instance Summary

Refer to OMAP4460 Silicon Revision ES1.x TRM.

8.4.1.4.2. SIMCOP Registers

8.4.1.4.2.1. SIMCOP Register Summary

Table 8.27. SIMCOP _CONTROL Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	Physical Address L3 Interconnect	Physical Address Cortex-M3 Private Access
SIMCOP_HL_REVISION	R	32	0x0000 0000	0x5202 0000	0x5506 0000
SIMCOP_HL_HWINFO	R	32	0x0000 0004	0x5202 0004	0x5506 0004
SIMCOP_HL_SYSCONFIG	RW	32	0x0000 0010	0x5202 0010	0x5506 0010
RESERVED	R	32	0x0000 001C	0x5202 001C	0x5506 001C
SIMCOP_HL_IRQSTATUS_RAW_i[1]	RW	32	0x0000 0020 + (0x10 * i)	0x5202 0020 + (0x10 * i)	0x5506 0020 + (0x10 * i)
SIMCOP_HL_IRQSTATUS_i[1]	RW	32	0x0000 0024 + (0x10 * i)	0x5202 0024 + (0x10 * i)	0x5506 0024 + (0x10 * i)
SIMCOP_HL_IRQENABLE_SET_i[1]	RW	32	0x0000 0028 + (0x10 * i)	0x5202 0028 + (0x10 * i)	0x5506 0028 + (0x10 * i)
SIMCOP_HL_IRQENABLE_CLR_i[1]	RW	32	0x0000 002C + (0x10 * i)	0x5202 002C + (0x10 * i)	0x5506 002C + (0x10 * i)
SIMCOP_CTRL	RW	32	0x0000 0060	0x5202 0060	0x5506 0060
SIMCOP_CLKCTRL	RW	32	0x0000 0064	0x5202 0064	0x5506 0064

1. i = 0 to 3

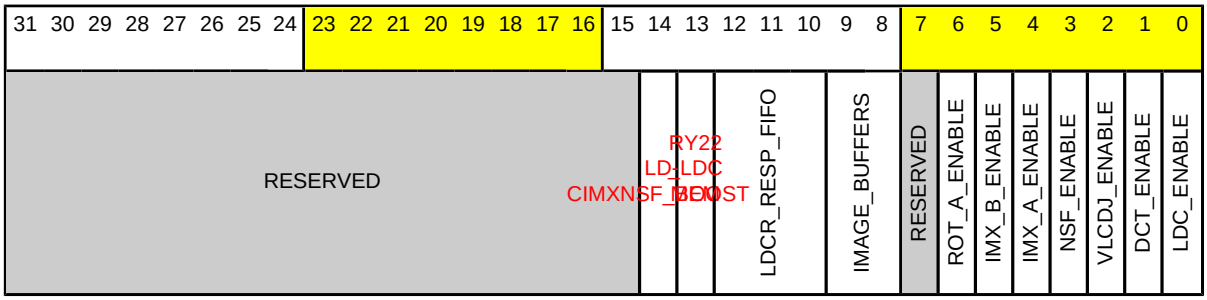
8.4.1.4.2.2. SIMCOP_CONTROL Register Descriptions

Note

This section contains only modified registers.

Table 8.28. SIMCOP_HL_HWINFO

Address Offset	0x0000 0004		
Physical Address	0x5202 0004 0x5506 0004	**Instance**	SIMCOP_CONTROL_L3 SIMCOP_CONTROL_CORTEX-M3
Description			
Type	RW		



Bits	Field Name	Description	Type	Reset
31:~~13~~15	RESERVED	Read returns 0.	R	0x00000
14	LDCIMXNSF_BOOST	Read 0x1: SIMCOP receives a 400 MHz clock. S ome modules receive the 400 Mhz clock and ot hers receive 400/2=200 Mhz Read 0x0: SIMCOP receives a 200 MHz clock dr iving all sub-modules	R	0x1
13	RY22_LDCMEM	Chooses the LDC working memory configuration Read 0x1: Working memory only populated for YUV420 operation A: 1024x32 B: 1024x32 C: 1024x16 D: 1024x16 Read 0x0: Working memory fully populated. Supports YUV422 operation. A: 512x32 B: 512x32 C: 1024x16 D: 1024x16 E: 512x32 F: 512x32 G: 1024x16 H: 1024x16	R	0x0
12:10	LDCR_RESP_FIFO	Defines the size of the LDC read master response FIFO in words of 128-bits. Read 0x2: 8x128 bits Read 0x3: 16x128 bits Read 0x4: 32x128 bits Read 0x5: 64x128 bits Read 0x6: 128x128 bits Read 0x7: 256x256 bits	R	0x4
9:8	IMAGE_BUFFERS	This parameter defines the image buffer count. Read 0x0: 4 Image buffers (e, f, g, h) Read 0x1: 8 Image buffers	R	0x1
7	RESERVED	Read returns 0.	R	0
6	ROT_A_ENABLE	The ROT a is present when this parameter is set. Read 0x0: Disabled at design time Read 0x1: Enabled at design time	R	1
5	IMX_B_ENABLE	The iMX B module and the CMD b, COEFF b memories are present when this parameter is set. Read 0x0: Disabled at design time Read 0x1: Enabled at design time	R	1
4	IMX_A_ENABLE	The iMX A module and the CMD a, COEFF a memories are present when this parameter is set. Read 0x0: Disabled at design time Read 0x1: Enabled at design time	R	1
		The NSF2 is present when this parameter is set.		

Bits	Field Name	Description	Type	Reset
3	NSF_ENABLE	Read 0x0: Disabled at design time Read 0x1: Enabled at design time	R	1
2	VLCDJ_ENABLE	The VLCD module and the QUANT, HUFFMAN, BITSTREAM memories are present when this parameter is set. Read 0x0: Disabled at design time Read 0x1: Enabled at design time	R	1
1	DCT_ENABLE	The DCT module is present when this parameter is set. Read 0x0: Disabled at design time Read 0x1: Enabled at design time	R	1
0	LDC_ENABLE	The LDC module and the LDC LUT are present w hen this parameter is set. Read 0x0: Disabled at design time Read 0x1: Enabled at design time	R	1

Table 8.29. SIMCOP_CLKCTRL

Address Offset	0x0000 0064		
Physical Address	0x5202 0064 0x5506 0064	**Instance**	SIMCOP_CONTROL_L3 SIMCOP_CON-TROL_CORTEX-M3
Description	SIMCOP clock control register. Use to enable/disable the interface and functional clock of SIMCOP submodules. Disabled modules cannot be accessed		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								LDCIMXNSF_BOOST	ROT_A	IMX_B	IMX_A	NSF2	VLCDJ	DCT	LDC	DMA

Bits	Field Name	Description	Type	Reset
31:89	RESERVED	Read returns 0.	R	0x000000
8	LDCIMXNSF_BOOST	Controls the processing speed of the LDC, iMX #a , iMX #b and NSF2 modules as well as the clock of the attached memories 0x0: Functional clock = OCP clock 0x1: Functional clock = 2x OCP clock	RW	0x0
7	ROT_A	ROT A Write 0x0: Request shutdown of the submodule. No effect if the submodule clock is already off. Read 0x0: The submodule is off Read 0x1: The submodule is on Write 0x1: Request enable of the submodule. No e ffect if the submodule clock is already off.	RW	0
6	IMX_B	iMX B Write 0x0: Request shutdown of the submodule. No effect if the submodule clock is already off. Read 0x0: The submodule is off. Read 0x1: The submodule is on. Write 0x1: Request enable of the submodule. No e ffect if the submodule clock is already off.	RW	0
5	IMX_A	iMX A Write 0x0: Request shutdown of the submodule. No effect if the submodule clock is already off.	RW	0

Bits	Field Name	Description	Type	Reset
		Read 0x0: The submodule is off. Read 0x1: The submodule is on. Write 0x1: Request enable of the submodule. No effect if the submodule clock is already off.		
4	NSF2	NSF2 Write 0x0: Request shutdown of the submodule. No effect if the submodule clock is already off. Read 0x0: The submodule is off. Read 0x1: The submodule is on. Write 0x1: Request enable of the submodule. No effect if the submodule clock is already off.	RW	0
3	VLCDJ	VLCDJ Write 0x0: Request shutdown of the submodule. No effect if the submodule clock is already off. Read 0x0: The submodule is off. Read 0x1: The submodule is on. Write 0x1: Request enable of the submodule. No effect if the submodule clock is already off.	RW	0
2	DCT	DCT Write 0x0: Request shutdown of the submodule. No effect if the submodule clock is already off. Read 0x0: The submodule is off. Read 0x1: The submodule is on. Write 0x1: Request enable of the submodule. No effect if the submodule clock is already off.	RW	0
1	LDC	LDC Write 0x0: Request shutdown of the submodule. No effect if the submodule clock is already off. Read 0x0: The submodule is off. Read 0x1: The submodule is on. Write 0x1: Request enable of the submodule. No effect if the submodule clock is already off.	RW	0
0	DMA	DMA Write 0x0: Request shutdown of the submodule. No effect if the submodule clock is already off. Read 0x0: The submodule is off. Read 0x1: The submodule is on. Write 0x1: Request enable of the submodule. No effect if the submodule clock is already off.	RW	0

8.4.1.5. ISS SIMCOP Memory Mapping

Refer to OMAP4460 Silicon Revision 1.x TRM.

8.4.2. ISS SIMCOP Hardware Sequencer and Buffers

Refer to OMAP4460 Silicon Revision 1.x TRM

8.4.3. ISS SIMCOP DMA Module

Refer to OMAP4460 Silicon Revision 1.x TRM

8.4.4. ISS SIMCOP LDC Module

Refer to OMAP4460 Silicon Revision 1.x TRM

8.4.5. ISS SIMCOP Discrete Cosine Transform Module

Refer to OMAP4460 Silicon Revision 1.x TRM.

8.4.6. ISS SIMCOP Variable Length Coder/Decoder for JPEG Module

Refer to OMAP4460 Silicon Revision 1.x TRM.

8.4.7. ISS SIMCOP Rotation Accelerator Module

Refer to OMAP4460 Silicon Revision 1.x TRM.

Chapter 9. Face Detect

This chapter describes the differences in the Face Detect between the OMAP4430 Silicon Revision 2.x and OMAP4460 Silicon Revision 1.x multimedia devices.

Note

This chapter has not changed. Refer to OMAP4460 Silicon Revision 1.x TRM.

Chapter 10. Display Subsystem

This chapter describes the differences in the Display Subsystem between OMAP4430 Silicon Revision 2.x and OMAP4460 Silicon Revision 1.x multimedia devices.

10.1. Display Subsystem Overview

Support for the 1080p@24Hz 3D Stereoscopic frame-packing format of HDMI v1.4 standard is added.

The Video DAC (VDAC) functionality is not supported.

10.2. Display Controller

10.2.1. Display Controller Overview

Refer to OMAP4460 Silicon Revision 1.x TRM.

10.2.2. Display Controller Environment

Refer to OMAP4460 Silicon Revision 1.x TRM.

10.2.3. Display Controller Integration

Refer to OMAP4460 Silicon Revision 1.x TRM.

10.2.4. Display Controller Functional Description

10.2.4.1. Clock configuration

Refer to OMAP4460 Silicon Revision 1.x TRM.

10.2.4.2. Software Reset

Refer to OMAP4460 Silicon Revision 1.x TRM.

10.2.4.3. Power Management

Refer to OMAP4460 Silicon Revision 1.x TRM.

10.2.4.4. Interrupt Request

Refer to OMAP4460 Silicon Revision 1.x TRM.

10.2.4.5. System DMA Request

Refer to OMAP4460 Silicon Revision 1.x TRM.

10.2.4.6. DMA Engine

Refer to OMAP4460 Silicon Revision 1.x TRM.

10.2.4.7. Rotation and Mirroring

Refer to OMAP4460 Silicon Revision 1.x TRM.

10.2.4.8. Memory Format

Refer to OMAP4460 Silicon Revision 1.x TRM.

10.2.4.9. Graphics Pipeline

Refer to OMAP4460 Silicon Revision 1.x TRM.

10.2.4.10. Video Pipelines

Refer to OMAP4460 Silicon Revision 1.x TRM.

10.2.4.11. Write-back Pipeline

Refer to OMAP4460 Silicon Revision 1.x TRM.

10.2.4.12. LCD Outputs

The usage of DISPC_VID2_ATTRIBUTES[31:30] CHANNELOUT2 register bit-field is changed to support 1080p HDMI 3D format on the TV output.

10.2.4.13. TV Output

Configuration details on the TV output settings for 1080p HDMI 3D format are added. It is required VID2 pipeline to carry the bottom field (Right stereoscopic picture) of the 3D frame. The following register is affected:

- DISPC_SIZE_TV

The Video DAC (VDAC) functionality is not supported.

10.2.4.14. Shadows Registers

Refer to OMAP4460 Silicon Revision 1.x TRM.

10.2.5. Display Controller Register Manual

10.2.5.1. Display Controller Instance Summary

Table 10.1. DISPC Instance Summary

Module Name	L4_PER Base Address	L3 Base Address	Size
DISPC	0x4804 1000	0x5800 1000	4KB

10.2.5.2. Display Controller Logical Register Mapping

Refer to OMAP4460 Silicon Revision 1.x TRM.

10.2.5.3. Display Controller Registers

10.2.5.3.1. Display Controller Register Summary

Table 10.2. Display Controller Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	DISPC L4_PER Physical Address	DISPC L3 Physical Address
DISPC_REVISION	R	32	0x0000 0000	0x4804 1000	0x5800 1000
DISPC_SYSCONFIG	RW	32	0x0000 0010	0x4804 1010	0x5800 1010
DISPC_SYSSTATUS	R	32	0x0000 0014	0x4804 1014	0x5800 1014
DISPC_IRQSTATUS	RW	32	0x0000 0018	0x4804 1018	0x5800 1018
DISPC_IRQENABLE	RW	32	0x0000 001C	0x4804 101C	0x5800 101C

Register Name	Type	Register Width (Bits)	Address Offset	DISPC L4_PER Physical Address	DISPC L3 Physical Address
DISPC_CONTROL1	RW	32	0x0000 0040	0x4804 1040	0x5800 1040
DISPC_CONFIG1	RW	32	0x0000 0044	0x4804 1044	0x5800 1044
RESERVED	R	32	0x0000 0048	0x4804 1048	0x5800 1048
DISPC_DEFAULT_COLOR0	RW	32	0x0000 004C	0x4804 104C	0x5800 104C
DISPC_DEFAULT_COLOR1	RW	32	0x0000 0050	0x4804 1050	0x5800 1050
DISPC_TRANS_COLOR0	RW	32	0x0000 0054	0x4804 1054	0x5800 1054
DISPC_TRANS_COLOR1	RW	32	0x0000 0058	0x4804 1058	0x5800 1058
DISPC_LINE_STATUS	R	32	0x0000 005C	0x4804 105C	0x5800 105C
DISPC_LINE_NUMBER	RW	32	0x0000 0060	0x4804 1060	0x5800 1060
DISPC_TIMING_H1	RW	32	0x0000 0064	0x4804 1064	0x5800 1064
DISPC_TIMING_V1	RW	32	0x0000 0068	0x4804 1068	0x5800 1068
DISPC_POL_FREQ1	RW	32	0x0000 006C	0x4804 106C	0x5800 106C
DISPC_DIVISOR1	RW	32	0x0000 0070	0x4804 1070	0x5800 1070
DISPC_GLOBAL_ALPHA	RW	32	0x0000 0074	0x4804 1074	0x5800 1074
DISPC_SIZE_TV	RW	32	0x0000 0078	0x4804 1078	0x5800 1078
DISPC_SIZE_LCD1	RW	32	0x0000 007C	0x4804 107C	0x5800 107C
DISPC_GFX_BA_j[1]	RW	32	0x0000 0080 + (0x4 * j)	0x4804 1080 + (0x4 * j)	0x5800 1080 + (0x4 * j)
DISPC_GFX_POSITION	RW	32	0x0000 0088	0x4804 1088	0x5800 1088
DISPC_GFX_SIZE	RW	32	0x0000 008C	0x4804 108C	0x5800 108C
DISPC_GFX_ATTRIBUTES	RW	32	0x0000 00A0	0x4804 10A0	0x5800 10A0
DISPC_GFX_BUF_THRESHOLD	RW	32	0x0000 00A4	0x4804 10A4	0x5800 10A4
DISPC_GFX_BUF_SIZE_STATUS	R	32	0x0000 00A8	0x4804 10A8	0x5800 10A8
DISPC_GFX_ROW_INC	RW	32	0x0000 00AC	0x4804 10AC	0x5800 10AC
DISPC_GFX_PIXEL_INC	RW	32	0x0000 00B0	0x4804 10B0	0x5800 10B0
DISPC_GFX_WINDOW_SKIP	R	32	0x0000 00B4	0x4804 10B4	0x5800 10B4
DISPC_GFX_TABLE_BA	RW	32	0x0000 00B8	0x4804 10B8	0x5800 10B8
DISPC_VID1_BA_j[1]	RW	32	0x0000 00BC + (0x4 * j)	0x4804 10BC + (0x4 * j)	0x5800 10BC + (0x4 * j)
DISPC_VID1_POSITION	RW	32	0x0000 00C4	0x4804 10C4	0x5800 10C4
DISPC_VID1_SIZE	RW	32	0x0000 00C8	0x4804 10C8	0x5800 10C8
DISPC_VID1_ATTRIBUTES	RW	32	0x0000 00CC	0x4804 10CC	0x5800 10CC
DISPC_VID1_BUF_THRESHOLD	RW	32	0x0000 00D0	0x4804 10D0	0x5800 10D0
DISPC_VID1_BUF_SIZE_STATUS	R	32	0x0000 00D4	0x4804 10D4	0x5800 10D4
DISPC_VID1_ROW_INC	RW	32	0x0000 00D8	0x4804 10D8	0x5800 10D8
DISPC_VID1_PIXEL_INC	RW	32	0x0000 00DC	0x4804 10DC	0x5800 10DC
DISPC_VID1_FIR	RW	32	0x0000 00E0	0x4804 10E0	0x5800 10E0
DISPC_VID1_PICTURE_SIZE	RW	32	0x0000 00E4	0x4804 10E4	0x5800 10E4
DISPC_VID1_ACCU_j[1]	RW	32	0x0000 00E8 + (0x4 * j)	0x4804 10E8 + (0x4 * j)	0x5800 10E8 + (0x4 * j)
DISPC_VID1_FIR_COEF_H_i[2]	RW	32	0x0000 00F0 + (0x8 * i)	0x4804 10F0 + (0x8 * i)	0x5800 10F0 + (0x8 * i)
DISPC_VID1_FIR_COEF_HV_i[2]	RW	32	0x0000 00F4 + (0x8 * i)	0x4804 10F4 + (0x8 * i)	0x5800 10F4 + (0x8 * i)
DISPC_VID1_CONV_COEF0	RW	32	0x0000 0130	0x4804 1130	0x5800 1130
DISPC_VID1_CONV_COEF1	RW	32	0x0000 0134	0x4804 1134	0x5800 1134
DISPC_VID1_CONV_COEF2	RW	32	0x0000 0138	0x4804 1138	0x5800 1138
DISPC_VID1_CONV_COEF3	RW	32	0x0000 013C	0x4804 113C	0x5800 113C
DISPC_VID1_CONV_COEF4	RW	32	0x0000 0140	0x4804 1140	0x5800 1140

Register Name	Type	Register Width (Bits)	Address Offset	DISPC L4_PER Physical Address	DISPC L3 Physical Address
DISPC_VID2_BA_j[1]	RW	32	0x0000 014C + (0x4 * j)	0x4804 114C + (0x4 * j)	0x5800 114C + (0x4 * j)
DISPC_VID2_POSITION	RW	32	0x0000 0154	0x4804 1154	0x5800 1154
DISPC_VID2_SIZE	RW	32	0x0000 0158	0x4804 1158	0x5800 1158
DISPC_VID2_ATTRIBUTES	RW	32	0x0000 015C	0x4804 115C	0x5800 115C
DISPC_VID2_BUF_THRESHOLD	RW	32	0x0000 0160	0x4804 1160	0x5800 1160
DISPC_VID2_BUF_SIZE_STATUS	R	32	0x0000 0164	0x4804 1164	0x5800 1164
DISPC_VID2_ROW_INC	RW	32	0x0000 0168	0x4804 1168	0x5800 1168
DISPC_VID2_PIXEL_INC	RW	32	0x0000 016C	0x4804 116C	0x5800 116C
DISPC_VID2_FIR	RW	32	0x0000 0170	0x4804 1170	0x5800 1170
DISPC_VID2_PICTURE_SIZE	RW	32	0x0000 0174	0x4804 1174	0x5800 1174
DISPC_VID2_ACCU_j[1]	RW	32	0x0000 0178 + (0x4 * j)	0x4804 1178 + (0x4 * j)	0x5800 1178 + (0x4 * j)
DISPC_VID2_FIR_COEF_H_i[2]	RW	32	0x0000 0180 + (0x8 * i)	0x4804 1180 + (0x8 * i)	0x5800 1180 + (0x8 * i)
DISPC_VID2_FIR_COEF_HV_i[2]	RW	32	0x0000 0184 + (0x8 * i)	0x4804 1184 + (0x8 * i)	0x5800 1184 + (0x8 * i)
DISPC_VID2_CONV_COEF0	RW	32	0x0000 01C0	0x4804 11C0	0x5800 11C0
DISPC_VID2_CONV_COEF1	RW	32	0x0000 01C4	0x4804 11C4	0x5800 11C4
DISPC_VID2_CONV_COEF2	RW	32	0x0000 01C8	0x4804 11C8	0x5800 11C8
DISPC_VID2_CONV_COEF3	RW	32	0x0000 01CC	0x4804 11CC	0x5800 11CC
DISPC_VID2_CONV_COEF4	RW	32	0x0000 01D0	0x4804 11D0	0x5800 11D0
DISPC_DATA1_CYCLE1	RW	32	0x0000 01D4	0x4804 11D4	0x5800 11D4
DISPC_DATA1_CYCLE2	RW	32	0x0000 01D8	0x4804 11D8	0x5800 11D8
DISPC_DATA1_CYCLE3	RW	32	0x0000 01DC	0x4804 11DC	0x5800 11DC
DISPC_VID1_FIR_COEF_V_i[2]	RW	32	0x0000 01E0 + (0x4 * i)	0x4804 11E0 + (0x4 * i)	0x5800 11E0 + (0x4 * i)
DISPC_VID2_FIR_COEF_V_i[2]	RW	32	0x0000 0200 + (0x4 * i)	0x4804 1200 + (0x4 * i)	0x5800 1200 + (0x4 * i)
DISPC_CPR1_COEF_R	RW	32	0x0000 0220	0x4804 1220	0x5800 1220
DISPC_CPR1_COEF_G	RW	32	0x0000 0224	0x4804 1224	0x5800 1224
DISPC_CPR1_COEF_B	RW	32	0x0000 0228	0x4804 1228	0x5800 1228
DISPC_GFX_PRELOAD	RW	32	0x0000 022C	0x4804 122C	0x5800 122C
DISPC_VID1_PRELOAD	RW	32	0x0000 0230	0x4804 1230	0x5800 1230
DISPC_VID2_PRELOAD	RW	32	0x0000 0234	0x4804 1234	0x5800 1234
DISPC_CONTROL2	RW	32	0x0000 0238	0x4804 1238	0x5800 1238
DISPC_VID3_ACCU_j[1]	RW	32	0x0000 0300 + (0x4 * j)	0x4804 1300 + (0x4 * j)	0x5800 1300 + (0x4 * j)
DISPC_VID3_BA_j[1]	RW	32	0x0000 0308 + (0x4 * j)	0x4804 1308 + (0x4 * j)	0x5800 1308 + (0x4 * j)
DISPC_VID3_FIR_COEF_H_i[2]	RW	32	0x0000 0310 + (0x8 * i)	0x4804 1310 + (0x8 * i)	0x5800 1310 + (0x8 * i)
DISPC_VID3_FIR_COEF_HV_i[2]	RW	32	0x0000 0314 + (0x8 * i)	0x4804 1314 + (0x8 * i)	0x5800 1314 + (0x8 * i)
DISPC_VID3_FIR_COEF_V_i[2]	RW	32	0x0000 0350 + (0x4 * i)	0x4804 1350 + (0x4 * i)	0x5800 1350 + (0x4 * i)
DISPC_VID3_ATTRIBUTES	RW	32	0x0000 0370	0x4804 1370	0x5800 1370
DISPC_VID3_CONV_COEF0	RW	32	0x0000 0374	0x4804 1374	0x5800 1374
DISPC_VID3_CONV_COEF1	RW	32	0x0000 0378	0x4804 1378	0x5800 1378
DISPC_VID3_CONV_COEF2	RW	32	0x0000 037C	0x4804 137C	0x5800 137C
DISPC_VID3_CONV_COEF3	RW	32	0x0000 0380	0x4804 1380	0x5800 1380

Register Name	Type	Register Width (Bits)	Address Offset	DISPC L4_PER Physical Address	DISPC L3 Physical Address
DISPC_VID3_CONV_COEF4	RW	32	0x0000 0384	0x4804 1384	0x5800 1384
DISPC_VID3_BUF_SIZE_STATUS	R	32	0x0000 0388	0x4804 1388	0x5800 1388
DISPC_VID3_BUF_THRESHOLD	RW	32	0x0000 038C	0x4804 138C	0x5800 138C
DISPC_VID3_FIR	RW	32	0x0000 0390	0x4804 1390	0x5800 1390
DISPC_VID3_PICTURE_SIZE	RW	32	0x0000 0394	0x4804 1394	0x5800 1394
DISPC_VID3_PIXEL_INC	RW	32	0x0000 0398	0x4804 1398	0x5800 1398
DISPC_VID3_POSITION	RW	32	0x0000 039C	0x4804 139C	0x5800 139C
DISPC_VID3_PRELOAD	RW	32	0x0000 03A0	0x4804 13A0	0x5800 13A0
DISPC_VID3_ROW_INC	RW	32	0x0000 03A4	0x4804 13A4	0x5800 13A4
DISPC_VID3_SIZE	RW	32	0x0000 03A8	0x4804 13A8	0x5800 13A8
DISPC_DEFAULT_COLOR2	RW	32	0x0000 03AC	0x4804 13AC	0x5800 13AC
DISPC_TRANS_COLOR2	RW	32	0x0000 03B0	0x4804 13B0	0x5800 13B0
DISPC_CPR2_COEF_B	RW	32	0x0000 03B4	0x4804 13B4	0x5800 13B4
DISPC_CPR2_COEF_G	RW	32	0x0000 03B8	0x4804 13B8	0x5800 13B8
DISPC_CPR2_COEF_R	RW	32	0x0000 03BC	0x4804 13BC	0x5800 13BC
DISPC_DATA2_CYCLE1	RW	32	0x0000 03C0	0x4804 13C0	0x5800 13C0
DISPC_DATA2_CYCLE2	RW	32	0x0000 03C4	0x4804 13C4	0x5800 13C4
DISPC_DATA2_CYCLE3	RW	32	0x0000 03C8	0x4804 13C8	0x5800 13C8
DISPC_SIZE_LCD2	RW	32	0x0000 03CC	0x4804 13CC	0x5800 13CC
DISPC_TIMING_H2	RW	32	0x0000 0400	0x4804 1400	0x5800 1400
DISPC_TIMING_V2	RW	32	0x0000 0404	0x4804 1404	0x5800 1404
DISPC_POL_FREQ2	RW	32	0x0000 0408	0x4804 1408	0x5800 1408
DISPC_DIVISOR2	RW	32	0x0000 040C	0x4804 140C	0x5800 140C
DISPC_WB_ACCU_j[1]	RW	32	0x0000 0500 + (0x4 * j)	0x4804 1500 + (0x4 * j)	0x5800 1500 + (0x4 * j)
DISPC_WB_BA_j[1]	RW	32	0x0000 0508 + (0x4 * j)	0x4804 1508 + (0x4 * j)	0x5800 1508 + (0x4 * j)
DISPC_WB_FIR_COEF_H_i[2]	RW	32	0x0000 0510 + (0x8 * i)	0x4804 1510 + (0x8 * i)	0x5800 1510 + (0x8 * i)
DISPC_WB_FIR_COEF_HV_i[2]	RW	32	0x0000 0514 + (0x8 * i)	0x4804 1514 + (0x8 * i)	0x5800 1514 + (0x8 * i)
DISPC_WB_FIR_COEF_V_i[2]	RW	32	0x0000 0550 + (0x4 * i)	0x4804 1550 + (0x4 * i)	0x5800 1550 + (0x4 * i)
DISPC_WB_ATTRIBUTES	RW	32	0x0000 0570	0x4804 1570	0x5800 1570
DISPC_WB_CONV_COEF0	RW	32	0x0000 0574	0x4804 1574	0x5800 1574
DISPC_WB_CONV_COEF1	RW	32	0x0000 0578	0x4804 1578	0x5800 1578
DISPC_WB_CONV_COEF2	RW	32	0x0000 057C	0x4804 157C	0x5800 157C
DISPC_WB_CONV_COEF3	RW	32	0x0000 0580	0x4804 1580	0x5800 1580
DISPC_WB_CONV_COEF4	RW	32	0x0000 0584	0x4804 1584	0x5800 1584
DISPC_WB_BUF_SIZE_STATUS	R	32	0x0000 0588	0x4804 1588	0x5800 1588
DISPC_WB_BUF_THRESHOLD	RW	32	0x0000 058C	0x4804 158C	0x5800 158C
DISPC_WB_FIR	RW	32	0x0000 0590	0x4804 1590	0x5800 1590
DISPC_WB_PICTURE_SIZE	RW	32	0x0000 0594	0x4804 1594	0x5800 1594
DISPC_WB_PIXEL_INC	RW	32	0x0000 0598	0x4804 1598	0x5800 1598
DISPC_WB_ROW_INC	RW	32	0x0000 05A4	0x4804 15A4	0x5800 15A4
DISPC_WB_SIZE	RW	32	0x0000 05A8	0x4804 15A8	0x5800 15A8
DISPC_VID1_BA_UV_j[1]	RW	32	0x0000 0600 + (0x4 * j)	0x4804 1600 + (0x4 * j)	0x5800 1600 + (0x4 * j)
DISPC_VID2_BA_UV_j[1]	RW	32	0x0000 0608 + (0x4 * j)	0x4804 1608 + (0x4 * j)	0x5800 1608 + (0x4 * j)

Register Name	Type	Register Width (Bits)	Address Offset	DISPC L4_PER Physical Address	DISPC L3 Physical Address
DISPC_VID3_BA_UV_j[1]	RW	32	0x0000 0610 + (0x4 * j)	0x4804 1610 + (0x4 * j)	0x5800 1610 + (0x4 * j)
DISPC_WB_BA_UV_j[1]	RW	32	0x0000 0618 + (0x4 * j)	0x4804 1618 + (0x4 * j)	0x5800 1618 + (0x4 * j)
DISPC_CONFIG2	RW	32	0x0000 0620	0x4804 1620	0x5800 1620
DISPC_VID1_ATTRIBUTES2	RW	32	0x0000 0624	0x4804 1624	0x5800 1624
DISPC_VID2_ATTRIBUTES2	RW	32	0x0000 0628	0x4804 1628	0x5800 1628
DISPC_VID3_ATTRIBUTES2	RW	32	0x0000 062C	0x4804 162C	0x5800 162C
DISPC_GAMMA_TABLE0	W	32	0x0000 0630	0x4804 1630	0x5800 1630
DISPC_GAMMA_TABLE1	W	32	0x0000 0634	0x4804 1634	0x5800 1634
DISPC_GAMMA_TABLE2	W	32	0x0000 0638	0x4804 1638	0x5800 1638
DISPC_VID1_FIR2	RW	32	0x0000 063C	0x4804 163C	0x5800 163C
DISPC_VID1_ACCU2_j[1]	RW	32	0x0000 0640 + (0x4 * j)	0x4804 1640 + (0x4 * j)	0x5800 1640 + (0x4 * j)
DISPC_VID1_FIR_COEF_H2_i[2]	RW	32	0x0000 0648 + (0x8 * i)	0x4804 1648 + (0x8 * i)	0x5800 1648 + (0x8 * i)
DISPC_VID1_FIR_COEF_HV2_i[2]	RW	32	0x0000 064C + (0x8 * i)	0x4804 164C + (0x8 * i)	0x5800 164C + (0x8 * i)
DISPC_VID1_FIR_COEF_V2_i[2]	RW	32	0x0000 0688 + (0x4 * i)	0x4804 1688 + (0x4 * i)	0x5800 1688 + (0x4 * i)
DISPC_VID2_FIR2	RW	32	0x0000 06A8	0x4804 16A8	0x5800 16A8
DISPC_VID2_ACCU2_j[1]	RW	32	0x0000 06AC + (0x4 * j)	0x4804 16AC + (0x4 * j)	0x5800 16AC + (0x4 * j)
DISPC_VID2_FIR_COEF_H2_i[2]	RW	32	0x0000 06B4 + (0x8 * i)	0x4804 16B4 + (0x8 * i)	0x5800 16B4 + (0x8 * i)
DISPC_VID2_FIR_COEF_HV2_i[2]	RW	32	0x0000 06B8 + (0x8 * i)	0x4804 16B8 + (0x8 * i)	0x5800 16B8 + (0x8 * i)
DISPC_VID2_FIR_COEF_V2_i[2]	RW	32	0x0000 06F4 + (0x4 * i)	0x4804 16F4 + (0x4 * i)	0x5800 16F4 + (0x4 * i)
DISPC_VID3_FIR2	RW	32	0x0000 0724	0x4804 1724	0x5800 1724
DISPC_VID3_ACCU2_j[1]	RW	32	0x0000 0728 + (0x4 * j)	0x4804 1728 + (0x4 * j)	0x5800 1728 + (0x4 * j)
DISPC_VID3_FIR_COEF_H2_i[2]	RW	32	0x0000 0730 + (0x8 * i)	0x4804 1730 + (0x8 * i)	0x5800 1730 + (0x8 * i)
DISPC_VID3_FIR_COEF_HV2_i[2]	RW	32	0x0000 0734 + (0x8 * i)	0x4804 1734 + (0x8 * i)	0x5800 1734 + (0x8 * i)
DISPC_VID3_FIR_COEF_V2_i[2]	RW	32	0x0000 0770 + (0x4 * i)	0x4804 1770 + (0x4 * i)	0x5800 1770 + (0x4 * i)
DISPC_WB_FIR2	RW	32	0x0000 0790	0x4804 1790	0x5800 1790
DISPC_WB_ACCU2_j[1]	RW	32	0x0000 0794 + (0x4 * j)	0x4804 1794 + (0x4 * j)	0x5800 1794 + (0x4 * j)
DISPC_WB_FIR_COEF_H2_i[2]	RW	32	0x0000 07A0 + (0x8 * i)	0x4804 17A0 + (0x8 * i)	0x5800 17A0 + (0x8 * i)
DISPC_WB_FIR_COEF_HV2_i[2]	RW	32	0x0000 07A4 + (0x8 * i)	0x4804 17A4 + (0x8 * i)	0x5800 17A4 + (0x8 * i)
DISPC_WB_FIR_COEF_V2_i[2]	RW	32	0x0000 07E0 + (0x4 * i)	0x4804 17E0 + (0x4 * i)	0x5800 17E0 + (0x4 * i)
DISPC_GLOBAL_BUFFER	RW	32	0x0000 0800	0x4804 1800	0x5800 1800
DISPC_DIVISOR	RW	32	0x0000 0804	0x4804 1804	0x5800 1804
DISPC_WB_ATTRIBUTES2	RW	32	0x0000 0810	0x4804 1810	0x5800 1810

1. j = 0 to 1
2. i = 0 to 7

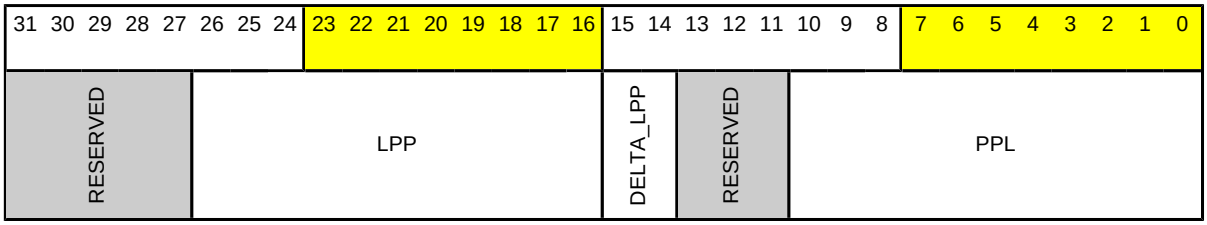
10.2.5.3.2. Display Controller Register Description

Note

This section contains only modified registers.

Table 10.3. DISPC_SIZE_TV

Address Offset	0x0000 0078
Physical Address	Please refer toTable 10.2
Description	The register configures the size of the TV output field (interlace), frame (progressive) (horizontal and vertical). Shadow register, updated on EVSYNC. A delta value is used to indicate if the odd field has same vertical size as the even field or +/- one line.
Type	RW



Bits	Field Name	Description	Type	Reset
31:27	RESERVED	Write 0's for future compatibility. Reads return 0	R	0x00
26:16	LPP	Lines per panel Encoded value (from 1 to 2048) to specify the number of lines per panel. IfDISPC_VID2_ATTRIBUTES[16] CHANNELOUT = 0x1 andDISPC_VID2_ATTRIBUTES[31:30] CHANNELOUT2 = 0x2, then the total number of lines per frame is equal to 2048 + LPP.	RW	0x000
15:14	DELTA_LPP	Indicates the delta size value of the odd field compared to the even field 0x0: Same size 0x1: Odd size = Even size +1 0x2: Odd size = Even Size -1	RW	0x0
13:11	RESERVED	Write 0's for future compatibility. Reads return 0	R	0x0
10:0	PPL	Pixels per line Encoded value (from 1 to 2048) to specify the number of pixels contains within each line on the display.	RW	0x000

Table 10.4. Register Call Summary for Register DISPC_SIZE_TV

Display Controller Functional Description

- TV Output:[0]

Table 10.5. DISPC_VID2_ATTRIBUTES

Address Offset	0x0000 015C		
Physical Address	SeeTable 10.2	**Instance**	DISPC
Description	The register configures the attributes of the video window 2. Shadow register, updated on VFP start period of primary LCD or VFP start period of the secondary LCD or EVSYNC or when DISPC_CONTROL2.GOWB is set to 1 by software and current WB frame is finished (no more data in the write-back pipeline). The synchronization event is defined based on the output using the pipeline: primary LCD, secondary LCD, TV output or write-back to the memory		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHANNELOUT2		BURSTTYPE		PREMULTIPLYALPHA		ZORDER		ZORDERENABLE	SELFREFRESH	ARBITRATION	DOUBLESTRIDE	VERTICALTAPS	DMAOPTIMIZATION	BUFPRELOAD	RESERVED	SELFREFRESHAUTO	CHANNELOUT	BURSTSIZE		ROTATION		FULLRANGE	REPLICATIONENABLE	COLORCONVENABLE	VRESIZECONF	HRESIZECONF		RESIZEENABLE		FORMAT		ENABLE

Bits	Field Name	Description	Type	Reset
31:30	CHANNELOUT2	~~It is not used if CHANNELOUT is set to TV. Reserved when CHANNELOUT = 1 (should set to zero)~~ Value 0x2 is Reserved when [16] CHANNELOUT bit = 0. Values 0x1, 0x2 and 0x3 are Reserved when CHANNELOUT bit = 1 and TV format other than HDMI 1.4 3D 1080p is to be output. wr: immediate 0x0: primary LCD output selected. 0x1: Secondary LCD output selected. 0x2: TV output selected. Used only for HDMI 1.4 3D 1080p format. 0x3: Write-back output to the memory selected.	RW	0x0
29	BURSTTYPE	The type of burst can be INCR (incremental) or B LCK (2D block). The 2D block is required when the TILER is targetted by the DMA engine. 0x0: INC burst type is used. 0x1: 2D block burst type is used.	RW	0
28	PREMULTIPLYALPHA	The field configures the DISPC VID2 to process incoming data as premultiplied alpha data or non premultiplied alpha data. Default setting is non premultiplied alpha data. 0x0: Non premultiplyalpha data color component 0x1: Premultiplyalpha data color component	RW	0
27:26	ZORDER	Z-Order defining the priority of the layer compared to others when overlaying. It is software responsibility to ensure that each layer connected to the same overlay manager has a different z-order value. If bit 25 is set to 0, the Zorder bit-field is ignored a nd replaced by the value 0. 0x0: Z-order 0: layer above solid background color and below layer with higher Z-order values. 0x1: Z-order 1: layer above layer with z-order value of 0 and below layers with z-order values of 2 and 3	RW	0x0

Bits	Field Name	Description	Type	Reset
		0x3: Z-order 3: layer above all the other layers 0x2: Z-order 2: layer above layers with z-order value of 0 and 1 and below layer with z-order value of 3		
25	ZORDERENABLE	Z-order Enable. The bit field ZORDER is only used when the Z-order is enabled. 0x0: Z-order disabled. The Z-order of the layer is 0. 0x1: Z-order enabled. The Z-order is defined by the bit-field ZORDER (bits 26 and 27).	RW	0
24	SELFREFRESH	Enables the self refresh of the video window from it s own DMA buffer only. 0x0: The video pipeline accesses the interconnect to fetch data from the system memory. 0x1: The video pipeline does not need anymore to fetch data from memory. Only the DMA buffer associated with the video2 is used. It takes effect after the frame has been loaded in the DMA buffer.	RW	0
23	ARBITRATION	Determines the priority of the video pipeline. The video pipeline is one of the high priority pipeline. The arbitration gives always the priority first to the high priority pipelines using round-robin between them. When there is only normal priority pipelines sending requests, the round-robin applies between them. 0x0: The video pipeline is one of the normal priorit y pipeline. 0x1: The video pipeline is one of the high priority pipeline.	RW	0
22	DOUBLESTRIDE	Determines if the stride for CbCr buffer is the 1x or 2x of the Y buffer stride. It is only used in case of YUV4:2:0. 0x0: The CbCr stride value is equal to the Y stride. 0x1: The CbCr stride value is double to the Y stride .	RW	0
21	VERTICALTAPS	Video Vertical Resize Tap Number 0x0: 3 taps are used for the vertical filtering logic. The 2 other taps are not used. The associated bit-fields for the 2 other taps coefficients do not need to be initialized. 0x1: 5 taps are used for the vertical filtering logic.	RW	0
20	DMAOPTIMIZATION	Write 0s for future compatibility. Reads return 0.	R	0
19	BUFPRELOAD	Video Preload Value 0x0: Hardware prefetches pixels up to the preload value defined in the preload register 0x1: Hardware prefetches pixels up to high thres hold value	RW	0
18	RESERVED	Write 0s for future compatibility. Reads return 0.	R	0
17	SELFREFRESHAUTO	Automatic self-refresh mode 0x0: The transition from SELFREFRESH "disabled" to "enabled" is controlled by SW. 0x1: The transition from SELFREFRESH "disabled" to "enabled" is controlled only by hardware.	RW	0
16	CHANNELOUT	Video Channel Out configuration: LCD, WB or TV. wr: immediate	RW	0

Bits	Field Name	Description	Type	Reset
		0x0: LCD output or WB to the memory selected. bit-fields 31 and 30 defines the output associated (primary, secondary or write-back). 0x1: TV output selected		
15:14	BURSTSIZE	Video DMA Burst Size 0x0: 2x128bit bursts 0x1: 4x128bit bursts 0x3: Reserved 0x2: 8x128bit bursts	RW	0x2
13:12	ROTATION	Video Rotation Flag 0x0: No rotation 0x1: Rotation by 90 degrees 0x3: Rotation by 270 degrees 0x2: Rotation by 180 degrees	RW	0x0
11	FULLRANGE	Color Space Conversion full range setting. 0x0: Limited range selected: 16 subtracted from Y before color space conversion 0x1: Full range selected: Y is not modified before the color space conversion	RW	0
10	REPLICATIONENABLE	Replication Enable 0x0: Disable Video replication logic 0x1: Enable Video replication logic	RW	1
9	COLORCONVENABLE	Enable the color space conversion. The hardware does not enable/disable the conversion based on the pixel format. The bit field shall be reset when the format is not YUV. 0x0: Disable Color Space Conversion YUV to RGB 0x1: Enable Color Space Conversion YUV to RGB	RW	0
8	VRESIZECONF	Write 0s for future compatibility. Reads return 0	R	0
7	HRESIZECONF	Write 0s for future compatibility. Reads return 0	R	0
6:5	RESIZEENABLE	Video Resize Enable 0x0: Disable both horizontal and vertical resize processing 0x1: Enable the horizontal resize processing 0x3: Enable both horizontal and vertical resize processing 0x2: Enable the vertical resize processing	RW	0x0
4:1	FORMAT	Video Format. It defines the pixel format when fetching the video 2 picture into memory. 0x6: RGB16-565 0x1: RGB12x-4444 0xA: YUV2 4:2:2 co-sited 0x7: ARGB16-1555 0xD: RGBA32-8888 0x0: NV12 4:2:0 2 buffers (Y + UV) 0x2: RGBA12-4444 0x8: xRGB24-8888 (32-bit container) 0x9: RGB24-888 (24-bit container) 0xB: UYVY 4:2:2 co-sited	RW	0x0

Bits	Field Name	Description	Type	Reset
		0x5: ARGB16-4444 0xF: xRGB15-1555 0xC: ARGB32-8888 0x4: xRGB12-4444 0xE: RGBx24-8888 (24-bit RGB aligned on MSB of the 32-bit container)		
0	ENABLE	VidEnable 0x0: Video disabled (video pipeline inactive and window not present) 0x1: Video enabled (video pipeline active and wi ndow present on the screen)	RW	0

Table 10.6. Register Call Summary for Register DISPC_VID2_ATTRIBUTES

Display Controller Functional Description

- LCD Outputs:[0][1][2]

10.3. MIPI Display Serial Interface

Note

This section has not changed. Refer to OMAP4460 Silicon Revision 1.x TRM.

10.4. High-Definition Multimedia Interface

Support for the 1080p@24Hz 3D Stereoscopic frame-packing format of HDMI v1.4 standard is added.

10.5. Remote Frame Buffer Interface

Note

This section has not changed. Refer to OMAP4460 Silicon Revision 1.x TRM.

10.6. Video Encoder

Note

The Video DAC (VDAC) functionality is not supported.

Chapter 11. 2D/3D Graphics Accelerator

This chapter describes the differences in the 2D/3D Graphics Accelerator between the OMAP4430 Silicon Revision 2.x and OMAP4460 Silicon Revision 1.x multimedia devices.

Note

The SGX subsystem is an instantiation by Texas Instruments of the POWERVR™ SGX540 core from Imagination Technologies Ltd.

11.1. SGX Overview

Refer to OMAP4460 Silicon Revision 1.x TRM.

11.2. SGX Integration

Refer to OMAP4460 Silicon Revision 1.x TRM.

11.3. SGX Functional Description

- The SGX_FCLK supported frequency is up to 384MHz, where in OMAP4430 ES2.x the supported frequency is up to 307MHz.

11.4. SGX Register Manual

Refer to OMAP4460 Silicon Revision 1.x TRM.

Chapter 12. ABE

This chapter describes the differences in the ABE between the OMAP4430 Silicon Revision 2.x and OMAP4460 Silicon Revision 1.x multimedia devices.

Note

This chapter has not changed. Refer to OMAP4460 Silicon Revision 1.x TRM.

Chapter 13. Interconnect

This chapter describes differences in the Interconnect between the OMAP4430 Silicon Revision 2.x and OMAP4460 Silicon Revision 1.x multimedia devices.

Note

The L3 interconnect is instantiation of the NoC interconnect from Arteris, Inc. Arteris is a registered trademark of Arteris, Inc.

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NoC is an abbreviation for Network On Chip.

Note

The L4 interconnects are instantiations of the Sonics3220™ interconnect from Sonics, Inc.

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13.1. Interconnect Overview

Note

This section has not changed. Refer to OMAP4460 Silicon Revision 1.x TRM.

13.2. L3 Interconnect

13.2.1. L3 Interconnect Overview

Refer to OMAP4460 Silicon Revision 1.x TRM.

13.2.2. L3 Interconnect Integration

Refer to OMAP4460 Silicon Revision 1.x TRM.

13.2.3. L3 Interconnect Functional Description

Memory Adapter Firewall is added. Address filtering for STATCOLL SDRAM registers is added. STATCOLL Base addresses of SDRAM, LAT0 and LAT1 are changed. This impacts the following tables:

- Slave NIU Firewall and Region Configuration
- L3 Firewall Register Summary
- STATCOLL Instance Summary - Base addresses and offsets changed.
- Three new registers for the address filtering of STATCOLL SDRAM added: L3_STCOL_FILTER_i_ADDRMIN, L3_STCOL_FILTER_i_ADDRMAX and L3_STCOL_FILTER_i_ADDREN.

The following figures are also impacted:

- L3 Interconnect Overview

13.2.4. L3 Interconnect Programming Guide

Refer to OMAP4460 Silicon Revision 1.x TRM.

13.2.5. L3 Interconnect Register Manual

13.2.5.1. L3 Register Group Summary

The registers in the L3 interconnect are divided into eight groups:

- Firewall registers
- HOST registers
- TARG registers
- PWR_DISK registers
- BW registers
- FLAGMUX registers
- RA registers
- STATCOLL registers

13.2.5.1.1. L3 Firewall Registers Summary and Description

Table 13.1. L3 Firewall Instance Summary

Module Name	Base Address	Size
C2C-Master NIU firewall	0x4A20 4000	4KB
C2C-Slave NIU firewall	0x4A20 6000	4KB
MA firewall	0x4A20 A000	4KB
EMIF firewall	0x4A20 C000	4KB
GPMC firewall	0x4A21 0000	4KB
L3 RAM firewall	0x4A21 2000	4KB
SGX firewall	0x4A21 4000	4KB
ISS firewall	0x4A21 6000	4KB
Dual Cortex-M3 firewall	0x4A21 8000	4KB
DSS firewall	0x4A21 C000	4KB
SL2 firewall	0x4A21 E000	4KB
IVA-HD firewall	0x4A22 0000	4KB
Debug firewall	0x4A22 6000	4KB
L4-ABE firewall	0x4A22 8000	4KB

13.2.5.1.1.1. L3 Firewall Registers Summary

Table 13.2. L3 Firewall Registers Summary

Register Name	Type	Register Width (Bits)	Address Offset	MA Firewall Physical Address	EMIF Firewall Physical Address	GPMC Firewall Physical Address	L3 RAM Firewall Physical Address
ERROR_LOG_k[3]	RW	32	0x000+(0 x10*k)	0x4A20 A 000+(0x10*k)	0x4A21 0 000+(0x10*k)	0x4A21 0 000+(0x10*k)	0x4A21 2 000+(0x10*k)
LOGICAL_ADDR_ERRLOG_k[3]	RO	32	0x004+(0 x10*k)	0x4A20 A 004+(0x10*k)	0x4A21 0 004+(0x10*k)	0x4A21 0 004+(0x10*k)	0x4A21 2 004+(0x10*k)
REGUPDATE_CONTROL	RW	32	0x040	0x4A20 A040	0x4A21 0040	0x4A21 0040	0x4A21 2040
START_REGION_i[1]	RW	32	0x080+(0 x10*i)	0x4A20 A 080+(0x10*i)	0x4A21 0 080+(0x10*i)	0x4A21 0 080+(0x10*i)	0x4A21 2 080+(0x10*i)
END_REGION_i[1]	RW	32	0x084+(0 x10*i)	0x4A20 A 084+(0x10*i)	0x4A21 0 084+(0x10*i)	0x4A21 0 084+(0x10*i)	0x4A21 2 084+(0x10*i)
MRM_PERMISSION_REGION_HIGH_j[2]	RW	32	0x08C+(0 x10*j)	0x4A20 A 08C+(0x10*j)	0x4A21 0 08C+(0x10*j)	0x4A21 0 08C+(0x10*j)	0x4A21 2 08C+(0x10*j)
MRM_PERMISSION_REGION_LOW_j[2]	RW	32	0x088+(0 x10*j)	0x4A20 A 088+(0x10*j)	0x4A21 0 088+(0x10*j)	0x4A21 0 088+(0x10*j)	0x4A21 2 088+(0x10*j)

1. i = 1 to 7 for EMIF firewall i = 1 to 7 for MA firewalli = 1 to 7 for GPMC firewalli = 1 to 9 for L3 RAM firewall
2. j = 0 to 7 for EMIF firewall j = 0 to 7 for MA firewallj = 0 to 7 for GPMC firewallj = 0 to 9 for L3 RAM firewall
3. k = 0 to 2 for EMIF firewall k = 0 to 2 for MA firewallk = 0 for GPMC firewall k = 0 for L3 RAM firewall

13.2.5.1.1.2. L3 Firewall Registers Description

Refer to OMAP4460 Silicon Revision 1.x TRM.

13.2.5.1.2. L3 Host Register Summary and Description

Refer to OMAP4460 Silicon Revision 1.x TRM.

13.2.5.1.3. L3 TARG Register Summary and Description

Refer to OMAP4460 Silicon Revision 1.x TRM.

13.2.5.1.4. L3 PWR_DISC Register Summary and Description

Refer to OMAP4460 Silicon Revision 1.x TRM.

13.2.5.1.5. L3 FLAGMUX Register Summary and Description

Refer to OMAP4460 Silicon Revision 1.x TRM.

13.2.5.1.6. L3 BW Regulator Register Summary and Description

Refer to OMAP4460 Silicon Revision 1.x TRM.

13.2.5.1.7. L3 Rate Adapt Register Summary and Description

Refer to OMAP4460 Silicon Revision 1.x TRM.

13.2.5.1.8. L3 STATCLOLL Register Summary and Description

Table 13.3. STATCOLL Instance Summary

Module Name	Base Address	Size
CLK3_STATCOLL_SDRAM	~~0x4500 0400~~0x4500 1000	512B
CLK3_STATCOLL_LAT0	~~0x4500 0600~~0x4500 2000	512B
CLK3_STATCOLL_LAT1	~~0x4500 0804~~0x4500 3000	512B

13.2.5.1.8.1. L3 STATCLOLL Register Summary

Table 13.4. STATCOLL Register Summary

Register Name	Type	Register Width (Bits)	Address Offset for SDRAM	CLK3_STATCOL L_SDRAM L3 Physical Address	Address Offset for LAT0	CLK3_STATCOL L_LAT0 L3 Physical Address	Address Offset for LAT1	CLK3_STATCOL L_LAT1 L3 Physical Address
L3_STCOL_STDHOSTHDR_COREREG	R	32	0x0100 1000	0x4500 1000	0x0100 2000	0x4500 2000	0x0100 3000	0x4500 3000
L3_STCOL_STDHOSTHDR_VERSIONREG	R	32	0x0100 1004	0x4500 1004	0x0100 2004	0x4500 2004	0x0100 3004	0x4500 3004
L3_STCOL_EN	RW	32	0x0100 1008	0x4500 1008	0x0100 2008	0x4500 2008	0x0100 3008	0x4500 3008
L3_STCOL_SOFTEN	RW	32	0x0100 100C	0x4500 100C	0x0100 200C	0x4500 200C	0x0100 300C	0x4500 300C
L3_STCOL_TRIGEN	RW	32	0x0100 1014	0x4500 1014	0x0100 2014	0x4500 2014	0x0100 3014	0x4500 3014
L3_STCOL_REQEVT	RW	32	0x0100 1018	0x4500 1018	0x0100 2018	0x4500 2018	0x0100 3018	0x4500 3018
L3_STCOL_RSPEVT	RW	32	0x0100 101C	0x4500 101C	0x0100 201C	0x4500 201C	0x0100 301C	0x4500 301C
L3_STCOL_EVTMUX_SEL0	RW	32	0x0100 1020	0x4500 1020	0x0100 2020	0x4500 2020	0x0100 3020	0x4500 3020
L3_STCOL_EVTMUX_SEL1	RW	32	0x0100 1024	0x4500 1024	0x0100 2024	0x4500 2024	0x0100 3024	0x4500 3024
L3_STCOL_EVTMUX_SEL2	RW	32	0x0100 1028	0x4500 1028	0x0100 2028	0x4500 2028	0x0100 3028	0x4500 3028
L3_STCOL_EVTMUX_SEL3	RW	32	0x0100 102C	0x4500 102C	0x0100 202C	0x4500 202C	0x0100 302C	0x4500 302C
L3_STCOL_EVTMUX_SEL4	RW	32	0x0100 1030	0x4500 1030	N/A	N/A	N/A	N/A
L3_STCOL_DUMP_IDENTIFIER	R	32	0x0100 1040	0x4500 1040	0x0100 2040	0x4500 2040	0x0100 3040	0x4500 3040
L3_STCOL_DUMP_COLLECTTIME	RW	32	0x0100 1044	0x4500 1044	0x0100 2044	0x4500 2044	0x0100 3044	0x4500 3044
L3_STCOL_DUMP_SLVADDR	R	32	0x0100 1048	0x4500 1048	0x0100 2048	0x4500 2048	0x0100 3048	0x4500 3048
L3_STCOL_DUMP_MSTADDR	R	32	0x0100 104C	0x4500 104C	0x0100 204C	0x4500 204C	0x0100 304C	0x4500 304C
L3_STCOL_DUMP_SLVOFS	RW	32	0x0100 1050	0x4500 1050	0x0100 2050	0x4500 2050	0x0100 3050	0x4500 3050
L3_STCOL_DUMP_MANUAL	RW	32	0x0100 1054	0x4500 1054	0x0100 2054	0x4500 2054	0x0100 3054	0x4500 3054
L3_STCOL_DUMP_SEND	RW	32	0x0100 1058	0x4500 1058	0x0100 2058	0x4500 2058	0x0100 3058	0x4500 3058
L3_STCOL_FILTER_i_GLOBALEN	RW	32	0x0100 10AC	0x4500 10AC	0x0100 20AC	0x4500 20AC	0x0100 30AC	0x4500 30AC
L3_STCOL_FILTER_i_ADDRMIN	RW	32	0x0100 10B0	0x4500 10B0	N/A	N/A	N/A	N/A

Register Name	Type	Register Width (Bits)	Address Offset for SDRAM	CLK3_STATCOL_L_SDRAM L3 Physical Address	Address Offset for LAT0	CLK3_STATCOL_L_LAT0 L3 Physical Address	Address Offset for LAT1	CLK3_STATCOL_L_LAT1 L3 Physical Address
L3_STCOL_FILTER_i_ADDRMAX	RW	32	0x0100 10B4	0x4500 10B4	N/A	N/A	N/A	N/A
L3_STCOL_FILTER_i_ADDREN	RW	32	0x0100 10B8	0x4500 10B8	N/A	N/A	N/A	N/A
L3_STCOL_FILTER_i_EN_k	RW	32	0x0100 10BC	0x4500 10BC	0x0100 20BC	0x4500 20BC	0x0100 30BC	0x4500 30BC
L3_STCOL_FILTER_i_MASK_m_MSTADDR	RW	32	0x0100 10C8	0x4500 10C8	0x0100 20C8	0x4500 20C8	0x0100 30C8	0x4500 30C8
L3_STCOL_FILTER_i_MASK_m_RD	RW	32	0x0100 10C0	0x4500 10C0	0x0100 20C0	0x4500 20C0	0x0100 30C0	0x4500 30C0
L3_STCOL_FILTER_i_MASK_m_WR	RW	32	0x0100 10C4	0x4500 10C4	0x0100 20C4	0x4500 20C4	0x0100 30C4	0x4500 30C4
L3_STCOL_FILTER_i_MASK_m_ERR	RW	32	0x0100 10D0	0x4500 10D0	0x0100 20D0	0x4500 20D0	0x0100 30D0	0x4500 30D0
L3_STCOL_FILTER_i_MASK_m_USERINFO	RW	32	0x0100 10D4	0x4500 10D4	N/A	N/A	N/A	N/A
L3_STCOL_FILTER_i_MATCH_m_MSTADDR	RW	32	0x0100 10E8	0x4500 10E8	0x0100 20E8	0x4500 20E8	0x0100 30E8	0x4500 30E8
L3_STCOL_FILTER_i_MATCH_m_RD	RW	32	0x0100 10E0	0x4500 10E0	0x0100 20E0	0x4500 20E0	0x0100 30E0	0x4500 30E0
L3_STCOL_FILTER_i_MATCH_m_WR	RW	32	0x0100 10E4	0x4500 10E4	0x0100 20E4	0x4500 20E4	0x0100 30E4	0x4500 30E4
L3_STCOL_FILTER_i_MATCH_m_ERR	RW	32	0x0100 10F0	0x4500 10F0	0x0100 20F0	0x4500 20F0	0x0100 30F0	0x4500 30F0
L3_STCOL_FILTER_i_MATCH_m_USERINFO	RW	32	0x0100 10F4	0x4500 10F4	N/A	N/A	N/A	N/A
L3_STCOL_OP_i_THRESHOLD_MINVAL	RW	32	0x0100 11F0	0x4500 11F0	0x0100 21F0	0x4500 21F0	0x0100 31F0	0x4500 31F0
L3_STCOL_OP_i_THRESHOLD_MAXVAL	RW	32	0x0100 11F4	0x4500 11F4	0x0100 21F4	0x4500 21F4	0x0100 31F4	0x4500 31F4
L3_STCOL_OP_i_EVTINFOSEL	RW	32	0x0100 11F8	0x4500 11F8	0x0100 21F8	0x4500 21F8	0x0100 31F8	0x4500 31F8
L3_STCOL_OP_i_SEL	RW	32	0x0100 11FC	0x4500 11FC	0x0100 21FC	0x4500 21FC	0x0100 31FC	0x4500 31FC

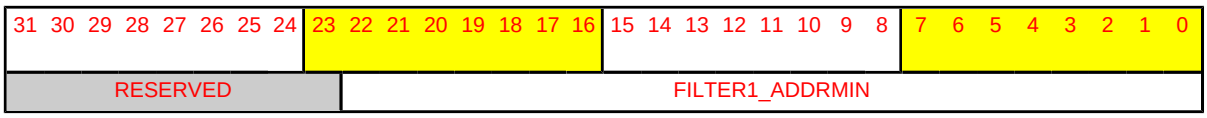
13.2.5.1.8.2. L3 STATCOLL Register Description

Note

This section contains only modified registers.

Table 13.5. L3_STCOL_FILTER_i_ADDRMIN

Address Offset	SeeTable 13.4		
Physical Address	SeeTable 13.4	**Instance**	SeeTable 13.4
Description			
Type	RW		



Bits	Field Name	Description	Type	Reset
31:23	RESERVED	Reserved	R	0bxxxxxxxxx
22:0	FILTER1_ADDRMIN	min addr range Type: Control. Reset value: 0x0.	RW	0x000000

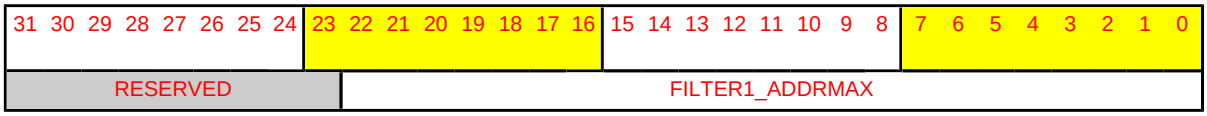
Table 13.6. Register Call Summary for Register L3_STCOL_FILTER_i_ADDRMIN

L3 Interconnect Functional Description

- L3 Interconnect Functional Description:[0]

Table 13.7. L3_STCOL_FILTER_i_ADDRMAX

Address Offset	SeeTable 13.4		
Physical Address	SeeTable 13.4	**Instance**	SeeTable 13.4
Description			
Type	RW		



Bits	Field Name	Description	Type	Reset
31:23	RESERVED	Reserved	R	0bxxxxxxxxx
22:0	FILTER1_ADDRMAX	max addr range Type: Control. Reset value: 0x0.	RW	0x000000

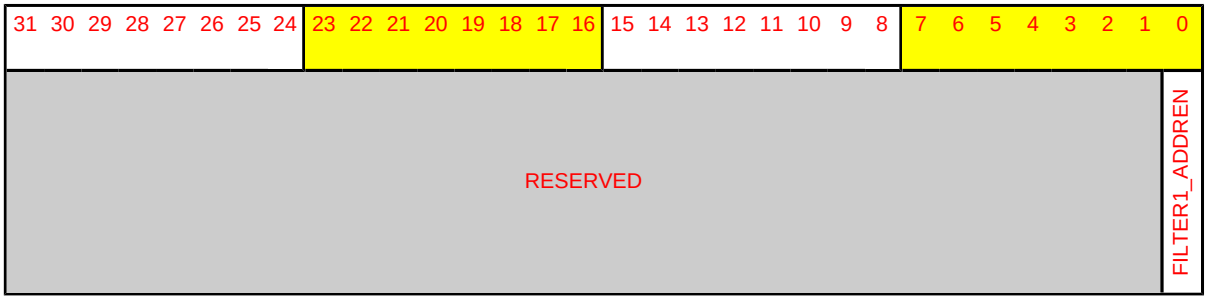
Table 13.8. Register Call Summary for Register L3_STCOL_FILTER_i_ADDRMAX

L3 Interconnect Functional Description

- L3 Interconnect Functional Description:[0]

Table 13.9. L3_STCOL_FILTER_i_ADDREN

Address Offset	SeeTable 13.4		
Physical Address	SeeTable 13.4	**Instance**	SeeTable 13.4
Description			
Type	RW		



Bits	Field Name	Description	Type	Reset
31:1	RESERVED	Reserved	R	0bxxxxxxxxxxxxxxx xxxxxxxxxxxxxxxx
0	FILTER1_ADDREN	max filtering enable Type: Control. Reset value: 0x0.	RW	0

Table 13.10. Register Call Summary for Register L3_STCOL_FILTER_i_ADDREN

L3 Interconnect Functional Description

- L3 Interconnect Functional Description:[0]

13.3. L4 Interconnects

13.3.1. L4-Interconnect Overview

Memory Adapter Firewall is added (MA FW), this impacts the following figure and tables :

- L4 - Interconnect Overview
- L4 CFG TAs
- Region Allocations for L4 CFG Interconnect
- L4_CFG to L4_WKUP region mapping is changed
- L4_CFG Instance Summary
- CFG_TA Register Mapping Summary 9

13.3.2. L4-Interconnect Integration

Refer to OMAP4460 Silicon Revision 1.x TRM.

13.3.3. L4-Interconnect Functional Description

Refer to OMAP4460 Silicon Revision 1.x TRM.

13.3.4. L4-Interconnect Programming Guide

Refer to OMAP4460 Silicon Revision 1.x TRM.

13.3.5. L4-Interconnects Register Manual

13.3.5.1. L4 Interconnects Instance Summary

Table 13.11. L4-PER Instance Summary

Module Name	L3 Base Address	Size
PER_AP	0x4800 0000	2 KB
PER_IA_0	0x4800 0800	2 KB
PER_LA	0x4800 1000	4 KB
PER_TA_UART3	0x4802 1000	4 KB
PER_TA_GPTIMER2	0x4803 3000	4 KB
PER_TA_GPTIMER3	0x4803 5000	4 KB
PER_TA_GPTIMER4	0x4803 7000	4 KB
PER_TA_GPTIMER9	0x4803 F000	4 KB
PER_TA_DSS	0x4805 0000	4 KB
PER_TA_GPIO2	0x4805 6000	4 KB
PER_TA_GPIO3	0x4805 8000	4 KB
PER_TA_GPIO4	0x4805 A000	4 KB
PER_TA_GPIO5	0x4805 C000	4 KB
PER_TA_GPIO6	0x4805 E000	4 KB
PER_TA_I2C3	0x4806 1000	4 KB
PER_TA_UART1	0x4806 B000	4 KB
PER_TA_UART2	0x4806 D000	4 KB
PER_TA_UART4	0x4806 F000	4 KB
PER_TA_I2C1	0x4807 1000	4 KB
PER_TA_I2C2	0x4807 3000	4 KB
PER_TA_SLIMBUS2	0x4807 7000	4 KB
PER_TA_ELM	0x4807 9000	4 KB
PER_TA_GPTIMER10	0x4808 7000	4 KB
PER_TA_GPTIMER11	0x4808 9000	4 KB
PER_TA_MCBSP4	0x4809 7000	4 KB
PER_TA_MCSPI1	0x4809 9000	4 KB
PER_TA_MCSPI2	0x4809 B000	4 KB
PER_TA_HSMMC1	0x4809 D000	4 KB
PER_TA_HSMMC3	0x480A E000	4 KB
PER_TA_HDQ	0x480B 3000	4 KB
PER_TA_HSMMC2	0x480B 5000	4 KB
PER_TA_MCSPI3	0x480B 9000	4 KB
PER_TA_MCSPI4	0x480B B000	4 KB
PER_TA_HSMMC4	0x480D 2000	4 KB
PER_TA_HSMMC5	0x480D 6000	4 KB
PER_TA_I2C4	0x4835 1000	4 KB

Table 13.12. L4-CFG Instance Summary

Module Name	L3 Base Address	Size
CFG_AP	0x4A00 0000	2 KB
CFG_IA_0	0x4A00 0800	2KB
CFG_LA	0x4A00 1000	4KB
CFG_TA_SYSCTRL_GENERAL_CORE	0x4A00 3000	4 KB
CFG_TA_CM1	0x4A00 5000	4 KB

Module Name	L3 Base Address	Size
CFG_TA_CM2	0x4A00 A000	4 KB
CFG_TA_SDMA	0x4A05 7000	4 KB
CFG_TA_HSI	0x4A05 C000	4 KB
CFG_TA_SAR_ROM	0x4A06 0000	4 KB
CFG_TA_HSUSBTLL	0x4A06 3000	4 KB
CFG_TA_USBHOSTHS	0x4A06 5000	4 KB
CFG_TA_DSP	0x4A06 7000	4 KB
CFG_TA_USBFS	0x4A0A A000	4 KB
CFG_TA_USBOTGHS	0x4A0A C000	4 KB
CFG_TA_USBPHY	0x4A0A E000	4 KB
CFG_TA_SR1	0x4A0D A000	4 KB
CFG_TA_SR2	0x4A0DC000	4 KB
CFG_TA_SR3	0x4A0D E000	4 KB
CFG_TA_MAILBOX	0x4A0F 5000	4 KB
CFG_TA_SPINLOCK	0x4A0F 7000	4 KB
CFG_TA_SYSCTRL_PADCONF_CORE	0x4A10 1000	4 KB
CFG_TA_FACEDETECT	0x4A10 B000	4 KB
CFG_TA_MAFW	0x4A20 A000	4 KB
CFG_TA_EMIFFW	0x4A20 D000	4 KB
CFG_TA_GPMCFW	0x4A21 1000	4 KB
CFG_TA_OCMCRAMFW	0x4A21 3000	4 KB
CFG_TA_SGXFW	0x4A21 5000	4 KB
CFG_TA_ISSFW	0x4A21 7000	4 KB
CFG_TA_CORTEXM3FW	0x4A21 9000	4 KB
CFG_TA_DSSFW	0x4A21 D000	4 KB
CFG_TA_SL2FW	0x4A21 F000	4 KB
CFG_TA_IVAHDFW	0x4A22 1000	4 KB
CFG_TA_EMUSSFW	0x4A22 7000	4 KB
CFG_TA_ABEFW	0x4A22 9000	4 KB
CFG_TA_L4WKUP	0x4A34 0000	4 KB

Table 13.13. L4-WKUP Instance Summary

Module Name	L3 Base Address	Size
WKUP_IA_0	0x4A30 0800	2KB
WKUP_LA	0x4A30 1000	4KB
WKUP_TA_32KTIMER	0x4A30 5000	4 KB
WKUP_TA_PRM	0x4A30 8000	4 KB
WKUP_TA_SCRM	0x4A30 B000	4 KB
WKUP_TA_SYSCTRL_GENERAL_WKUP	0x4A30 D000	4 KB
WKUP_TA_GPIO1	0x4A31 1000	4 KB
WKUP_TA_WDTIMER2	0x4A31 5000	4 KB
WKUP_TA_DM_TIMER1MS_1	0x4A31 9000	4 KB
WKUP_TA_KEYBOARD	0x4A31 D000	4 KB
WKUP_TA_SYSCTRL_PADCONF_WKUP	0x4A31 F000	4 KB
WKUP_TA_SAR_RAM	0x4A32 A000	4 KB

13.3.5.2. L4 Initiator Agent (L4 IA)

Refer to OMAP4460 Silicon Revision 1.x TRM.

13.3.5.3. L4 Target Agent (L4 TA)

13.3.5.3.1. L4 Target Agent (L4 TA) Register Summary

Table 13.14. CFG_TA Register Mapping Summary 10

Register Name	Type	Register Width (Bits)	Address Offset	CFG_TA_MAFW L3 Base Address	CFG_TA_EMIFFW L3 Base Address	CFG_TA_GPMC-FW L3 Base Address
L4_TA_COMPONENT_H	R	32	0x0000 0000	0x4A20 A000	0x4A20 D000	0x4A21 1000
L4_TA_COMPONENT_L	R	32	0x0000 0000	0x4A20 A000	0x4A20 D000	0x4A21 1000
L4_TA_CORE_L	R	32	0x0000 0018	0x4A20 A018	0x4A20 D018	0x4A21 1018
L4_TA_CORE_H	R	32	0x0000 001C	0x4A20 A01C	0x4A20 D01C	0x4A21 101C
L4_TA_AGENT_CONTROL_L	RW	32	0x0000 0020	0x4A20 A020	0x4A20 D020	0x4A21 1020
L4_TA_AGENT_CONTROL_H	R	32	0x0000 0024	0x4A20 A024	0x4A20 D024	0x4A21 1024
L4_TA_AGENT_STATUS_L	R	32	0x0000 0028	0x4A20 A028	0x4A20 D028	0x4A21 1028
L4_TA_AGENT_STATUS_H	R	32	0x0000 002C	0x4A20 A02C	0x4A20 D02C	0x4A21 102C

13.3.5.3.2. L4 Target Agent (L4 TA) Register Description

Refer to OMAP4460 Silicon Revision 1.x TRM.

13.3.5.4. L4 Link Agent (L4 LA)

Refer to OMAP4460 Silicon Revision 1.x TRM.

13.3.5.5. L4 Address Protection (L4 AP)

Refer to OMAP4460 Silicon Revision 1.x TRM.

Chapter 14. Chip-to-Chip Interface (C2C)

This chapter describes the differences in the C2C between the OMAP4430 Silicon Revision 2.x and OMAP4460 Silicon Revision 1.x multimedia devices.

14.1. C2C Overview

Refer to OMAP4460 Silicon Revision 1.x TRM.

14.2. C2C Integration

Refer to OMAP4460 Silicon Revision 1.x TRM.

Note

The gpio_wk0 device pad can be used as a C2C pre-wakeup pin. The aim of this pin is to be able to start the APE wakeup before to have C2C ready on the distant device to trigger the c2c_wakereqin pad. The signal from the C2C pre-wakeup pin is going only to the PRCM module and not to the C2C module.

14.3. C2C Power, Reset, and Clock Management

Refer to OMAP4460 Silicon Revision 1.x TRM.

14.4. C2C L3 Interconnect

Refer to OMAP4460 Silicon Revision 1.x TRM.

14.5. C2C SSCM

Refer to OMAP4460 Silicon Revision 1.x TRM.

14.6. Intersystem Communication Register (ICR)

Refer to OMAP4460 Silicon Revision 1.x TRM.

14.7. C2C Register Manual

Refer to OMAP4460 Silicon Revision 1.x TRM.

Chapter 15. Memory Subsystem

This chapter describes the differences in the Memory Subsystem between the OMAP4430 Silicon Revision 2.x and OMAP4460 Silicon Revision 1.x multimedia devices.

15.1. Memory Subsystem Overview

Note

This section has not changed. Refer to OMAP4460 Silicon Revision 1.x TRM.

15.2. Dynamic Memory Manager

15.2.1. DMM Overview

Refer to OMAP4460 Silicon Revision 1.x TRM.

15.2.2. DMM Integration

Refer to OMAP4460 Silicon Revision 1.x TRM.

15.2.3. DMM Functional Description

The Extra Low Latency Access (ELLA) block is removed, this impacts the following subsections, figures and registers:

- Figure DMM Block Diagram is changed.
- DMM Transaction Flows
- ELLA Description - subsection is removed.
- LISA Description is modified.
- Register DMM_HWINFO is changed. Reset value of bitfield ELLA_CNT is changed from 0x1 to 0x0.

15.2.4. DMM Use Cases and Tips

Information about the LUT_ID information in the PAT refill engines programming is added. This impacts the following subsections and figures:

- Simple Manual Area Refill is changed - subsection and scheme changed.
- Single Auto-Configured Area Refill - subsection and scheme changed.
- Chained Auto-Configured Area Refill - subsection and scheme changed.
- Synchronized Auto-Configured Area Refill - subsection and scheme changed.
- Cyclic Synchronized Auto-Configured Area Refill - subsection and scheme changed.

15.2.5. DMM Basic Programming Model

Refer to OMAP4460 Silicon Revision 1.x TRM.

15.2.6. DMM Register Manual

15.2.6.1. DMM Instance Summary

Table 15.1. DMM Instance Summary

Module Name	Base Address	Size
DMM	0x4E00 0000	32 Mbytes

15.2.6.2. DMM Registers

15.2.6.2.1. DMM Register Summary

Table 15.2. DMM Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	DMM Base Address
DMM_REVISION	R	32	0x0000 0000	0x4E00 0000
DMM_HWINFO	R	32	0x0000 0004	0x4E00 0004
DMM_LISA_HWINFO	R	32	0x0000 0008	0x4E00 0008
DMM_SYSCONFIG	RW	32	0x0000 0010	0x4E00 0010
DMM_LISA_LOCK	RW	32	0x0000 001C	0x4E00 001C
DMM_LISA_MAP_i[1]	RW	32	0x0000 0040 + (0x4 * i)	0x4E00 0040 + (0x4 * i)
DMM_TILER_HWINFO	R	32	0x0000 0208	0x4E00 0208
DMM_TILER_OR0	RW	32	0x0000 0220	0x4E00 0220
DMM_TILER_OR1	RW	32	0x0000 0224	0x4E00 0224
DMM_PAT_HWINFO	R	32	0x0000 0408	0x4E00 0408
DMM_PAT_GE-OMETRY	R	32	0x0000 040C	0x4E00 040C
DMM_PAT_CONFIG	RW	32	0x0000 0410	0x4E00 0410
DMM_PAT_VIEW0	RW	32	0x0000 0420	0x4E00 0420
DMM_PAT_VIEW1	RW	32	0x0000 0424	0x4E00 0424
DMM_PAT_VIEW _MAP_i[1]	RW	32	0x0000 0440 + (0x4 * i)	0x4E00 0440 + (0x4 * i)
DMM_PAT_VIEW _MAP_BASE	RW	32	0x0000 0460	0x4E00 0460
DMM_PAT_IRQSTATUS_RAW	RW	32	0x0000 0480	0x4E00 0480
DMM_PAT_IRQSTATUS	RW	32	0x0000 0490	0x4E00 0490
DMM_PAT_IRQENABLE_SET	RW	32	0x0000 04A0	0x4E00 04A0
DMM_PAT_IRQENABLE_CLR	RW	32	0x0000 04B0	0x4E00 04B0
DMM_PAT_STATUS_i[1]	R	32	0x0000 04C0 + (0x4 * i)	0x4E00 04C0 + (0x4 * i)
DMM_PAT_DESCR_i[1]	RW	32	0x0000 0500 + (0x10 * i)	0x4E00 0500 + (0x10 * i)
DMM_PAT_AREA_i[1]	RW	32	0x0000 0504 + (0x10 * i)	0x4E00 0504 + (0x10 * i)
DMM_PAT_CTRL_i[1]	RW	32	0x0000 0508 + (0x10 * i)	0x4E00 0508 + (0x10 * i)
DMM_PAT_DATA_i[1]	RW	32	0x0000 050C + (0x10 * i)	0x4E00 050C + (0x10 * i)
DMM_PEG_HWINFO	R	32	0x0000 0608	0x4E00 0608
DMM_PEG_PRIO_k[2]	RW	32	0x0000 0620 + (0x4 * k)	0x4E00 0620 + (0x4 * k)
DMM_PEG_PRIO_PAT	RW	32	0x0000 0640	0x4E00 0640

1. i = 0 to 3 for DMM
2. k = 0 to 7

15.2.6.2.2. DMM Register Description

Note

This section contains only modified registers.

Table 15.3. DMM_HWINFO

Address Offset	0x0000 0004		
Physical Address	SeeTable 15.2	**Instance**	DMM
Description	DMM hardware configuration		
Type	R		

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
RESERVED	ROBIN_CNT	RESERVED / ELLA_CNT	RESERVED / TILER_CNT

Bits	Field Name	Description	Type	Reset
31:20	RESERVED	Reserved	R	0x000
19:16	ROBIN_CNT	Number of ROBIN in the DMM	R	0x2
15:12	RESERVED	Reserved	R	0x0
11:8	ELLA_CNT	Number of ELLA in the DMM	R	~~0x1~~0x0
7:4	RESERVED	Reserved	R	0x0
3:0	TILER_CNT	Number of TILER in the DMM	R	0x2

15.3. EMIF Controller

15.3.1. EMIF Module Overview

Support for LPDDR2-NVM memories is removed.

15.3.2. EMIF Environment

Refer to OMAP4460 Silicon Revision 1.0 TRM.

15.3.3. EMIF Integration

There is a new connection between the EMIF Controller and Memory Adapter in Cortex-A9 MPU. Two new clocks added (EOCP_MA_ICLK and EOCP_L3_ICLK) comming from PRCM. This impacts the following figures:

- EMIF Module Overview - link to MA added
- EMIF Overall Architecture - link to MA added
- EMIF1 Integration - link to MA added and new clocks
- EMIF2 Integration - link to MA added and new clocks
- A Note added regarding EOCP_MA_ICLK and EOCP_L3_ICLK clocks.

15.3.4. EMIF Functional Description

Due to the link of EMIF and MA the following changes are applied:

- EMIF Block Diagram - figure and subsection are updated.
- L3 Interface subsection is updated
- Table. MAddrSpace Mapping to Chip Selects, is updated.
- FIFOs Description and FIFO Block Diagram are changed.
- FIFO Allocation is updated.
- In Arbitration section is added information about the new REG_MPU_TRESH_MAX bitfield of EMIF_L3_CONFIG register.
- New subsection added - MPU Port restrictions.
- System Power Management is updated. EMIF_READ_IDLE_CTRL register description is changed.
- EMIF_SDRAM_REF_CTRL register description is changed.

15.3.5. External Memory Interface (EMIF) Programming Guide

Refer to OMAP4460 Silicon Revision 1.x TRM.

15.3.6. EMIF Register Manual

15.3.6.1. EMIF Instance Summary

Table 15.4. EMIF Instance Summary

Module Name	Base Address	Size
EMIF1	0x4C00 0000	16 MB
EMIF2	0x4D00 0000	16 MB

15.3.6.2. EMIF Registers

15.3.6.2.1. EMIF Register Summary

Table 15.5. EMIF Registers Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	EMIF1 Physical Address	EMIF2 Physical Address
EMIF_MOD_ID_REV	R	32	0x0000 0000	0x4C00 0000	0x4D00 0000
EMIF_STATUS	R	32	0x0000 0004	0x4C00 0004	0x4D00 0004
EMIF_SDRAM_CONFIG	RW	32	0x0000 0008	0x4C00 0008	0x4D00 0008
EMIF_SDRAM_CONFIG_2	RW	32	0x0000 000C	0x4C00 000C	0x4D00 000C
EMIF_SDRAM_REF_CTRL	RW	32	0x0000 0010	0x4C00 0010	0x4D00 0010
EMIF_SDRAM_REF_CTRL_SHDW	RW	32	0x0000 0014	0x4C00 0014	0x4D00 0014
EMIF_SDRAM_TIM_1	RW	32	0x0000 0018	0x4C00 0018	0x4D00 0018
EMIF_SDRAM_TIM_1_SHDW	RW	32	0x0000 001C	0x4C00 001C	0x4D00 001C
EMIF_SDRAM_TIM_2	RW	32	0x0000 0020	0x4C00 0020	0x4D00 0020
EMIF_SDRAM_TIM_2_SHDW	RW	32	0x0000 0024	0x4C00 0024	0x4D00 0024
EMIF_SDRAM_TIM_3	RW	32	0x0000 0028	0x4C00 0028	0x4D00 0028
EMIF_SDRAM_TIM_3_SHDW	RW	32	0x0000 002C	0x4C00 002C	0x4D00 002C
EMIF_LPDDR2_NVM_TIM	RW	32	0x0000 0030	0x4C00 0030	0x4D00 0030
EMIF_LPDDR2_NVM_TIM_SHDW	RW	32	0x0000 0034	0x4C00 0034	0x4D00 0034
EMIF_PWR_MGMT_CTRL	RW	32	0x0000 0038	0x4C00 0038	0x4D00 0038
EMIF_PWR_MGMT_CTRL_SHDW	RW	32	0x0000 003C	0x4C00 003C	0x4D00 003C
EMIF_LPDDR2_MODE_REG_DATA	RW	32	0x0000 0040	0x4C00 0040	0x4D00 0040
EMIF_LPDDR2_MODE_REG_CFG	RW	32	0x0000 0050	0x4C00 0050	0x4D00 0050
EMIF_L3_CONFIG	RW	32	0x0000 0054	0x4C00 0054	0x4D00 0054
EMIF_L3_CFG_VAL_1	R	32	0x0000 0058	0x4C00 0058	0x4D00 0058
	R	32	0x0000 005C	0x4C00 005C	0x4D00 005C

Register Name	Type	Register Width (Bits)	Address Offset	EMIF1 Physical Address	EMIF2 Physical Address
EMIF_L3_CFG_VAL_2					
EMIF_PERF_CNT_1	R	32	0x0000 0080	0x4C00 0080	0x4D00 0080
EMIF_PERF_CNT_2	R	32	0x0000 0084	0x4C00 0084	0x4D00 0084
EMIF_PERF_CNT_CFG	RW	32	0x0000 0088	0x4C00 0088	0x4D00 0088
EMIF_PERF_CNT_SEL	RW	32	0x0000 008C	0x4C00 008C	0x4D00 008C
EMIF_PERF_CNT_TIM	R	32	0x0000 0090	0x4C00 0090	0x4D00 0090
EMIF_READ_IDLE_CTRL	RW	32	0x0000 0090	0x4C00 0098	0x4D00 0098
EMIF_READ_IDLE_CTRL_SHDW	RW	32	0x0000 0090	0x4C00 009C	0x4D00 009C
EMIF_IRQSTATUS_RAW_SYS	RW	32	0x0000 00A4	0x4C00 00A4	0x4D00 00A4
EMIF_IRQSTATUS_RAW_LL	RW	32	0x0000 00A8	0x4C00 00A8	0x4D00 00A8
EMIF_IRQSTATUS_SYS	RW	32	0x0000 00AC	0x4C00 00AC	0x4D00 00AC
EMIF_IRQSTATUS_LL	RW	32	0x0000 00B0	0x4C00 00B0	0x4D00 00B0
EMIF_IRQENABLE_SET_SYS	RW	32	0x0000 00B4	0x4C00 00B4	0x4D00 00B4
EMIF_IRQENABLE_SET_LL	RW	32	0x0000 00B8	0x4C00 00B8	0x4D00 00B8
EMIF_IRQENABLE_CLR_SYS	RW	32	0x0000 00BC	0x4C00 00BC	0x4D00 00BC
EMIF_IRQENABLE_CLR_LL	RW	32	0x0000 00C0	0x4C00 00C0	0x4D00 00C0
EMIF_ZQ_CONFIG	RW	32	0x0000 00C8	0x4C00 00C8	0x4D00 00C8
EMIF_TEMP_ALERT_CONFIG	RW	32	0x0000 00CC	0x4C00 00CC	0x4D00 00CC
EMIF_L3_ERR_LOG	R	32	0x0000 00D0	0x4C00 00D0	0x4D00 00D0
EMIF_DDR_PHY_CTRL_1	RW	32	0x0000 00E4	0x4C00 00E4	0x4D00 00E4
EMIF_DDR_PHY_CTRL_1_SHDW	RW	32	0x0000 00E8	0x4C00 00E8	0x4D00 00E8
EMIF_DDR_PHY_CTRL_2	RW	32	0x0000 00EC	0x4C00 00EC	0x4D00 00EC

15.3.6.2.2. EMIF Register Description

Note

This section contains only modified registers.

Table 15.6. EMIF_L3_CONFIG

Address Offset	0x0000 0054		
Physical Address	SeeTable 15.5	**Instance**	EMIF1 EMIF2
Description	Config Register		
Type	RW		

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
RESERVED	REG_SYS_THRESH_MAX	RESERVED REG_MPU_TRESH_MAX	REG_LL_THRESH_MAX	RESERVED	REG_PR_OLD_COUNT

Bits	Field Name	Description	Type	Reset
31:28	RESERVED	Reserved for future use.	R	0x0
27:24	REG_SYS_THRESH_MAX	System L3 Threshold Maximum. The number of commands the system interface can consume in the command FIFO. The value is used to determine when to stop future request, writing a zero will reserve no space for the associated interface. In the event the value is set to zero and a request is seen for that interface, the command FIFO will assume a value of 1. Since the low-latency interface has effectively a higher priority, the only way for the system interface to use all command FIFO entries is to set the REG_LL_THRESH_MAX to zero.	RW	0x7
23:20	~~RESERVED~~REG_MPU_TRESH_MAX	~~Reserved for future use.~~MPU Interface Threshold Maximum. The number of commands the MPU interface can consume in the command FIFO. The value is used to determine when to stop future request, writing a zero will reserve no space for the associated interface. In the event the value is set to zero and a request is seen for that interface, the command FIFO will assume a value of 1.	~~R~~RW	~~0x0~~0x7
19:16	REG_LL_THRESH_MAX	Low-latency L3 Threshold Maximum. The number of commands the low latency interface can consume in the command FIFO. The value is used to determine when to stop future request, writing a zero will reserve no space for the associated interface. In the event the value is set to zero and a request is seen for that interface, the command FIFO will assume a value of 1.	RW	0x7
15:8	RESERVED	Reserved for future use.	R	0x0
7:0	~~REG_PR_OLD_COUNT~~ RESERVED	~~Priority Raise Old Counter. Number of memory transfers after which the EMIF momentarily raises the priority of old commands in the L3 Command FIFO.~~Although this field is reserved, it is still read writable. Values written have no effect on operation of the EMIF4D3	RW	0xFF

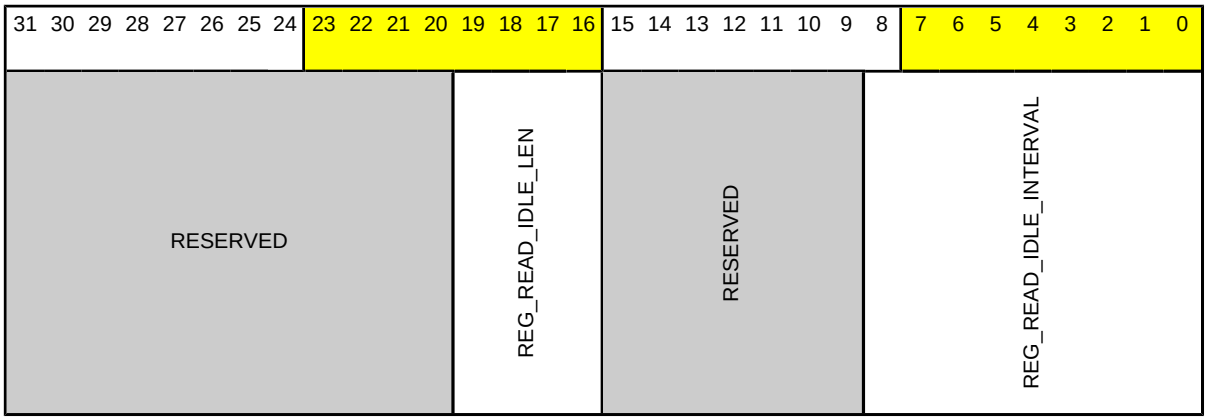
Table 15.7. Register Call Summary for Register EMIF_L3_CONFIG

EMIF Functional Description

- EMIF Functional Description:[0]

Table 15.8. EMIF_READ_IDLE_CTRL

Address Offset	0x0000 0098		
Physical Address	SeeTable 15.5	**Instance**	EMIF1 EMIF2
Description	Read Idle Control Register		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:20	RESERVED	Reserved for future use.	R	0x0
19:16	REG_READ_IDLE_LEN	~~The Read Idle Length field determines the minimum size (reg_read_idle_len-1 EMIF_FCLK clock cycles) of Read Idle window for the read idle detection as well as the force read idle time.~~The Read Idle Length field determines the minimum required size that a read idle window must be to be detected or generated. The actual read idle length will be (REG_READ_IDLE_LEN+1)*2 EMIF_FCLK clocks. The value programmed should be (the required read idle length minus one) divided by two.	RW	0x5
15:9	RESERVED	Reserved for future use.	R	0x0
8:0	REG_READ_IDLE_INTERVAL	~~The Read Idle Interval field determines the maximum interval ((REG_READ_IDLE_INTERVAL - 1) * 64 EMIF_FCLK clock cycles) between read idle detections or force.~~ ~~A value of zero disables the read idle function.~~The Read Idle Interval field determines the maximum interval between successive read idle events. The actual interval between read idle events is (REG_READ_IDLE_INTERVAL+1)*64 EMIF_FCLK clocks. The value programmed should be (the required max interval divided by sixty four) minus one. A value of 0 disables the read idle function.	RW	0x0

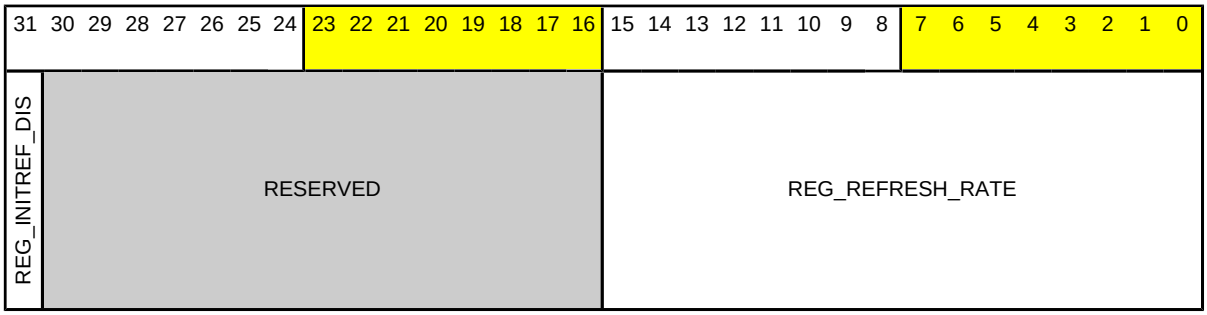
Table 15.9. Register Call Summary for Register EMIF_READ_IDLE_CTRL

EMIF Functional Description

- EMIF Functional Description:[0]

Table 15.10. EMIF_SDRAM_REF_CTRL

Address Offset	0x0000 0010		
Physical Address	SeeTable 15.5	**Instance**	EMIF1 EMIF2
Description	SDRAM Refresh Control Register		
Type	RW		



Bits	Field Name	Description	Type	Reset
31	REG_INITREF_DIS	Initialization and Refresh disable. When set to 1, EMIF will disable SDRAM initialization and refreshes, but will carry out SDRAM write/read transactions.	RW	0
30:16	RESERVED	Reserved	R	0
15:0	REG_REFRESH_RATE	Refresh Rate. Value in this field is used to define the rate at which connected SDRAM devices will be refreshed. SDRAM refresh rate = DDR_PHY_CLK / REG_REFRESH_RATE.~~SDRAM refresh rate = DDR clock rate / REFRESH_RATE. If REFRESH_RATE < (8 × T_RFC) + T_RP + T_RCD + 20 then it will be loaded with (8 × T_RFC) + T_RP + T_RCD + 20. This is done to avoid lock-up situations when illegal values are programmed.~~ To avoid lock-up situations, the programmer must not program REG_REFRESH_RATE < (6 x REG_T_RFC).For DDR_PHY_CLK description, see Section 16.3.3, EMIF Integration.	RW	0x0000

Table 15.11. Register Call Summary for Register EMIF_SDRAM_REF_CTRL

EMIF Functional Description

- EMIF Functional Description:[0]

15.4. General-Purpose Memory Controller Overview

Note

This section has not changed. Refer to OMAP4460 Silicon Revision 1.x TRM.

15.5. Error Location Module

Note

This section has not changed. Refer to OMAP4460 Silicon Revision 1.x TRM.

15.6. On-Chip Memory (OCM) Subsystem

Note

This section has not changed. Refer to OMAP4460 Silicon Revision 1.x TRM.

Chapter 16. SDMA

This chapter describes differences in sDMA between the OMAP4430 Silicon Revision 2.x and OMAP4460 Silicon Revision 1.x multimedia devices.

16.1. sDMA Module Overview

Refer to OMAP4460 Silicon Revision 1.x TRM.

16.2. sDMA Controller Environment

Refer to OMAP4460 Silicon Revision 1.x TRM.

16.3. sDMA Module Integration

Refer to OMAP4460 Silicon Revision 1.x TRM.

16.4. sDMA Functional Description

16.4.1. sDMA Controller Power Management

Refer to OMAP4460 Silicon Revision 1.x TRM.

16.4.2. sDMA Controller Interrupt Requests

Refer to OMAP4460 Silicon Revision 1.x TRM.

16.4.3. Logical Channel Transfer Overview

Refer to OMAP4460 Silicon Revision 1.x TRM.

16.4.4. FIFO Queue Memory Pool

Refer to OMAP4460 Silicon Revision 1.x TRM.

16.4.5. Addressing Modes

Refer to OMAP4460 Silicon Revision 1.x TRM.

16.4.6. Packed Accesses

Refer to OMAP4460 Silicon Revision 1.x TRM.

16.4.7. Burst Transactions

Refer to OMAP4460 Silicon Revision 1.x TRM.

16.4.8. Endianism Conversion

Refer to OMAP4460 Silicon Revision 1.x TRM.

16.4.9. Transfer Synchronization

Refer to OMAP4460 Silicon Revision 1.x TRM.

16.4.10. Thread Budget Allocation

Refer to OMAP4460 Silicon Revision 1.x TRM.

16.4.11. FIFO Budget Allocation

Refer to OMAP4460 Silicon Revision 1.x TRM.

16.4.12. Chained Logical Channel Transfers

Refer to OMAP4460 Silicon Revision 1.x TRM.

16.4.13. Reprogramming an Active Channel

Refer to OMAP4460 Silicon Revision 1.x TRM.

16.4.14. Packet Synchronization

Refer to OMAP4460 Silicon Revision 1.x TRM.

16.4.15. Graphics Acceleration Support

Refer to OMAP4460 Silicon Revision 1.x TRM.

16.4.16. Supervisor Modes

Refer to OMAP4460 Silicon Revision 1.x TRM.

16.4.17. Posted and Nonposted Writes

Refer to OMAP4460 Silicon Revision 1.x TRM.

16.4.18. Disabling a Channel During Transfer

Refer to OMAP4460 Silicon Revision 1.x TRM.

16.4.19. FIFO Draining Mechanism

Refer to OMAP4460 Silicon Revision 1.x TRM.

16.4.20. Linked List

Refer to OMAP4460 Silicon Revision 1.x TRM.

16.4.21. Auto-Restore Feature

The Auto-Restore feature has the following updates:

- There is new ordering for the registers in SAR_RAM_1 - EMIF1.EMIF_SDRAM_CONFIG is saved in order 2 instead of order 1, and EMIF1.EMIF_LPDDR2_NVM_CONFIG is saved in order 1 instead of order 2. EMIF2.EMIF_SDRAM_CONFIG is saved in order 28 instead of order 27, and EMIF2.EMIF_LPDDR2_NVM_CONFIG is saved in order 27 instead of order 28. SYSCTRL_PADCONF_CORE.CONTROL_PADCONF_GLOBAL previously under number 97, now under number 98. New register added to the list - CONTROL_HWOBS_CONTROL, saved in order 106. All registers after SYSCTRL_PADCONF_CORE.CONTROL_PADCONF_GLOBAL (till SYSCTRL_PADCONF_CORE.CONTROL_EFUSE_4) are also shifted with one position.

There is new ordering for the DMM.DMM_LISA_MAP_0 register in SAR_RAM_1, previously under number 239, now under number 246. All other registers after DMM.DMM_LISA_MAP_0 are shifted with seven positions. All registers from DMM.DMM_LISA_MAP_0 to RESTORE_CM2.CM_SDMA_STATICDEP_RESTORE have updated SAR RAM address, updated with plus 4 bytes.

- One new register added to the SAR_RAM_2 list - SYSCTRL_PADCONF_CORE.CONTROL_CORE_PAD0_CSI22_DY2
- Five new registers added to the SAR_RAM_3 list - MPUMA_FW.MRM_PERMISSION_REGION_LOW_0, CFG_AP.L4_AP_REGION_92_L, CFG_AP.L4_AP_REGION_93_L, CFG_AP.L4_AP_REGION_94_L and CFG_AP.L4_AP_REGION_95_L. The ordering of the registers is changed with plus three positions.

Table 16.1. SAR_RAM_1 Memory Mapping

Order	Register Name	Register Start Addr	Register End Addr	Size	SAR RAM Address
~~1~~2	EMIF1.EMIF_SDRAM_CONFIG	0x4C 000008		4	0x4A 326000
~~2~~1	EMIF1.EMIF_LPDDR2_NVM_CONFIG	0x4C 00000C		4	0x4A 326004
...	.....	.....		....	.....
26	EMIF1.EMIF_DDR_PHY_CTRL_2	0x4C 0000EC		4	0x4A 326064
~~27~~28	EMIF2.EMIF_SDRAM_CONFIG	0x4D 000008		4	0x4A 326064
~~28~~27	EMIF2.EMIF_LPDDR2_NVM_CONFIG	0x4D 00000C		4	0x4A 32606C
29	EMIF2.EMIF_SDRAM_REF_CTRL	0x4D 000010		4	0x4A 326070
...	.....	.....		....	.....
95	C2C.C2C_GENO_LEVEL	0x5C 000088		4	0x4A 326068
~~97~~98	SYSCTRL_PADCONF_CORE .CONTROL_PADCONF_GLOBAL	0x4A 1005A0	0x4A 1005DB	60	0x4A 32617C
~~98~~99	SYSCTRL_PADCONF_CORE.CONTROL_PBIASLITE	0x4A 100600	0x4A 100637	56	0x4A 3261B8
~~99~~100	SYSCTRL_PADCONF_CORE.CONTROL_LPDDR2IO1_0	0x4A 100638	0x4A 100657	32	0x4A 3261F0
~~100~~101	SYSCTRL_PADCONF_CORE.CONTROL_BUS_HOLD	0x4A 100658		4	0x4A 326210
~~101~~102	SYSCTRL_PADCONF_CORE.CONTROL_C2C	0x4A 10065C		4	0x4A 326214
~~102~~103	SYSCTRL_PADCONF_CORE.CONTROL_EFUSE_1	0x4A 100700		4	0x4A 326218
~~103~~104	SYSCTRL_PADCONF_CORE.CONTROL_EFUSE_2	0x4A 100704		4	0x4A 32621C
~~104~~105	SYSCTRL_PADCONF_CORE.CONTROL_EFUSE_4	0x4A 10070C		4	0x4A 326220
106	CONTROL_HWOBS_CONTROL	0x4A 002350		4	0x4A 326224
~~239~~246	DMM.DMM_LISA_MAP_0	0x4E 000040		4	0x4A 3262248
~~240~~247	DMM.DMM_LISA_MAP_1	0x4E 000044		4	0x4A 326228C
~~241~~248	DMM.DMM_LISA_MAP_2	0x4E 000048		4	0x4A3262 ~~2C~~30
~~242~~249	DMM.DMM_LISA_MAP_3	0x4E 00004C		4	0x4A 326230~~0~~4
~~243~~250	DMM.DMM_LISA_LOCK	0x4E 00001C		4	0x4A 3262348
~~244~~251	DMM.DMM_TILER_OR0			4	

Order	Register Name	Register Start Addr	Register End Addr	Size	SAR RAM Address
		0x4E 000220			0x4A 326238C
245252	DMM.DMM_TILER_OR1	0x4E 000224		4	0x4A3262 3C40
246253	DMM.DMM_PAT_VIEW0	0x4E 000420		4	0x4A 326240 4
247254	DMM.DMM_PAT_VIEW1	0x4E 000424		4	0x4A 326244 8
248255	DMM.DMM_PAT_VIEW_MAP_0	0x4E 000440		4	0x4A 326248C
249256	DMM.DMM_PAT_VIEW_MAP_1	0x4E 000444		4	0x4A3262 4C50
250257	DMM.DMM_PAT_VIEW_MAP_2	0x4E 000448		4	0x4A 326250 4
251258	DMM.DMM_PAT_VIEW_MAP_3	0x4E 00044C		4	0x4A 326254 8
252259	DMM.DMM_PAT_VIEW_MAP_BASE	0x4E 000460		4	0x4A 326258C
253260	DMM.DMM_PAT_IRQENABLE_SET	0x4E 0004A0		4	0x4A3262 5C60
254261	DMM.DMM_PAT_DESCR_0	0x4E 000500		4	0x4A 326260 4
255262	DMM.DMM_PAT_AREA_0	0x4E 000504		4	0x4A 326264 8
256263	DMM.DMM_PAT_CTRL_0	0x4E 000508		4	0x4A 326268C
257264	DMM.DMM_PAT_DATA_0	0x4E 00050C		4	0x4A3262 6C70
258265	DMM.DMM_PAT_DESCR_1	0x4E 000510		4	0x4A 326270 4
259266	DMM.DMM_PAT_AREA_1	0x4E 000514		4	0x4A 326274 8
260267	DMM.DMM_PAT_CTRL_1	0x4E 000518		4	0x4A 326278C
261268	DMM.DMM_PAT_DATA_1	0x4E 00051C		4	0x4A3262 7C80
262269	DMM.DMM_PAT_DESCR_2	0x4E 000520		4	0x4A 326280 4
263270	DMM.DMM_PAT_AREA_2	0x4E 000524		4	0x4A 326284 8
264271	DMM.DMM_PAT_CTRL_2	0x4E 000528		4	0x4A 326288C
265272	DMM.DMM_PAT_DATA_2	0x4E 00052C		4	0x4A3262 8C90
266273	DMM.DMM_PAT_DESCR_3	0x4E 000530		4	0x4A 326290 4
267274	DMM.DMM_PAT_AREA_3	0x4E 000534		4	0x4A 326294 8
268275	DMM.DMM_PAT_CTRL_3	0x4E 000538		4	0x4A 326298C
269276	DMM.DMM_PAT_DATA_3	0x4E 00053C		4	0x4A3262 9CA0
270277	DMM.DMM_PEG_PRIO0	0x4E 000460		4	0x4A 3262A0 4

Order	Register Name	Register Start Addr	Register End Addr	Size	SAR RAM Address
271278	DMM.DMM_PEG_PRIO1	0x4E 000464		4	0x4A 3262A448
272279	DMM.DMM_PEG_PRIO_PAT	0x4E 000640		4	0x4A 3262A8C
273280	CLK1_FLAGMUX_CLK1.L3_FLAGMUX_MASK0	0x44 000508		4	0x4A3262 ACB0
274281	CLK1_FLAGMUX_CLK1.L3_FLAGMUX_MASK1	0x44 000510		4	0x4A 3262B04
275282	CLK1_DSS_BW_REGULATOR.L3_BW_R_BANDWIDTH	0x44 000708		4	0x4A 3262B48
276283	CLK1_DSS_BW_REGULATOR.L3_BW_R_WATERMARK	0x44 00070C		4	0x4A 3262B8C
277284	CLK1_RATE_ADAPT_RESP_32TO128_CLK1.L3_RA_CNF	0x44 000808		4	0x4A3262 BCC0
278285	CLK2_FLAGMUX_CLK2.L3_FLAGMUX_MASK0	0x44 801008		4	0x4A 3262C04
279286	CLK2_FLAGMUX_CLK2.L3_FLAGMUX_MASK1	0x44 801010		4	0x4A 3262C48
280287	CLK2_RATE_ADAPT_RESP_32TO128_CLK2.L3_RA_CNF	0x44 801208		4	0x4A 3262C8C
281288	CLK2_ISS_BW_REGULATOR.L3_BW_R_BANDWIDTH	0x44 801308		4	0x4A3262 CCD0
282289	CLK2_ISS_BW_REGULATOR.L3_BW_R_WATERMARK	0x44 80130C		4	0x4A 3262D04
283290	CLK2_IVAHD_BW_REGULATOR.L3_BW_R_BANDWIDTH	0x44 801408		4	0x4A 3262D48
284291	CCLK2_IVAHD_BW_REGULATOR.L3_BW_R_WATER-MARK	0x44 80140C		4	0x4A 3262D8C
285292	CLK2_SGX_BW_REGULATOR.L3_BW_R_BANDWIDTH	0x44 801508		4	0x4A3262 DCE0
286293	CLK2_SGX_BW_REGULATOR.L3_BW_R_WATERMARK	0x44 80150C		4	0x4A 3262E04
287294	CLK3_FLAGMUX_CLK3.L3_FLAGMUX_MASK0	0x45 000208		4	0x4A 3262E48
288295	CLK3_FLAGMUX_CLK3.L3_FLAGMUX_MASK1	0x45 000210		4	0x4A 3262E8C
292299	RESTORE_CM2.CM_L3INIT_USB_HOST_CLKCTRL_RES-TORE	0x4A 009E54		4	0x4A3262 ECF0
293300	RESTORE_CM2.CM_L3INIT_USB_TLL_CLKC-TRL_RESTORE	0x4A 009E58		4	0x4A 3262F04
294301	RESTORE_CM2.CM_SDMA_STATICDEP_RESTORE	0x4A 009E5C		4	0x4A 3262F48
296303	USBTLLHS_config.USBTLL_SAR_CNTX_0	0x4A 062400		4	0x4A 3262F8C
297304	USBTLLHS_config.USBTLL_SAR_CNTX_1	0x4A 062404		4	0x4A326 2FC300
298305	USBTLLHS_config.USBTLL_SAR_CNTX_2	0x4A 062408		4	0x4A 3263004
299306	USBTLLHS_config.USBTLL_SAR_CNTX_3	0x4A 06240C		4	0x4A 3263048
300307	USBTLLHS_config.USBTLL_SAR_CNTX_4	0x4A 062410		4	0x4A 326308C
301308	USBTLLHS_config.USBTLL_SAR_CNTX_5	0x4A 062414		4	0x4A3263 0C10

Order	Register Name	Register Start Addr	Register End Addr	Size	SAR RAM Address
~~302~~309	USBTLLHS_config.USBTLL_SAR_CNTX_6	0x4A 062418		4	0x4A 32631~~0~~4
~~303~~310	HSUSBHOST.UHH_SYSCONFIG	0x4A 064010		4	0x4A 32631~~4~~8
~~304~~311	HSUSBHOST.UHH_HOSTCONFIG	0x4A 064040		4	0x4A 32631~~8~~C
~~305~~312	HSUSBHOST.UHH_SAR_CNTX_0	0x4A 064100	0x4A 0646FF	1536	0x4A3263 ~~1~~C20
~~306~~313	RESTORE_CM2.CM_L3INIT_HSUS-BHOST_CLKCTRL_RESTORE	0x4A 009E54		4	0x4A3269 ~~1~~C20
~~307~~314	RESTORE_CM2.CM_L3INIT_HSUS-BTLL_CLKCTRL_RESTORE	0x4A 009E58		4	0x4A 32692~~0~~4
~~308~~315	RESTORE_CM2.CM_SDMA_STATICDEP_RESTORE	0x4A 009E5C		4	0x4A 32692~~4~~8

Table 16.2. SAR_RAM_2 Memory Mapping

Order	Register Name	Register Start Addr	Register End Addr	Size	SAR RAM Address
96	SYSCTRL_PADCONF_CORE. CONTROL_CORE_PAD0_GPMC_AD0_PAD1_GPMC_AD1	0x4A1000 40	0x4A1001 D7	408	0x4A3270 00
97	SYSCTRL_PADCONF_CORE. CONTROL_CORE_PAD0_CSI22_DY2	0x4A1001 F4		4	0x4A3271 98

Table 16.3. SAR_RAM_3 memory mapping

Order	Register Name	Register Start Addr	Register End Addr	Size	SAR RAM Address
140	MPUMA_FW.MRM_PERMISSION_REGION_LOW_0	0x4A20A0 88	0x4A20A0 FF	120	0x4A3282 6C
~~138~~141	PER_AP.L4_AP_PROT_GROUP_MEMBERS_3_L	0x480002 18		4	0x4A3282 E4
~~139~~142	PER_AP.L4_AP_PROT_GROUP_MEMBERS_4_L	0x480002 20		4	0x4A3282 E8
~~140~~143	PER_AP.L4_AP_PROT_GROUP_MEMBERS_5_L	0x480002 28		4	0x4A3282 EC
~~141~~144	PER_AP.L4_AP_PROT_GROUP_MEMBERS_6_L	0x480002 30		4	0x4A3282 F0
~~142~~145	PER_AP.L4_AP_PROT_GROUP_MEMBERS_7_L	0x480002 38		4	0x4A3282 F4
~~143~~146	PER_AP.L4_AP_PROT_GROUP_ROLES_3	0x480002 98	0x480002 9F	8	0x4A3282 F8
~~144~~147	PER_AP.L4_AP_PROT_GROUP_ROLES_4	0x480002 A0	0x480002 A7	8	0x4A3283 00
~~145~~148	PER_AP.L4_AP_PROT_GROUP_ROLES_5	0x480002 A8	0x480002 AF	8	0x4A3283 08
~~146~~149	PER_AP.L4_AP_PROT_GROUP_ROLES_6	0x480002 B0	0x480002 B7	8	0x4A3282 98
~~147~~150	PER_AP.L4_AP_PROT_GROUP_ROLES_7	0x480002 B8	0x480002 BF	8	0x4A3282 A0
~~148~~151	PER_AP.L4_AP_REGION_0_L	0x480003 04		4	0x4A3282 A8
~~149~~152	PER_AP.L4_AP_REGION_3_L	0x480003 1C		4	0x4A3282 AC
~~150~~153	PER_AP.L4_AP_REGION_5_L	0x480003 2C		4	0x4A3282 B0

~~151~~154	PER_AP.L4_AP_REGION_7_L	0x4800033C		4	0x4A3282B4
~~152~~155	PER_AP.L4_AP_REGION_9_L	0x4800034C		4	0x4A3282B8
~~153~~156	PER_AP.L4_AP_REGION_11_L	0x4800035C		4	0x4A3282BC
~~154~~157	PER_AP.L4_AP_REGION_13_L	0x4800036C		4	0x4A3282C0
~~155~~158	PER_AP.L4_AP_REGION_15_L	0x4800037C		4	0x4A3282C4
~~156~~159	PER_AP.L4_AP_REGION_17_L	0x4800038C		4	0x4A3282C8
~~157~~160	PER_AP.L4_AP_REGION_19_L	0x4800039C		4	0x4A3282CC
~~158~~161	PER_AP.L4_AP_REGION_21_L	0x480003AC		4	0x4A3282D0
~~159~~162	PER_AP.L4_AP_REGION_23_L	0x480003BC		4	0x4A3282D4
~~160~~163	PER_AP.L4_AP_REGION_25_L	0x480003CC		4	0x4A3282D8
~~161~~164	PER_AP.L4_AP_REGION_26_L	0x480003D4		4	0x4A3282DC
~~162~~165	PER_AP.L4_AP_REGION_28_L	0x480003E4		4	0x4A3282E0
~~163~~166	PER_AP.L4_AP_REGION_30_L	0x480003F4		4	0x4A3282E4
~~164~~167	PER_AP.L4_AP_REGION_32_L	0x48000404		4	0x4A3282E8
~~165~~168	PER_AP.L4_AP_REGION_34_L	0x48000414		4	0x4A3282EC
~~166~~169	PER_AP.L4_AP_REGION_37_L	0x48000402C		4	0x4A3282F0
~~167~~170	PER_AP.L4_AP_REGION_39_L	0x48000403C		4	0x4A3282F4
~~168~~171	PER_AP.L4_AP_REGION_41_L	0x48000404C		4	0x4A3282F8
~~169~~172	PER_AP.L4_AP_REGION_43_L	0x48000405C		4	0x4A3282FC
~~178~~173	PER_AP.L4_AP_REGION_45_L	0x48000406C		4	0x4A328300
~~171~~174	PER_AP.L4_AP_REGION_47_L	0x48000407C		4	0x4A328304
~~172~~175	PER_AP.L4_AP_REGION_49_L	0x48000408C		4	0x4A328308
~~173~~176	PER_AP.L4_AP_REGION_51_L	0x48000409C		4	0x4A32830C
.....	.....	.....	.....	.....	.....
~~237~~240	CFG_AP.L4_AP_REGION_90_L	0x4A0005D4		4	0x4A32848C
~~238~~241	CFG_AP.L4_AP_REGION_91_L	0x4A0005DC		4	0x4A328490
242	CFG_AP.L4_AP_REGION_92_L	0x4A0005E4		4	0x4A328494
243	CFG_AP.L4_AP_REGION_93_L	0x4A0005EC		4	0x4A328498

244	CFG_AP.L4_AP_REGION_94_L	0x4A0005F4		4	0x4A32849C
245	CFG_AP.L4_AP_REGION_95_L	0x4A0005FC		4	0x4A3284A0

16.5. sDMA Basic Programming Model

Refer to OMAP4460 Silicon Revision 1.x TRM.

16.6. sDMA Register Manual

Refer to OMAP4460 Silicon Revision 1.x TRM.

Chapter 17. Interrupt Controllers

This chapter describes differences in Interrupt Controllers between the OMAP4430 Silicon Revision 2.x and OMAP4460 Silicon Revision 1.x multimedia devices.

17.1. Interrupt Controllers Overview

Refer to OMAP4460 Silicon Revision 1.x TRM.

17.2. Interrupt Controllers Environment

Refer to OMAP4460 Silicon Revision 1.x TRM.

17.3. Interrupt Controllers Integration

17.3.1. Interrupts Mapping

Refer to OMAP4460 Silicon Revision 1.x TRM.

17.3.2. Interrupt Requests to Cortex-A9 MPU INTC

- New interrupt requests are added:
  - THERMAL_ALERT interrupt from General CORE Control Module thermal sensor, mapped to interrupt line MA_IRQ_126;
  - CMU_IRQ_P interrupt from Cache Managment Unit, mapped to interrupt line MA_IRQ_5;
  - CORTEXA9_CPU0_PMU_IRQ interrupt from Cortex-A9 CPU0 PMU, mapped to interrupt line MA_IRQ_54;
  - CORTEXA9_CPU1_PMU_IRQ interrupt from Cortex-A9 CPU1 PMU, mapped to interrupt line MA_IRQ_55;

17.3.3. Interrupt Requests to Cortex-M3 MPU INTC

Refer to OMAP4460 Silicon Revision 1.x TRM.

17.4. Interrupt Controllers Functional Description

Refer to OMAP4460 Silicon Revision 1.x TRM.

17.5. Interrupt Controllers Register Manual

Refer to OMAP4460 Silicon Revision 1.x TRM.

Chapter 18. Control Module

This chapter describes differencies in the Control Module between the OMAP4430 Silicon Revision 2.x and OMAP4460 Silicon Revision 1.x.

18.1. Control Module Overview

Refer to OMAP4460 Silicon Revision 1.x TRM.

18.2. Control Module Environment

Refer to OMAP4460 Silicon Revision 1.x TRM.

18.3. Control Module Integration

-The clock WKUP_32K_FCLK is no longer used to drive the VBGAPTS module. The clock schema is changed, as follows :

- New PRCM clock -WKUP_TS_FCLK drives the VBGAPTS cell clock input.

- CORE_TS_FCLK clock which duplicates WKUP_TS_FCLK is added to drive the instantiated inside General Core Control Module band gap fsm logic and its band gap counter.

- One IRQ - THERMAL_ALERT is generated at General Core Control module level and delivered to the Cortex-A9 INTC.- The TSHUT signal to GPIO3 is now generated by the General Core Control module, and not by the VBGAPTS cell.These changes impact :

- Figure Control Module Overview
- Subsection *Control Module Integration*
  - Table *Clocks and Resets*
  - Figure *Control Module Integration*
  - A new Table - *Hardware Requests* is inserted
- Other subsections - for more information refer to sections *Section 18.4.2 , Control Module Clock Configuration, Section 18.4.5, Hardware Requests* and *Band Gap Voltage and Temperature Sensor, Section 18.4.10*

18.4. Control Module Functional Description

18.4.1. Control Module Block Diagram

Refer to OMAP4460 Silicon Revision 1.x TRM.

18.4.2. Control Module Clock Configuration

The addition of clock CORE_TS_FCLK and its local gating at General Core Control module (through bit CONTROL_TEMP_SENSOR [13] BGAP_TEMPSOFF) impacts:

- Subsection *Control Module Clock Configuration*
  - Figure *Control Module Internal Clock Paths*

18.4.3. Control Module Software Reset

Refer to OMAP4460 Silicon Revision 1.x TRM.

18.4.4. Control Module Power Management

Refer to OMAP4460 Silicon Revision 1.x TRM.

18.4.5. Hardware Requests

One interrupt request (THERMAL_ALERT) is generated by General Core Control module to the MPUSS.

18.4.6. Control Module Initialization

Refer to OMAP4460 Silicon Revision 1.x TRM.

18.4.7. Control Module Instances

18.4.7.1. General Core Control Module Instance

Following new registers are introduced in the SYSCTRL_GENERAL_CORE instance:

- CONTROL_EMIF1_OFFSET
- CONTROL_EMIF2_OFFSET
- CONTROL_EMIF1_MASTER_CODE_0
- CONTROL_EMIF1_MASTER_CODE_1
- CONTROL_EMIF2_MASTER_CODE_0
- CONTROL_EMIF2_MASTER_CODE_1
- CONTROL_BANDGAP_CTRL
- CONTROL_BANDGAP_COUNTER
- CONTROL_BANDGAP_THRESHOLD
- CONTROL_TSHUT_THRESHOLD
- CONTROL_BANDGAP_STATUS
- CONTROL_FORCEWRNP

Introduction of VDD_CORE OPP119 (Overdrive Mode) to OMAP4460 Silicon Revision 1.x impacts the OPP eFUSE registers: CONTROL_STD_FUSE_OPP_VDD_CORE_1 and CONTROL_STD_FUSE_OPP_VDD_CORE_2. Two new bitfields are added inside each of them, correspondingly.
Introduction of OPP_NITRO for the VDD_IVA voltage domain to OMAP4460 Silicon Revision 1.x impacts the OPP eFUSE register: CONTROL_STD_FUSE_OPP_VDD_IVA_2. Four new bitfields for VDD_IVA OPP_NITRO Ntarget efuse values monitoring are added at location (31:8).
Introduction of OPP_NTSB for the VDD_IVA voltage domain in OMAP4460 Silicon Revision 1.x impacts the OPP eFUSE registers:

- CONTROL_STD_FUSE_OPP_VDD_IVA_3

Four new bitfields for VDD_IVA are added at location (23:0) in the register CONTROL_STD_FUSE_OPP_VDD_IVA_3.OPP_NTSB replaces OPP_NITRO1.2G in VDD_MPU voltage domain in OMAP4460 Silicon Revision 1.x, which impacts the OPP Efuse register:

- CONTROL_STD_FUSE_OPP_VDD_MPU_3

The four bitfields assigned to monitor the OMAP4430 - VDD_MPU OPP_NITRO1.2G Ntarget efuse values at location 23:0 of the CONTROL_STD_FUSE_OPP_VDD_MPU_3 , are replaced with the corresponding VDD_MPU OPP_NTSB Ntarget efuse bitfields following the same format.Three new bitfields are introduced inside the register CONTROL_STD_FUSE_OPP_DPLL_1, to reflect updates in the device Adaptive Body Bias (ABB) strategy :

1. CONTROL_STD_FUSE_OPP_DPLL_1 [21] IVA_RBB_TURBO

2. CONTROL_STD_FUSE_OPP_DPLL_1 [20] MPU_RBB_TURBO

3. CONTROL_STD_FUSE_OPP_DPLL_1 [19:18] MPU_DPLL_TRIM_FREQ

ABB Set2 is introduced for both IVA and MPU OPP_TURBO, and this impacts two registers:

- Three bitfields are added inside the register CONTROL_LDOVBB_IVA_VOLTAGE_CTRL :
  1. CONTROL_LDOVBB_IVA_VOLTAGE_CTRL [26] LDOVBBIVA_RBB_MUX_CTRL
  2. CONTROL_LDOVBB_IVA_VOLTAGE_CTRL [25:21] LDOVBBIVA_RBB_VSET_IN
  3. CONTROL_LDOVBB_IVA_VOLTAGE_CTRL [20:16] LDOVBBIVA_RBB_VSET_OUT
- Three bitfields are added inside the register CONTROL_LDOVBB_MPU_VOLTAGE_CTRL:
  1. CONTROL_LDOVBB_MPU_VOLTAGE_CTRL [26] LDOVBBMPU_RBB_MUX_CTRL
  2. CONTROL_LDOVBB_MPU_VOLTAGE_CTRL [25:21] LDOVBBMPU_RBB_VSET_IN
  3. CONTROL_LDOVBB_MPU_VOLTAGE_CTRL [20:16] LDOVBBMPU_RBB_VSET_OUT

18.4.7.2. General Wakeup Control Module Instance

Refer to OMAP4460 Silicon Revision 1.x TRM.

18.4.7.3. Device Core Control Module Instance

Following changes are valid for the SYSCTRL_PADCONF_CORE register set :

- The unused in OMAP4430 Silicon Revision 2.x - MSB bits - [31:16] of the register CONTROL_CORE_PAD0_DPM_EMU19 are dedicated to configure the added new pad - csi22_dx2, and register is renamed to CONTROL_CORE_PAD0_DPM_EMU19_PAD1_CSI22_DX2. Refer to Table 18.2 for more information about these changes.
- New padconf register is added in CORE domain - CONTROL_CORE_PAD0_CSI22_DY2, to configure the new pad - csi22_dy2. Refer to Table 18.2 for more information about these changes.

18.4.7.4. Device Wakeup Control Module Instance

Refer to OMAP4460 Silicon Revision 1.x TRM.

18.4.8. PAD Functional Multiplexing and Configuration

Following updates are done to pad functional multiplexing and configuration schema :

- Pad multiplexing schema in WAKEUP domain is updated as follows:
  - Hardware observability signal hw_dbg0 is remuxed on WKUP domain pad - sys_pwron_reset_out. This impacts register CONTROL_WKUP_PAD0_SYS_PWR_REQ_PAD1_SYS_PWRON_RESET_OUT
  - c2c_pwkup signal is added in the mux set of the WKUP domain pad - gpio_wk0. This impacts register CONTROL_WKUP_PAD0_GPIO_WK0_PAD1_GPIO_WK1

  Refer to Table 18.1 for more details on WKUP mux mapping .
- Pad multiplexing schema in CORE domain is updated as follows:
  - Part of the new parallel camera interface signals : cam2_d0 - cam2_d7 are available in MuxMode=0x1 on pads: csi22_dy1, csi22_dx1, csi22_dy0, csi22_dx0, csi21_dy4, csi21_dx4, csi21_dy3, csi21_dx3.
    This impacts registers:
    - CONTROL_CORE_PAD0_CSI22_DX1_PAD1_CSI22_DY1
    - CONTROL_CORE_PAD0_CSI22_DX0_PAD1_CSI22_DY0
    - CONTROL_CORE_PAD0_CSI21_DX4_PAD1_CSI21_DY4
    - CONTROL_CORE_PAD0_CSI21_DX3_PAD1_CSI21_DY3
    - CONTROL_CAMERA_RX
  - Full set of new parallel camera interface signals : cam2_d0 - cam2_d15, cam2_fid, cam2_wen, cam2_hs, cam2_vs and cam2_pclk is covered in MuxMode=0x2 on pads :
    kpd_col0 - kpd_col5 , kpd_row0 - kpd_row5, csi22_dx0, csi22_dy0, csi22_dx1, csi22_dy1, csi22_dx2, csi22_dy2, cam_shutter, cam_strobe, cam_globalreset.
    This impacts registers:
    - CONTROL_CORE_PAD0_KPD_COL3_PAD1_KPD_COL4
    - CONTROL_CORE_PAD0_KPD_COL5_PAD1_KPD_COL0
    - CONTROL_CORE_PAD0_KPD_COL1_PAD1_KPD_COL2
    - CONTROL_CORE_PAD0_KPD_ROW3_PAD1_KPD_ROW4
    - CONTROL_CORE_PAD0_KPD_ROW5_PAD1_KPD_ROW0
    - CONTROL_CORE_PAD0_KPD_ROW1_PAD1_KPD_ROW2
    - CONTROL_CORE_PAD0_CSI22_DX0_PAD1_CSI22_DY0
    - CONTROL_CORE_PAD0_CSI22_DX1_PAD1_CSI22_DY1
    - CONTROL_CORE_PAD0_CAM_SHUTTER_PAD1_CAM_STROBE
    - CONTROL_CORE_PAD0_CAM_GLOBALRESET_PAD1_USBB1_ULPITLL_CLK
  - Camera timing control interface signals - cam_globalreset, cam_shutter, cam_strobe are also available in MuxMode=0x2 on the UART3 pads :
    uart3_rts_sd, uart3_rx_irrx, uart3_tx_irtx
    This impacts registers:
    - CONTROL_CORE_PAD0_UART3_CTS_RCTX_PAD1_UART3_RTS_SD
    - CONTROL_CORE_PAD0_UART3_RX_IRRX_PAD1_UART3_TX_IRTX
  - Register CONTROL_CORE_PAD0_HDQ_SIO_PAD1_I2C1_SCL - the I2C1_SCL_PULLUDENABLE and the I2C1_SCL_PULLTYPESELECT bit power-on reset values are changed to '0' to disable internal weak PU/PD resistor at i2c1_scl pad by default.
  - Register CONTROL_WKUP_PAD0_SYS_NRESPWRON_PAD1_SYS_NRESWARM- the SYS_NRESPWRON_PULLTYPESELECT and SYS_NRESPWRON_PULLUDENABLE bits are changed to RESERVED with access changed to read only.
  - Power-on reset values of bits CONTROL_WKUP_PAD0_GPIO_WK4_PAD1_SR_SCL [20] SR_SCL_PULLTYPESELECT and CONTROL_WKUP_PAD0_GPIO_WK4_PAD1_SR_SCL [19] SR_SCL_PULLUDENABLE are changed from 0x1 to 0x0, i.e. SR_SCL pad internal pulls are disabled by default.
  - Power-on reset values of bits CONTROL_WKUP_PAD0_SR_SDA_PAD1_FREF_XTAL_IN [4] SR_SDA_PULLTYPESELECT and CONTROL_WKUP_PAD0_SR_SDA_PAD1_FREF_XTAL_IN [3] SR_SDA_PULLUDENABLE are changed from 0x1 to 0x0, i.e. SR_SDA pad internal pulls are disabled by default.
  - Register CONTROL_I2C_0 - the I2C1_SCL_LOAD_BITS and I2C1_SDA_LOAD_BITS bitfield power-on reset values are changed from 0x1 to 0x2.
- Duplicate wake-up event monitoring feature is updated as follows:

- Two bits are added to the register CONTROL_PADCONF_WAKEUPEVENT_6 to duplicate wake up event monitoring for the new pads - csi22_dx2 and csi22_dy2.

Refer to Table 18.2 for more details on CORE domain mux mapping .

The pad-configuration muxmode sets are updated as follows:

Table 18.1. Device Wakeup Control Module Pad Configuration Register Fields

SYSCTRL_GENERAL_WKUP.[Register name]	Address Offset	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
CONTROL_WKUP_PAD0_GPIO_WK0_PAD1_GPIO_WK1[15:0]	0x040	reserved			gpio_wk0	c2c_pwkup		hw_dbg1	safe_mode
CONTROL_WKUP_PAD0_SYS_PWR_REQ_PAD1_SYS_PWRON_RESET_OUT[31:16]	0x064	sys_pwron_reset_out			gpio_wk29		hw_dbg0	hw_dbg11	

Table 18.2. Device Core Control Module Pad Configuration Register Fields

SYSCTRL_GENERAL_CORE.[Register Name]	Address Offset	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
CONTROL_CORE_PAD0_CSI21_DX3_PAD1_CSI21_DY3[15:0]	0x0AC	csi21_dx3	cam2_d7		gpi_73				safe_mode
CONTROL_CORE_PAD0_CSI21_DX3_PAD1_CSI21_DY3[31:16]	0x0AC	csi21_dy3	cam2_d6		gpi_74				safe_mode
CONTROL_CORE_PAD0_CSI21_DX4_PAD1_CSI21_DY4[15:0]	0x0B0	csi21_dx4	cam2_d5		gpi_75				safe_mode

SYSCTRL_GENERAL_CORE.[Register Name]	Address Offset	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
CONTROL_CORE_PAD0_CSI21_DX4_PAD1_CSI21_DY4[31:16]	0x0B0	csi21_dy4	cam2_d4		gpi_76				safe_mode
CONTROL_CORE_PAD0_CSI22_DX0_PAD1_CSI22_DY0[15:0]	0x0B4	csi22_dx0	cam2_d3	cam2_d12	gpi_77				safe_mode
CONTROL_CORE_PAD0_CSI22_DX0_PAD1_CSI22_DY0[31:16]	0x0B4	csi22_dy0	cam2_d2	cam2_d13	gpi_78				safe_mode
CONTROL_CORE_PAD0_CSI22_DX1_PAD1_CSI22_DY1[15:0]	0x0B8	csi22_dx1	cam2_d1	cam2_d14	gpi_79				safe_mode
CONTROL_CORE_PAD0_CSI22_DX1_PAD1_CSI22_DY1[31:16]	0x0B8	csi22_dy1	cam2_d0	cam2_d15	gpi_80				safe_mode
CONTROL_CORE_PAD0_CAM_SHUTTER_PAD1_CAM_STROBE[15:0]	0x0BC	cam_shutter		cam2_hs	gpio_81				safe_mode
CONTROL_CORE_PAD0_CAM_SHUTTER_PAD1_	0x0BC	cam_strobe		cam2_vs	gpio_82				safe_mode

SYSCTRL_GENERAL_CORE.[Register Name]	Address Offset	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
CAM_STROBE[31:16]									
CONTROL_CORE_PAD0_CAM_GLOBALRESET_PAD1_USBB1_ULPITLL_CLK[15:0]	0x0C0	cam_globalreset		cam2_pclk	gpio_83				safe_mode
CONTROL_CORE_PAD0_UART3_CTS_RC-TX_PAD1_UART3_RTS_SD[31:16]	0x140	uart3_rts_sd		cam_globalreset	gpio_142				safe_mode
CONTROL_CORE_PAD0_UART3_RX_IRRX_PAD1_UART3_TX_IRTX[15:0]	0x144	uart3_rx_irrx	dmtimer8_pwm_evt	cam_shutter	gpio_143				safe_mode
CONTROL_CORE_PAD0_UART3_RX_IRRX_PAD1_UART3_TX_IRTX[31:16]	0x144	uart3_tx_irtx	dmtimer9_pwm_evt	cam_strobe	gpio_144				safe_mode
CONTROL_CORE_PAD0_KPD_COL3_PAD1_KPD_COL4[15:0]	0x17C	kpd_col3	kpd_col0	cam2_d0	gpio_171				safe_mode
CONTROL_CORE_PAD0_KPD_COL3_PAD1_KPD_COL4[31:16]	0x17C	kpd_col4	kpd_col1	cam2_d1	gpio_172				safe_mode
CONTROL_CORE	0x180	kpd_col5	kpd_col2	cam2_d2	gpio_173				safe_mode

SYSCTRL_GENERAL_CORE.[Register Name]	Address Offset	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
_PAD0_KPD_COL5_PAD1_KPD_COL0[15:0]									
CONTROL_CORE_PAD0_KPD_COL5_PAD1_KPD_COL0[31:16]	0x180	kpd_col0	kpd_col3	cam2_d3	gpio_174				safe_mode
CONTROL_CORE_PAD0_KPD_COL1_PAD1_KPD_COL2[15:0]	0x184	kpd_col1	kpd_col4	cam2_d8	gpio_0				safe_mode
CONTROL_CORE_PAD0_KPD_COL1_PAD1_KPD_COL2[31:16]	0x184	kpd_col2	kpd_col5	cam2_d10	gpio_1				safe_mode
CONTROL_CORE_PAD0_KPD_ROW3_PAD1_KPD_ROW4[15:0]	0x188	kpd_row3	kpd_row0	cam2_d4	gpio_175				safe_mode
CONTROL_CORE_PAD0_KPD_ROW3_PAD1_KPD_ROW4[31:16]	0x188	kpd_row4	kpd_row1	cam2_d5	gpio_176				safe_mode
CONTROL_CORE_PAD0_KPD_ROW5_PAD1_KPD_ROW0[15:0]	0x18C	kpd_row5	kpd_row2	cam2_d6	gpio_177				safe_mode
CONTROL_CORE_PAD0_KPD_ROW5_PAD1_KPD_ROW0[31:16]	0x18C	kpd_row0	kpd_row3	cam2_d7	gpio_178				safe_mode

SYSCTRL_GENERAL_CORE.[Register Name]	Address Offset	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7
CONTROL_CORE_PAD0_KPD_ROW1_PAD1_KPD_ROW2[15:0]	0x190	kpd_row1	kpd_row4	cam2_d9	gpio_2				safe_mode
CONTROL_CORE_PAD0_KPD_ROW1_PAD1_KPD_ROW2[31:16]	0x190	kpd_row2	kpd_row5	cam2_d11	gpio_3				safe_mode
~~CONTROL_CORE_PAD0_DPM_EMU19[15:0]~~ CONTROL_CORE_PAD0_DPM_EMU19_PAD1_CSI22_DX2[15:0]	0x1D4	dpm_emu19	dmtimer11_pwm_evt	dsi2_te1	gpio_191	rfbi_data0	dispc2_data0	hw_dbg19	safe_mode
CONTROL_CORE_PAD0_DPM_EMU19_PAD1_CSI22_DX2[31:16]	0x1D4	csi22_dx2		cam2_fid					safe_mode
CONTROL_CORE_PAD0_CSI22_DY2[15:0]	0x1F4	csi22_dy2		cam2_wen					safe_mode

18.4.9. Extended-Drain I/O and PBIAS Cell

Change in the multiplex mapping has the following impact :

Besides for the gpio_wk0 and hw_dbg1 signals, the PBIAS1 cell need to be also configured when c2c_pwkup signal is selected on the gpio_wk0 pad in WKUP domain.

18.4.10. Band Gap Voltage and Temperature Sensor

Thermal management schema is updated as follows :

- The device thermal operation requirements are changed between OMAP4460 and OMAP4430. In OMAP4460 Silicon Revision 1.x, the temperature offset between the on-die temperature sensor measured value and the on-die hottest spot temperature is decreased (although still significant) due to temperature sensor closer location to the MPU on the device die. For more details refer to your TI representative.

- The thermal sensor parameters are changed between OMAP4460 and OMAP4430. For more details refer to your TI representative.
- VBGAPTS cell is modified as follows:
  - The VBGAPTS clock input (VBGAPTS signal name CLK) no longer uses 32kHZ clock (WKUP_32K_FCLK). A new PRCM clock - WKUP_TS_FCLK adjustable in the range (1MHz -2MHz) is used to drive it .
  - 10-bit ADC is introduced in VBGAPTS. As a consequence, DTEMP bus size is increased from 8-bit to 10-bit.
  - The embedded TSHUT comparator is removed from VBGAPTS cell, and implemented at General Core Control Module level.
  - Bitfield CONTROL_TEMP_SENSOR[11] TSHUT is removed.
  - Single conversion mode is always enabled at VBGAPTS level. The VBGAPTS continuous conversion mode is no longer used. The bitfield CONTROL_TEMP_SENSOR[12] CONTCONV is "RESERVED" .
- A new bandgap interface logic -a bandgap state machine with an embedded 24-bit band gap counter is instantiated inside the General Core Control module, to help VBGAPTS cell accomplish different temperature measurement modes.
- A new clock - CORE_TS_FCLK (1MHz - 2MHz) is introduced to drive the band gap logic located in the General Core Control module. There is added functionality for the CONTROL_TEMP_SENSOR[13] BGAP_TEMPSOFF. Not only disables it the VBGAPTS CLK, but also the CORE_TS_FCLK when setting bandgap logic in OFF mode.
- A new flag - CONTROL_BANDGAP_STATUS[3] CLEAN_STOP is added to insure bandgap state machine is in IDLE state before band gap clock is switched off in software.
- Timing relations between signals in single conversion mode are changed.
- The work in continuous mode is simulated through sequences of single conversions automatically performed by the new band-gap state machine in General Core Control module.
- The old continuous conversion mode is replaced by two other single-repeat conversion modes:
  - Fixed-delay single repeat conversion
  - Programmable-delay single repeat conversion
- A new bitfield - CONTROL_BANDGAP_CTRL[31] SINGLE_MODE is introduced at the General Core Control leve to switch between a programmable-delay single repeat conversion or fixed-delay / single conversion modes.
- A new bitfield - CONTROL_BANDGAP_COUNTER[23:0] COUNTER is introduced at the General Core Control leve to program the periods of automatic SOC pulse insertions between two consecutive conversions.
- Timing relations between interface signals in single repeat conversion mode are changed.
- A thermal data post-processing logic which consist of two comparator blocks is instantiated in the General Core Control module. It allows for two separately programmable functional outputs - THERMAL ALERT and TSHUT. The THERMAL ALERT is mapped as an interrupt on the MPUSS.
- Programmable LOW and HI hysteresis thresholds are available to each of the THERMAL ALERT and TSHUT outputs, to maintain output stability as temperature decreases.
- Following new registers are added in the General Core Control module space to configure thermal data post-processing functionalities:
  - CONTROL_BANDGAP_CTRL
  - CONTROL_BANDGAP_THRESHOLD
  - CONTROL_TSHUT_THRESHOLD
  - CONTROL_BANDGAP_STATUS
- The above stated changes impact section *Band Gap Voltage and Temperature Sensor :*
  - Updated figure *Functional Block Diagram*
  - Updated table *Band Gap Voltage and Temperature Sensor Signal Description*
  - Added table *General Core Control Thermal Logic Outputs Description*
  - Updated figure *Single Conversion Mode*
  - Section - *Repeat-Single Conversion Mode* (previously entitled Continuous Conversion Mode) is divided into two new subsections - *Fixed-Delay Repeated Single Conversions* and *Programmable-Delay Repeated Single Conversions*
  - A new section called *Thermal Data Post-Processing Logic* is added
  - Table *ADC Code Versus Temperature* is updated

18.4.11. Hardware Observability

18.4.11.1. Device Internal Signals Observability Overview

Refer to OMAP4460 Silicon Revision 1.x TRM.

18.4.11.2. Observability Gating Capabilities

Dividers are added on paths of the hw_dbg1 and hw_dbg2 observability signals in CORE power domain. This change impacts the CONTROL_HWOBS_CONTROL register . The [13:9] and [18:14] bitfields are no longer RESERVED, and are now used to program the observable signal clock divider ratios - HWOBS_CLKDIV_SEL_1 (for hwobs_dbg1) and HWOBS_CLKDIV_SEL_2 (for hwobs_dbg2).The addition of HWOBS_CLKDIV_SEL_1 and HWOBS_CLKDIV_SEL_2 bitfields impacts sections :

- *Device Internal Signals Observability Overview*
  - Figure : *Overview of the Hardware Observability Functionality*
- *Observability Gating Capabilities*

18.4.11.3. Observability Signals Multiplexing at General Core/Wakeup Control Level

The Video DAC (VDAC) functionality is not supported.

18.4.11.4. Observability Signals Multiplexing at Device Core Control Level

The signal hw_dbg0 can be muxed in the WKUP domain (MuxMode=0x5) by the Device Wakeup Control Module. Refer to Table 18.1 for more information.

18.4.11.5. Observability Signals Sourced at Module Level

Dual Cortex-A9 Subsystem Observable Signals muxing is changed as follows:

- "ARM_FCLK/ 16" signal is replaced by "PIDPLLIDLE" signal on the hwobs_int_mpu[3] line when CONTROL_DEBOBS_MMR_MPU [3:0] SELECT = 0x0. This impacts table *Observability Signals Multiplexing at Cortex-A9 MPUSS Level - Mode 0*
- Following Clock Signals are replaced in the CONTROL_DEBOBS_MMR_MPU [3:0] SELECT = 0x1 - mux set. on the hwobs_int_mpu[8] line.This impacts table *Observability Signals Multiplexing at Cortex-A9 MPUSS Level - Mode 1.*
  - "ARM_FCLK_enb / 8" signal is replaced by "aclk_abe_final_phase" signal on the hwobs_int_mpu[8] line
  - "DPLLInitZ" signal is replaced by "aclk_l3_final_phase" signal on the hwobs_int_mpu[7] line
- 4 Mux sets are added and extend MPUSS observability up to 12 set of signals , i.e. CONTROL_DEBOBS_MMR_MPU [3:0] SELECT range of valid values (0x0 - 0x7) is extended to (0x0 - 0xB) range. Copy of EMIF clock and ARM_FCLK / 16 are remuxed in these sets. As a consequence - 4 new tables are added in *Dual Cortex-A9 Subsystem Observable Signals* section.
- There are changes in multiplexing values selecting different CM2/CM1/PRM observability signal sets, as well as changes in CM2/CM1/PRM signals mapping to the debugcm2(i), debugcm1(i) and debugprm(i) hwobs inputs of the General Control Module, where (i=0 to 7). The changes impact the tables:
  - *CM2 Subsystem Observable Signals*
  - *CM1 Subsystem Observable Signals*
  - *PRM Subsystem Observable Signals*

  The Video DAC (VDAC) functionality is not supported

18.4.12. Functional Register Description

- A new register - CONTROL_FORCEWRNP is introduced in the General Core Control module to allow forcing only non-posted write transactions from MPUSS to L3 interconnect.
- Two registers are added inside the General Core Control module to program signed offsets for individual DLL slave delay compensation in EMIF1 and EMIF2 instances :
  - CONTROL_EMIF1_OFFSET
  - CONTROL_EMIF2_OFFSET
- Four new RO registers inside General Core Control module provide monitoring of the four DLL MASTER code values transfered to the four EMIF DLL Slaves (EMIF1,EMIF2) :
  - CONTROL_EMIF1_MASTER_CODE_0
  - CONTROL_EMIF1_MASTER_CODE_1
  - CONTROL_EMIF2_MASTER_CODE_0
  - CONTROL_EMIF2_MASTER_CODE_1
- The changes have following impact:
  - A new subsection is added - *EMIF DLL Master / Slave Specific Registers*
  - A new subsection is added - *Force MPU Write Nonposted Transactions Control Registerr*
- One more bit is added in the CONTROL_CAMERA_RX register for enabling the new CSI22 lane.

18.4.12.1. DSP Boot Register

Refer to OMAP4460 Silicon Revision 1.x TRM.

18.4.12.2. Temperature Sensor Control Register

The section is updated with the new five registers related to thermal management :

- CONTROL_BANDGAP_CTRL
- CONTROL_BANDGAP_COUNTER
- CONTROL_BANDGAP_THRESHOLD
- CONTROL_TSHUT_THRESHOLD
- CONTROL_BANDGAP_STATUS

18.4.12.3. Protection Status Registers

Refer to OMAP4460 Silicon Revision 1.x TRM.

18.4.12.4. Protection SDRAM Configuration Registers

Refer to OMAP4460 Silicon Revision 1.x TRM.

18.4.12.5. Register Controls for the LPDDR2IO1 / LPDDR2IO2 I/O Buffer Modes

Refer to OMAP4460 Silicon Revision 1.x TRM.

18.4.12.6. Reference voltage for OMAP LPDDR2IO1 / LPDDR2IO2 I/O buffers and LPDDR2 memory

Refer to OMAP4460 Silicon Revision 1.x TRM.

18.4.12.7. EMIF DLL Master/Slave Specific Registers

New section added.

18.4.12.8. Force MPU Write Nonposted Transactions Control Register

New section added.

18.4.12.9. Signal Integrity Parameter Control Registers With Pad Group Assignment

Refer to OMAP4460 Silicon Revision 1.x TRM.

18.4.12.10. Dual Voltage-Supplied Peripheral Controls

Refer to OMAP4460 Silicon Revision 1.x TRM.

18.5. Control Module Programming Guide

The introduction of CORE_TS_FCLK functional clock for the General Core Control thermal logic impacts sections:

- *Surrounidng Modules Global Initialization*
- *Clock Gating Configuration*

The addition of HWOBS_CLKDIV_SEL_1 and HWOBS_CLKDIV_SEL_2 bitfields in the CONTROL_HWOBS_CONTROL register impacts section :

- *Hardware Observability Settings*
- *Device Internal Signals Observability Overview*
  - Figure : *Overview of the Hardware Observability Functionality*
- *Observability Gating Capabilities*

The Video DAC (VDAC) functionality is not supported

18.6. Control Module Register Manual

18.6.1. Control Module Instance Summary

Table 18.3. Control Module Instance Summary

Module instance	Base Address	Size	Description
SYSCTRL_GENERAL_CORE	0x4A00 2000	4KB	Module
SYSCTRL_GENERAL_WKUP	0x4A30 C000	4KB	Module
SYSCTRL_PADCONF_CORE	0x4A10 0000	4KB	Module
SYSCTRL_PADCONF_WKUP	0x4A31 E000	4KB	Module

18.6.2. SYSCTRL_GENERAL_CORE Register Summary

Table 18.4. SYSCTRL_GENERAL_CORE Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	SYSCTRL_GENERAL_CORE Physical Address
CONTROL_GEN_CORE_REVISION	R	32	0x00000000	0x4A002000
CONTROL_GEN_CORE_HWINFO	R	32	0x00000004	0x4A002004
CONTROL_GEN_CORE_SYSCONFIG	RW	32	0x00000010	0x4A002010
CONTROL_STD_FUSE_DIE_ID_0	R	32	0x0000 0200	0x4A00 2200
CONTROL_ID_CODE	R	32	0x0000 0204	0x4A00 2204
CONTROL_STD_FUSE_DIE_ID_1	R	32	0x0000 0208	0x4A00 2208
CONTROL_STD_FUSE_DIE_ID_2	R	32	0x0000 020C	0x4A00 220C
CONTROL_STD_FUSE_DIE_ID_3	R	32	0x0000 0210	0x4A00 2210
CONTROL_STD_FUSE_PROD_ID_0	R	32	0x0000 0214	0x4A00 2214
CONTROL_STD_FUSE_PROD_ID_1	R	32	0x0000 0218	0x4A00 2218
CONTROL_STD_FUSE_USB_CONF	R	32	0x0000 021C	0x4A00 221C
CONTROL_STD_FUSE_CONF	R	32	0x0000 0220	0x4A00 2220
CONTROL_STD_FUSE_OPP_VDD_WKUP	R	32	0x0000 0228	0x4A00 2228
CONTROL_STD_FUSE_OPP_VDD_IVA_0	R	32	0x0000 022C	0x4A00 222C
CONTROL_STD_FUSE_OPP_VDD_IVA_1	R	32	0x0000 0230	0x4A00 2230
CONTROL_STD_FUSE_OPP_VDD_IVA_2	R	32	0x0000 0234	0x4A00 2234
CONTROL_STD_FUSE_OPP_VDD_IVA_3	R	32	0x0000 0238	0x4A00 2238
RESERVED	R	32	0x0000 023C	0x4A00 223C
CONTROL_STD_FUSE_OPP_VDD_MPU_0	R	32	0x0000 0240	0x4A00 2240

Register Name	Type	Register Width (Bits)	Address Offset	SYSCTRL_GENERAL_CORE Physical Address
CONTROL_STD_FUSE_OPP_VDD_MPU_1	R	32	0x0000 0244	0x4A00 2244
CONTROL_STD_FUSE_OPP_VDD_MPU_2	R	32	0x0000 0248	0x4A00 2248
CONTROL_STD_FUSE_OPP_VDD_MPU_3	R	32	0x0000 024C	0x4A00 224C
RESERVED	R	32	0x0000 0250	0x4A00 2250
CONTROL_STD_FUSE_OPP_VDD_CORE_0	R	32	0x0000 0254	0x4A00 2254
CONTROL_STD_FUSE_OPP_VDD_CORE_1	R	32	0x0000 0258	0x4A00 2258
CONTROL_STD_FUSE_OPP_VDD_CORE_2	R	32	0x0000 025C	0x4A00 225C
CONTROL_STD_FUSE_OPP_BGAP	R	32	0x0000 0260	0x4A00 2260
CONTROL_STD_FUSE_OPP_DPLL_0	R	32	0x0000 0264	0x4A00 2264
CONTROL_STD_FUSE_OPP_DPLL_1	R	32	0x0000 0268	0x4A00 2268
CONTROL_STATUS	R	32	0x0000 02C4	0x4A00 22C4
CONTROL_SEC_ERR_STATUS_FUNC	RW	32	0x0000 02D0	0x4A00 22D0
CONTROL_SEC_ERR_STATUS_DEBUG	RW	32	0x0000 02D4	0x4A00 22D4
RESERVED	R	32	0x0000 02D8	0x4A00 22D8
RESERVED	R	32	0x0000 02DC	0x4A00 22DC
CONTROL_DEV_CONF	RW	32	0x0000 0300	0x4A00 2300
CONTROL_DSP_BOOTADDR	RW	32	0x0000 0304	0x4A00 2304
CONTROL_LDOVBB_IVA_VOLTAGE_CTRL	RW	32	0x0000 0314	0x4A00 2314
CONTROL_LDOVBB_MPU_VOLTAGE_CTRL	RW	32	0x0000 0318	0x4A00 2318
CONTROL_LDOSRAM_IVA_VOLTAGE_CTRL	RW	32	0x0000 0320	0x4A00 2320
CONTROL_LDOSRAM_MPU_VOLTAGE_CTRL	RW	32	0x0000 0324	0x4A00 2324
CONTROL_LDOSRAM_CORE_VOLTAGE_CTRL	RW	32	0x0000 0328	0x4A00 2328
CONTROL_TEMP_SENSOR	RW	32	0x0000 032C	0x4A00 232C
CONTROL_DPLL_NWELL_TRIM_0	RW	32	0x0000 0330	0x4A00 2330
CONTROL_DPLL_NWELL_TRIM_1	RW	32	0x0000 0334	0x4A00 2334
RESERVED	RW	32	0x0000 0338	0x4A00 2338
CONTROL_USBOTGHS_CONTROL	RW	32	0x0000 033C	0x4A00 233C
CONTROL_DSS_CONTROL	RW	32	0x0000 0340	0x4A00 2340

Register Name	Type	Register Width (Bits)	Address Offset	SYSCTRL_GENERAL_CORE Physical Address
RESERVED	RO	32	0x0000 0344	0x4A00 2344
CONTROL_CORTEX_M3_MMUADDRTRANSLTR	RW	32	0x0000 0348	0x4A00 2348
CONTROL_CORTEX_M3_MMUADDR-LOGICTR	RW	32	0x0000 034C	0x4A00 234C
CONTROL_HWOBS_CONTROL	RW	32	0x0000 0350	0x4A00 2350
CONTROL_EMIF1_OFFSET	RW	32	0x0000 0360	0x4A00 2360
CONTROL_EMIF2_OFFSET	RW	32	0x0000 0364	0x4A00 2364
CONTROL_EMIF1_MASTER_CODE_0	R	32	0x0000 0368	0x4A00 2368
CONTROL_EMIF1_MASTER_CODE_1	R	32	0x0000 036C	0x4A00 236C
CONTROL_EMIF2_MASTER_CODE_0	R	32	0x0000 0370	0x4A00 2370
CONTROL_EMIF2_MASTER_CODE_1	R	32	0x0000 0374	0x4A00 2374
CONTROL_BANDGAP_CTRL	RW	32	0x0000 0378	0x4A00 2378
CONTROL_BANDGAP_COUNTER	RW	32	0x0000 037C	0x4A00 237C
CONTROL_BANDGAP_THRESHOLD	RW	32	0x0000 0380	0x4A00 2380
CONTROL_TSHUT_THRESHOLD	RW	32	0x0000 0384	0x4A00 2384
CONTROL_BANDGAP_STATUS	R	32	0x0000 0388	0x4A00 2388
CONTROL_FORCEWRNP	RW	32	0x0000 03C0	0x4A00 23C0
CONTROL_GEN_CORE_OCPREG_SPARE	RW	32	0x0000 03FC	0x4A00 23FC
CONTROL_DEBOBS_FINAL_MUX_SEL	RW	32	0x0000 0400	0x4A00 2400
RESERVED	RO	32	0x0000 0404	0x4A00 2404
CONTROL_DE-BOBS_MMR_MPU	RW	32	0x0000 0408	0x4A00 2408
RESERVED	RO	32	0x0000 0410	0x4A00 2410
RESERVED	RO	32	0x0000 0414	0x4A00 2414
RESERVED	RO	32	0x0000 0418	0x4A00 2418
RESERVED	RO	32	0x0000 041C	0x4A00 241C
RESERVED	RO	32	0x0000 0420	0x4A00 2420
RESERVED	RO	32	0x0000 0424	0x4A00 2424
CONTROL_CONF_SDMA_REQ_SEL0	RW	32	0x0000 042C	0x4A00 242C
CONTROL_CONF_SDMA_REQ_SEL1	RW	32	0x0000 0430	0x4A00 2430
CONTROL_CONF_SDMA_REQ_SEL2	RW	32	0x0000 0434	0x4A00 2434
CONTROL_CONF_SDMA_REQ_SEL3	RW	32	0x0000 0438	0x4A00 2438

Register Name	Type	Register Width (Bits)	Address Offset	SYSCTRL_GENERAL_CORE Physical Address
CONTROL_CONF_CLK_SEL0	RW	32	0x0000 0440	0x4A00 2440
CONTROL_CONF_CLK_SEL1	RW	32	0x0000 0444	0x4A00 2444
CONTROL_CONF_CLK_SEL2	RW	32	0x0000 0448	0x4A00 2448
CONTROL_CONF_DPLL_FREQ-LOCK_SEL	RW	32	0x0000 044C	0x4A00 244C
CONTROL_CONF_DPLL_TINITZ_SEL	RW	32	0x0000 0450	0x4A00 2450
CONTROL_CONF_DPLL_PHASELOCK_SEL	RW	32	0x0000 0454	0x4A00 2454
RESERVED	RW	32	0x0000 0458	0x4A00 2458
CONTROL_CONF_DPLL_TENABLE_SEL	RW	32	0x0000 045C	0x4A00 245C
CONTROL_CONF_DPLL_BYPASSACK_SEL	RW	32	0x0000 0464	0x4A00 2464
CONTROL_CONF_DPLL_IDLE_SEL	RW	32	0x0000 0468	0x4A00 2468
CONTROL_CORE_CONF_DEBUG_SEL_TST_0	RW	32	0x0000 0480	0x4A00 2480
CONTROL_CORE_CONF_DEBUG_SEL_TST_1	RW	32	0x0000 0484	0x4A00 2484
CONTROL_CORE_CONF_DEBUG_SEL_TST_2	RW	32	0x0000 0488	0x4A00 2488
CONTROL_CORE_CONF_DEBUG_SEL_TST_3	RW	32	0x0000 048C	0x4A00 248C
CONTROL_CORE_CONF_DEBUG_SEL_TST_4	RW	32	0x0000 0490	0x4A00 2490
CONTROL_CORE_CONF_DEBUG_SEL_TST_5	RW	32	0x0000 0494	0x4A00 2494
CONTROL_CORE_CONF_DEBUG_SEL_TST_6	RW	32	0x0000 0498	0x4A00 2498
CONTROL_CORE_CONF_DEBUG_SEL_TST_7	RW	32	0x0000 049C	0x4A00 249C
CONTROL_CORE_CONF_DEBUG_SEL_TST_8	RW	32	0x0000 04A0	0x4A00 24A0
CONTROL_CORE_CONF_DEBUG_SEL_TST_9	RW	32	0x0000 04A4	0x4A00 24A4
CONTROL_CORE_CONF_DEBUG_SEL_TST_10	RW	32	0x0000 04A8	0x4A00 24A8
CONTROL_CORE_CONF_DEBUG_SEL_TST_11	RW	32	0x0000 04AC	0x4A00 24AC

Register Name	Type	Register Width (Bits)	Address Offset	SYSCTRL_GENERAL_CORE Physical Address
CONTROL_CORE_CONF_DEBUG_SEL_TST_12	RW	32	0x0000 04B0	0x4A00 24B0
CONTROL_CORE_CONF_DEBUG_SEL_TST_13	RW	32	0x0000 04B4	0x4A00 24B4
CONTROL_CORE_CONF_DEBUG_SEL_TST_14	RW	32	0x0000 04B8	0x4A00 24B8
CONTROL_CORE_CONF_DEBUG_SEL_TST_15	RW	32	0x0000 04BC	0x4A00 24BC
CONTROL_CORE_CONF_DEBUG_SEL_TST_16	RW	32	0x0000 04C0	0x4A00 24C0
CONTROL_CORE_CONF_DEBUG_SEL_TST_17	RW	32	0x0000 04C4	0x4A00 24C4
CONTROL_CORE_CONF_DEBUG_SEL_TST_18	RW	32	0x0000 04C8	0x4A00 24C8
CONTROL_CORE_CONF_DEBUG_SEL_TST_19	RW	32	0x0000 04CC	0x4A00 24CC
CONTROL_CORE_CONF_DEBUG_SEL_TST_20	RW	32	0x0000 04D0	0x4A00 24D0
CONTROL_CORE_CONF_DEBUG_SEL_TST_21	RW	32	0x0000 04D4	0x4A00 24D4
CONTROL_CORE_CONF_DEBUG_SEL_TST_22	RW	32	0x0000 04D8	0x4A00 24D8
CONTROL_CORE_CONF_DEBUG_SEL_TST_23	RW	32	0x0000 04DC	0x4A00 24DC
CONTROL_CORE_CONF_DEBUG_SEL_TST_24	RW	32	0x0000 04E0	0x4A00 24E0
CONTROL_CORE_CONF_DEBUG_SEL_TST_25	RW	32	0x0000 04E4	0x4A00 24E4
CONTROL_CORE_CONF_DEBUG_SEL_TST_26	RW	32	0x0000 04E8	0x4A00 24E8
CONTROL_CORE_CONF_DEBUG_SEL_TST_27	RW	32	0x0000 04EC	0x4A00 24EC
CONTROL_CORE_CONF_DEBUG_SEL_TST_28	RW	32	0x0000 04F0	0x4A00 24F0
CONTROL_CORE_CONF_DEBUG_SEL_TST_29	RW	32	0x0000 04F4	0x4A00 24F4
CONTROL_CORE_CONF_DEBUG_SEL_TST_30	RW	32	0x0000 04F8	0x4A00 24F8

Register Name	Type	Register Width (Bits)	Address Offset	SYSCTRL_GENERAL_CORE Physical Address
CONTROL_CORE_CONF_DEBUG_SEL_TST_31	RW	32	0x0000 04FC	0x4A00 24FC

18.6.3. SYSCTRL_GENERAL_CORE Register Description

Note

This section contains only modified registers.

Table 18.5. CONTROL_STD_FUSE_OPP_VDD_IVA_2

Address Offset	0x0000 0234		
Physical Address	Please refer toTable 18.4	**Instance**	SYSCTRL_GENERAL_CORE
Description	Standard Fuse OPP VDD_IVA_2. Register shows part of the chip eFuse configuration on the L4 interface. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31 30 29 28	27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4	3 2 1 0
VDD_IVA_OPP_NITRO_SENP_GAIN	VDD_IVA_OPP_NITRO_SENN_GAIN	VDD_IVA_OPP_NITRO_SENP_REC	VDD_IVA_OPP_NITRO_SENN_REC	VDD_IVA_OPP_TURBO_SENP_GAIN	VDD_IVA_OPP_TURBO_SENN_GAIN

Bits	Field Name	Description	Type	Reset
~~31:8~~	~~RESERVED~~	-	~~R~~	~~0x000000~~
31:28	VDD_IVA_OPP_NITRO_SENP_GAIN	Voltage domain VDD_IVA OPP_NITRO [23:20] from Standard Fuse.	R	0x0
27:24	VDD_IVA_OPP_NITRO_SENN_GAIN	Voltage domain VDD_IVA OPP_NITRO [19:16] from Standard Fuse.	R	0x0
23:16	VDD_IVA_OPP_NITRO_SENP_REC	Voltage domain VDD_IVA OPP_NITRO [15:8] from Standard Fuse.	R	0x00
15:8	VDD_IVA_OPP_NITRO_SENN_REC	Voltage domain VDD_IVA OPP_NITRO [7:0] from Standard Fuse.	R	0x00
7:4	VDD_IVA_OPP_TURBO_SENP_GAIN	Voltage domain VDD_IVA OPP_TURBO [23:20] from Standard Fuse	R	0x0
3:0	VDD_IVA_OPP_TURBO_SENN_GAIN	Voltage domain VDD_IVA OPP_TURBO [19:16] from Standard Fuse	R	0x0

Table 18.6. Register Call Summary for Register CONTROL_STD_FUSE_OPP_VDD_IVA_2

Control Module Functional Description

- General Core Control Module Instance:[0]

Table 18.7. CONTROL_STD_FUSE_OPP_VDD_IVA_3

Address Offset	0x0000 0238		
Physical Address	Please refer toTable 18.4	**Instance**	SYSCTRL_GENERAL_CORE
Description	Standard Fuse OPP VDD_IVA_3. Register shows part of the chip eFuse configuration on the L4 interface. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31 30 29 28	27 26	25 24	23 22 21 20	19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
RESERVED	VDD_IVA_SR_SENN	VDD_IVA_SR_SENP	VDD_IVA_OPP_NTSB_SENP_GAIN	VDD_IVA_OPP_NTSB_SENN_GAIN	VDD_IVA_OPP_NTSB_SENP_REC	VDD_IVA_OPP_NTSB_SENN_REC

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:26	VDD_IVA_SR_SENN	VDD_IVA Smart Reflex from Standard FUSE	R	0x0
25:24	VDD_IVA_SR_SENP	VDD_IVA Smart Reflex from Standard FUSE	R	0x0
~~23:0~~	~~RESERVED~~	-	~~R~~	~~0x000000~~
23:20	VDD_IVA_OPP_NTSB_SENP_GAIN	Voltage domain VDD_IVA OPP_NTSB [23:20] from Standard Fuse	R	0x0
19:16	VDD_IVA_OPP_NTSB_SENN_GAIN	Voltage domain VDD_IVA OPP_NTSB [19:16] from Standard Fuse	R	0x0
15:8	VDD_IVA_OPP_NTSB_SENP_REC	Voltage domain VDD_IVA OPP_NTSB [15:8] from Standard Fuse	R	0x00
7:0	VDD_IVA_OPP_NTSB_SENN_REC	Voltage domain VDD_IVA OPP_NTSB [7:0] from Standard Fuse	R	0x00

Table 18.8. Register Call Summary for Register CONTROL_STD_FUSE_OPP_VDD_IVA_3

Control Module Functional Description

- General Core Control Module Instance:[0][1]

Table 18.9. CONTROL_STD_FUSE_OPP_VDD_MPU_3

Address Offset	0x0000 024C		
Physical Address	Please refer toTable 18.4	**Instance**	SYSCTRL_GENERAL_CORE
Description	Standard Fuse OPP VDD_MPU_3. Register shows part of the chip eFuse configuration on the L4 interface. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31 30 29 28	27 26	25 24	23 22 21 20	19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
RESERVED	VDD_MPU_SR_SENN	VDD_MPU_SR_SENP	VDD_MPU_OPP_NTSB_SENP_GAIN	VDD_MPU_OPP_NTSB_SENN_GAIN	VDD_MPU_OPP_NTSB_SENP_REC	VDD_MPU_OPP_NTSB_SENN_REC

Bits	Field Name	Description	Type	Reset
31:28	RESERVED		R	0x0
27:26	VDD_MPU_SR_SENN	VDD_MPU Smart Reflex from Standard FUSE	R	0x0
25:24	VDD_MPU_SR_SENP	VDD_MPU Smart Reflex from Standard FUSE	R	0x0
~~23:20~~	~~VDD_MPU_OPP_NITRO1.2G_SENP_GAIN~~	~~oltage domain VDD_MPU OPP_NITRO1.2G [23:20] from Standard Fuse~~	~~R~~	~~0x0~~
~~19:16~~	~~VDD_MPU_OPP_NITRO1.2G_SENN_GAIN~~	~~Voltage domain VDD_MPU OPP_NITRO1.2G [19:16] from Standard Fuse~~	~~R~~	~~0x0~~
~~15:8~~	~~VDD_MPU_OPP_NITRO1.2G_SENP_REC~~	~~Voltage domain VDD_MPU OPP_NITRO1.2G [15:8] from Standard Fuse~~	~~R~~	~~0x00~~
~~7:0~~	~~VDD_MPU_OPP_NITRO1.2G_SENN_REC~~	~~Voltage domain VDD_MPU OPP_NITRO1.2G [7:0] from Standard Fuse~~	~~R~~	~~0x00~~
23:20	VDD_MPU_OPP_NTSB_SENP_GAIN	Voltage domain VDD_MPU OPP_NTSB [23:20] from Standard Fuse	R	0x0
19:16	VDD_MPU_OPP_NTSB_SENN_GAIN	Voltage domain VDD_MPU OPP_NTSB [19:16] from Standard Fuse	R	0x0
15:8	VDD_MPU_OPP_NTSB_SENP_REC	Voltage domain VDD_MPU OPP_NTSB [15:8] from Standard Fuse	R	0x00
7:0	VDD_MPU_OPP_NTSB_SENN_REC	Voltage domain VDD_MPU OPP_NTSB [7:0] from Standard Fuse	R	0x00

Table 18.10. Register Call Summary for Register CONTROL_STD_FUSE_OPP_VDD_MPU_3

Control Module Functional Description

- General Core Control Module Instance:[0][1]

Table 18.11. CONTROL_STD_FUSE_OPP_VDD_CORE_1

Address Offset	0x0000 0258		
Physical Address	Please refer toTable 18.4	**Instance**	SYSCTRL_GENERAL_CORE
Description	Standard Fuse OPP VDD_CORE_1. Register shows part of the chip eFuse configuration on the L4 interface. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4 3 2 1 0
VDD_CORE_OPP119_SENP_REC	VDD_CORE_OPP119_SENN_REC	VDD_CORE_OPP100_SENP_GAIN	VDD_CORE_OPP100_SENN_GAIN	VDD_CORE_OPP100_SENP_REC

Bits	Field Name	Description	Type	Reset
~~31:16~~	~~RESERVED~~	-	~~R~~	~~0x0000~~
31:24	VDD_CORE_OPP119_SENP_REC	Voltage domain VDD_CORE OPP119 [15:8] from Standard Fuse (Overdrive Mode)	R	0x00
23:16	VDD_CORE_OPP119_SENN_REC	Voltage domain VDD_CORE OPP119 [7:0] from Standard Fuse (Overdrive Mode)	R	0x00
15:12	VDD_CORE_OPP100_SENP_GAIN	Voltage domain VDD_CORE OPP100 [23:20] from Standard Fuse	R	0x0
11:8	VDD_CORE_OPP100_SENN_GAIN	Voltage domain VDD_CORE OPP100 [19:16] from Standard Fuse	R	0x0
7:0	VDD_CORE_OPP100_SENP_REC	Voltage domain VDD_CORE OPP100 [15:8] from Standard Fuse	R	0x00

Table 18.12. Register Call Summary for Register CONTROL_STD_FUSE_OPP_VDD_CORE_1

Control Module Functional Description

- General Core Control Module Instance:[0]

Table 18.13. CONTROL_STD_FUSE_OPP_VDD_CORE_2

Address Offset	0x0000 025C		
Physical Address	Please refer toTable 18.4	**Instance**	SYSCTRL_GENERAL_CORE
Description	Standard Fuse OPP VDD_CORE_2. Register shows part of the chip eFuse configuration on the L4 interface. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
RESERVED		VDD_CORE_SR_SENN	VDD_CORE_SR_SENP	VDD_CORE_OPP119_SENP_GAIN	VDD_CORE_OPP119_SENN_GAIN

Bits	Field Name	Description	Type	Reset
31:12	RESERVED		R	0x0000
11:10	VDD_CORE_SR_SENN	VDD_CORE Smart Reflex from Standard FUSE	R	0x0
9:8	VDD_CORE_SR_SENP	VDD_CORE Smart Reflex from Standard FUSE	R	0x0
~~7:0~~	~~RESERVED~~	-	~~R~~	~~0x00~~
7:4	VDD_CORE_OPP119_SENP_GAIN	Voltage domain VDD_CORE OPP119 [23:20] from Standard Fuse (Overdrive Mode)	R	0x0
3:0	VDD_CORE_OPP119_SENN_GAIN	Voltage domain VDD_CORE OPP119 [19:16] from Standard Fuse (Overdrive Mode)	R	0x0

Table 18.14. Register Call Summary for Register CONTROL_STD_FUSE_OPP_VDD_CORE_2

Control Module Functional Description

- General Core Control Module Instance:[0]

Table 18.15. CONTROL_STD_FUSE_OPP_DPLL_1

Address Offset	0x0000 0268
Physical Address	Please refer toTable 18.4 **Instance** SYSCTRL_GENERAL_CORE
Description	Standard Fuse OPP DPLL. Register shows part of the chip eFuse configuration on the L4 interface. Reading at the address of one of these registers provides a direct view into a part of the eFuse chain. Access conditions. Read: unrestricted, Write: unrestricted
Type	R

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
RESERVED	IVA_RBB_TURBO, MPU_RBB_TURBO, MPU_DPLL_TRIM_FREQ	RESERVED	

Bits	Field Name	Description	Type	Reset
~~31:0~~	~~STD_FUSE_OPP_DPLL_1~~	-	~~R~~	~~0x0000 0000~~
31:22	RESERVED		R	0x000
21	IVA_RBB_TURBO	If trimmed, ABB (Adaptive Body Bias) set2 mode can be enabled at OPP TURBO on IVA	R	0x-[2]
		0x0: IVA ABB set2 voltage is NOT trimmed		
		0x1: IVA ABB set2 voltage is trimmed		
20	MPU_RBB_TURBO[1]	If trimmed, ABB set2 mode can be enabled at OPP TURBO on MPU.	R	0x-[2]
		0x0: MPU ABB set2 voltage is NOT trimmed		
		0x1: MPU ABB set2 voltage is trimmed		
19:18	MPU_DPLL_TRIM_FREQ[1]	Lock frequency at which the MPU DPLL is trimmed. The DPLL can be locked at any valid frequencies up to this value.	R	0x-[2]
		0x0: 2 GHz		
		0x1: 2.4 GHz		
		0x2: Reserved		
		0x3: 3 GHz		

Bits	Field Name	Description	Type	Reset
17:0	RESERVED		R	0x000

1. If [18] =0b1 and [20] =0b0, ABB set 1 can be enabled at OPP TURBO on MPU
2. The default value is the value fused during device production

Table 18.16. Register Call Summary for Register CONTROL_STD_FUSE_OPP_DPLL_1

Control Module Functional Description

- General Core Control Module Instance:[0][1][2][3]

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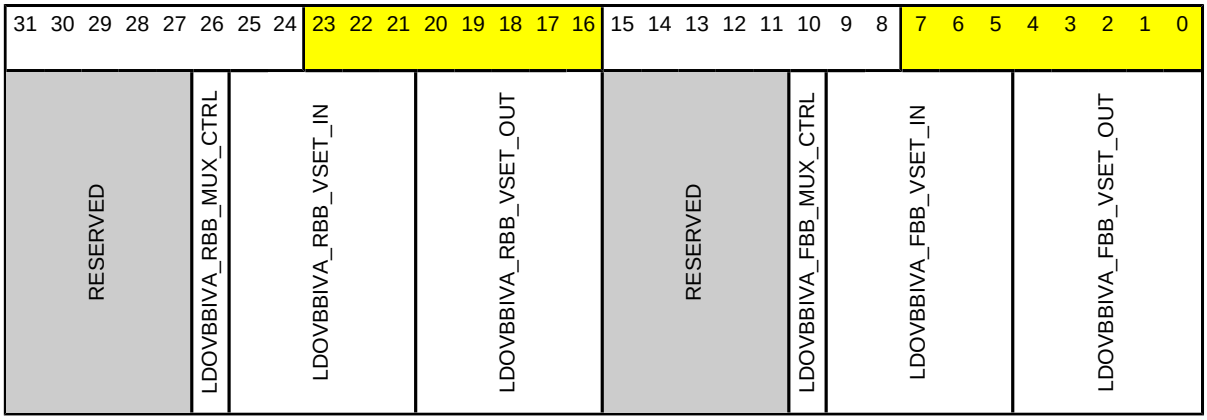
- SYSCTRL_GENERAL_CORE Register Description:[4][5]

Table 18.17. CONTROL_LDOVBB_IVA_VOLTAGE_CTRL

Address Offset	0x0000 0314		
Physical Address	Please refer toTable 18.4	**Instance**	SYSCTRL_GENERAL_CORE
Description	IVA Voltage Body Bias LDO Control register Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:~~11~~27	RESERVED		R	0x00
26	LDOVBBIVA_RBB_MUX_CTRL	Override control of EFUSE Adaptive Body Bias set2 voltage value 0x0: EFUSE value is used 0x1: override value is used	RW	0
25:21	LDOVBBIVA_RBB_VSET_IN	EFUSE Adaptive Body Bias set2 voltage value	R	0x00
20:16	LDOVBBIVA_RBB_VSET_OUT	Override value for Adaptive Body Bias set2 voltage	RW	0x00
15:11	RESERVED		R	0x00
10	LDOVBBIVA_FBB_MUX_CTRL	Override control of EFUSE Adaptive Body Bias set1 voltage value 0x0: EFUSE value is used 0x1: override value is used	RW	0
9:5	LDOVBBIVA_FBB_VSET_IN	EFUSE Adaptive Body Bias set1 voltage value	R	0x00
4:0	LDOVBBIVA_FBB_VSET_OUT	Override value for Adaptive Body Bias set1 voltage	RW	0x00

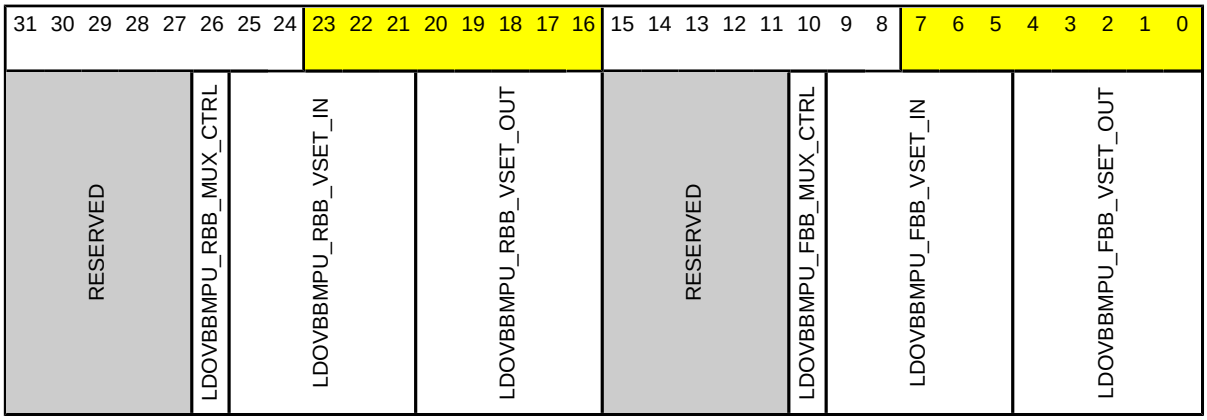
Table 18.18. Register Call Summary for Register CONTROL_LDOVBB_IVA_VOLTAGE_CTRL

Control Module Functional Description

- General Core Control Module Instance:[0][1][2][3]

Table 18.19. CONTROL_LDOVBB_MPU_VOLTAGE_CTRL

Address Offset	0x0000 0318		
Physical Address	Please refer toTable 18.4	**Instance**	SYSCTRL_GENERAL_CORE
Description	MPU Voltage Body Bias LDO Control register Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:~~11~~27	RESERVED		R	0x00
26	LDOVBBMPU_RBB_MUX_CTRL	Override control of EFUSE Adaptive Body Bias set2 voltage value 0x0: EFUSE value is used 0x1: override value is used	RW	0
25:21	LDOVBBMPU_RBB_VSET_IN	EFUSE Adaptive Body Bias set2 voltage value	R	0x00
20:16	LDOVBBMPU_RBB_VSET_OUT	Override value for Adaptive Body Bias set2 voltage	RW	0x00
15:11	RESERVED		R	0x00
10	LDOVBBMPU_FBB_MUX_CTRL	Override control of EFUSE Adaptive Body Bias set1 voltage value 0x0: EFUSE value is used 0x1: override value is used	RW	0
9:5	LDOVBBMPU_FBB_VSET_IN	EFUSE Adaptive Body Bias set1 voltage value	R	0x00
4:0	LDOVBBMPU_FBB_VSET_OUT	Override value for Adaptive Body Bias set1 voltage	RW	0x00

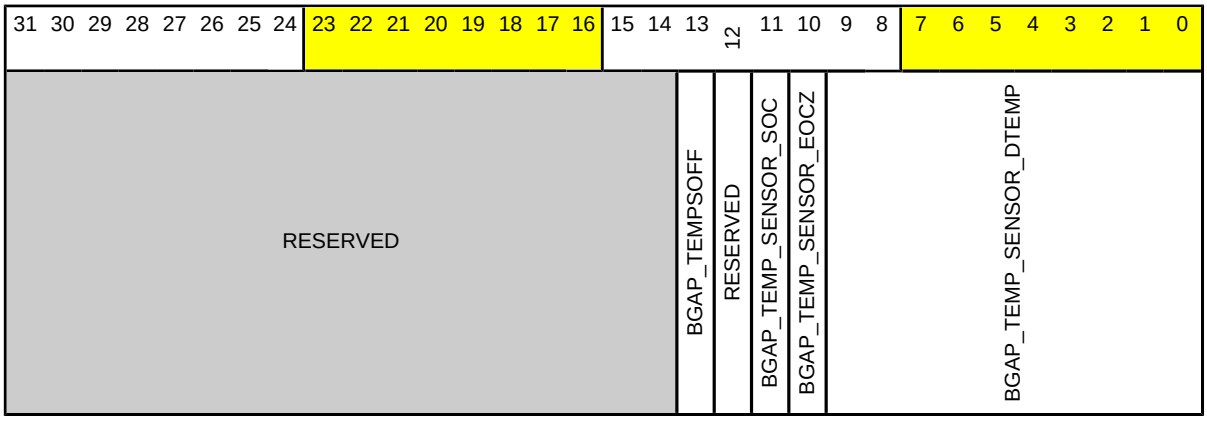
Table 18.20. Register Call Summary for Register CONTROL_LDOVBB_MPU_VOLTAGE_CTRL

Control Module Functional Description

- General Core Control Module Instance:[0][1][2][3]

Table 18.21. CONTROL_TEMP_SENSOR

Address Offset	0x0000 032C		
Physical Address	Please refer toTable 18.4	**Instance**	SYSCTRL_GENERAL_CORE
Description	Control VBGAPTS temperature sensorand thermal comparator shutdown register Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:~~13~~14	RESERVED		R	0x00000
~~12~~13	BGAP_TEMPSOFF	Temperature sensor and thermal shutdown mode. 0x0: Temperature sensor and thermal shutdown is active 0x1: Temperature sensor and thermal shutdown set in OFF mode	RW	0
~~10~~12	~~BGAP_TEMP_SENSOR_CONTCONV~~ RESERVED	~~VDD level digital inputs. When high the ADC is in continuous conversion mode.~~Reserved. ~~0x0: ADC Single Conversion Mode~~ ~~0x1: ADC Continuous Conversion Mode~~	RW	0
~~11~~	~~BGAP_TSHUT~~	~~Thermal shutdown comparator output. It is low during normal operation and goes high during a thermal shutdown event.~~	~~R~~	~~0~~
9~~11~~	BGAP_TEMP_SENSOR_SOC	ADC Start of Conversion. A transition to high starts a new ADC conversion cycle	RW	0
~~8~~10	BGAP_TEMP_SENSOR_EOCZ	ADC End of Conversion. Active low, when CTRL_TEMP(5:0) is valid.	R	0
~~7~~9:0	BGAP_TEMP_SENSOR_DTEMP	Temperature data from the ADC. Valid if EOCZ is low.	R	0x000

Table 18.22. Register Call Summary for Register CONTROL_TEMP_SENSOR

Control Module Functional Description

- Control Module Clock Configuration:[0]
- Band Gap Voltage and Temperature Sensor:[1][2][3]

Table 18.23. CONTROL_HWOBS_CONTROL

Address Offset	0x0000 0350		
Physical Address	See Table 18.4	**Instance**	SYSCTRL_GENERAL_CORE
Description	HW observability control. This register enables or disables HW observability outputs (to save power primarily) Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													RESERVED HWOBS_CLKDIV_SEL_2					RESERVED HWOBS_CLKDIV_SEL_1					RESERVED	HWOBS_CLKDIV_SEL					HWOBS_ALL_ZERO_MODE	HWOBS_ALL_ONE_MODE	HWOBS_MACRO_ENABLE

Bits	Field Name	Description	Type	Reset
31:19	RESERVED		R	0x000000
18:14	HWOBS_CLKDIV_SEL_2	Clock divider selection on po_hwobs(2). 0x1: output is not divided 0x2: output is divided by 2 0x4: output is divided by 4 0x8: output is divided by 8 0x10: output is divided by 16[1]	RW	0x00
13:9	HWOBS_CLKDIV_SEL_1	Clock divider selection on po_hwobs(1). 0x1: output is not divided 0x2: output is divided by 2 0x4: output is divided by 4 0x8: output is divided by 8 0x10: output is divided by 16[1]	RW	0x00
8	RESERVED		R	0x0
7:3	HWOBS_CLKDIV_SEL	Clock divider selection on po_hwobs(0). 0x1: output is not divided 0x2: output is divided by 2 0x4: output is divided by 4 0x8: output is divided by 8 0x10: output is divided by 16[1]	RW	0x00
2	HWOBS_ALL_ZERO_MODE	Used to gate observable signals. When set all outputs are set to zero (can be used to check the path from HW observability to external pads). 0x0: hw observability ports are not gated 0x1: hw observability ports are all set to 0	RW	0
1	HWOBS_ALL_ONE_MODE	Used to gate observable signals. When set all outputs are set to one (can be used to check the path from HW observability to external pads). 0x0: hw observability ports are not gated 0x1: hw observability ports are all set to 1	RW	0
0	HWOBS_MACRO_ENABLE	Used to gate observable signals coming from macros using the 32-bit HWOBS bus definition. When deasserted all outputs of the HWOBS busdef are set to zero. 0x0: hw observability ports from macros are gated and set to zero	RW	0

Bits	Field Name	Description	Type	Reset
		0x1: hw observability ports from macros are not gated		

1. The values different than 1, 2, 4, 8, and 16 are reserved.

Table 18.24. Register Call Summary for Register CONTROL_HWOBS_CONTROL

Control Module Functional Description

- Observability Gating Capabilities:[0]

Control Module Programming Guide

- Control Module Programming Guide:[1]

Table 18.25. CONTROL_EMIF1_OFFSET

Address Offset	0x0000 0360		
Physical Address	0x4A00 2360	**Instance**	SYSCTRL_GENERAL_CORE
Description	emif1 offset Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
EMIF1_DLL_OFFSET_3	EMIF1_DLL_OFFSET_2	EMIF1_DLL_OFFSET_1	EMIF1_DLL_OFFSET_0

Bits	Field Name	Description	Type	Reset
31:24	EMIF1_DLL_OFFSET_3	8-bit signed offset value (-128 .. +127) for EMIF1 DLL Slave3 delay correction	RW	0x00
23:16	EMIF1_DLL_OFFSET_2	8-bit signed offset value (-128 .. +127) for EMIF1 DLL Slave2 delay correction	RW	0x00
15:8	EMIF1_DLL_OFFSET_1	8-bit signed offset value (-128 .. +127) for EMIF1 DLL Slave1 delay correction	RW	0x00
7:0	EMIF1_DLL_OFFSET_0	8-bit signed offset value (-128 .. +127) for EMIF1 DLL Slave0 delay correction	RW	0x00

Table 18.26. Register Call Summary for Register CONTROL_EMIF1_OFFSET

Control Module Functional Description

- General Core Control Module Instance:[0]
- Functional Register Description:[1]

Table 18.27. CONTROL_EMIF2_OFFSET

Address Offset	0x0000 0364		
Physical Address	0x4A00 2364	**Instance**	SYSCTRL_GENERAL_CORE
Description	emif2 offset Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
EMIF2_DLL_OFFSET_3	EMIF2_DLL_OFFSET_2	EMIF2_DLL_OFFSET_1	EMIF2_DLL_OFFSET_0

Bits	Field Name	Description	Type	Reset
31:24	EMIF2_DLL_OFFSET_3	8-bit signed offset value (-128 .. +127) for EMIF2 DLL Slave3 delay correction	RW	0x00
23:16	EMIF2_DLL_OFFSET_2	8-bit signed offset value (-128 .. +127) for EMIF2 DLL Slave2 delay correction	RW	0x00
15:8	EMIF2_DLL_OFFSET_1	8-bit signed offset value (-128 .. +127) for EMIF2 DLL Slave1 delay correction	RW	0x00
7:0	EMIF2_DLL_OFFSET_0	8-bit signed offset value (-128 .. +127) for EMIF2 DLL Slave0 delay correction	RW	0x00

Table 18.28. Register Call Summary for Register CONTROL_EMIF2_OFFSET

Control Module Functional Description

- General Core Control Module Instance:[0]
- Functional Register Description:[1]

Table 18.29. CONTROL_EMIF1_MASTER_CODE_0

Address Offset	0x0000 0368		
Physical Address	0x4A00 2368	**Instance**	SYSCTRL_GENERAL_CORE
Description	emif1 master code Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
RESERVED	EMIF1_MASTER_CODE_1	RESERVED	EMIF1_MASTER_CODE_0

Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00

Bits	Field Name	Description	Type	Reset
25:16	EMIF1_MASTER_CODE_1	EMIF1 DLL Master1 code	R	0x000
15:10	RESERVED		R	0x00
9:0	EMIF1_MASTER_CODE_0	EMIF1 DLL Master0 code	R	0x000

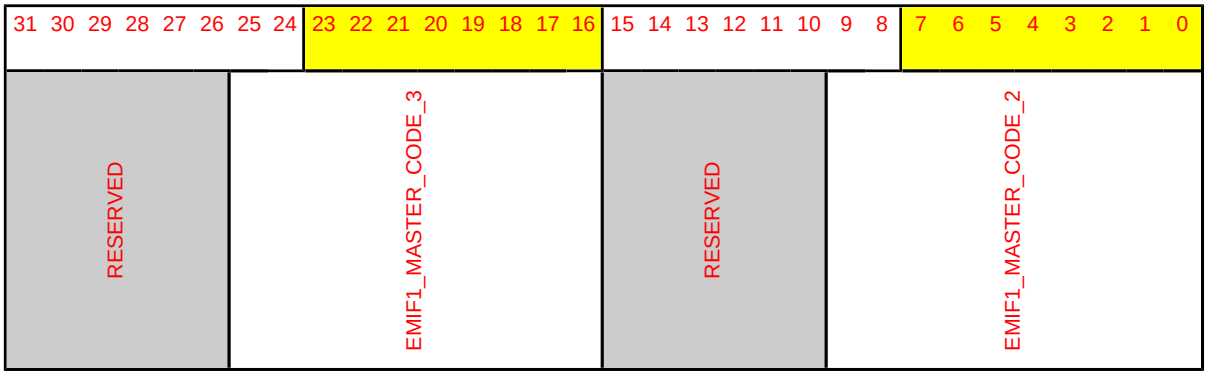
Table 18.30. Register Call Summary for Register CONTROL_EMIF1_MASTER_CODE_0

Control Module Functional Description

- General Core Control Module Instance:[0]
- Functional Register Description:[1]

Table 18.31. CONTROL_EMIF1_MASTER_CODE_1

Address Offset	0x0000 036C		
Physical Address	0x4A00 236C	**Instance**	SYSCTRL_GENERAL_CORE
Description	Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		



Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25:16	EMIF1_MASTER_CODE_3	EMIF1 DLL Master3 code	R	0x000
15:10	RESERVED		R	0x00
9:0	EMIF1_MASTER_CODE_2	EMIF1 DLL Master2 code	R	0x000

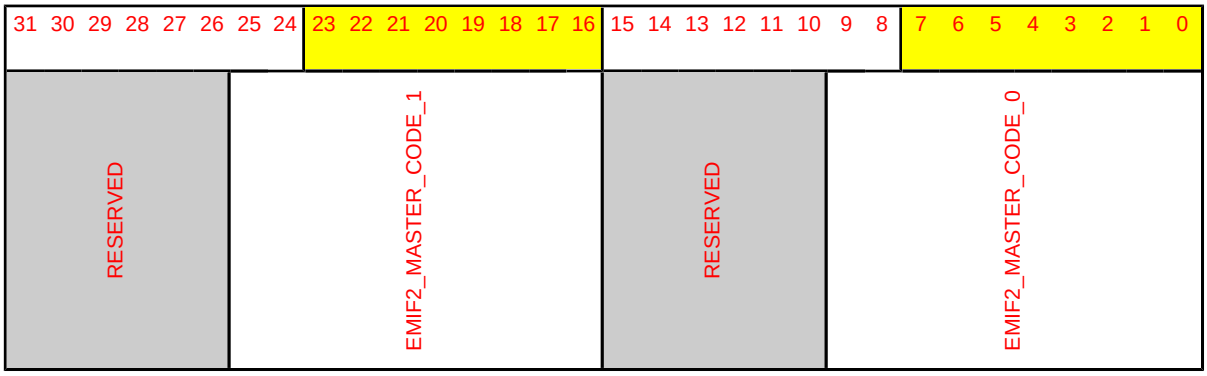
Table 18.32. Register Call Summary for Register CONTROL_EMIF1_MASTER_CODE_1

Control Module Functional Description

- General Core Control Module Instance:[0]
- Functional Register Description:[1]

Table 18.33. CONTROL_EMIF2_MASTER_CODE_0

Address Offset	0x0000 0370		
Physical Address	0x4A00 2370	**Instance**	SYSCTRL_GENERAL_CORE
Description	emif2 master code Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		



Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25:16	EMIF2_MASTER_CODE_1	EMIF2 DLL Master1 code	R	0x000
15:10	RESERVED		R	0x00
9:0	EMIF2_MASTER_CODE_0	EMIF2 DLL Master0 code	R	0x000

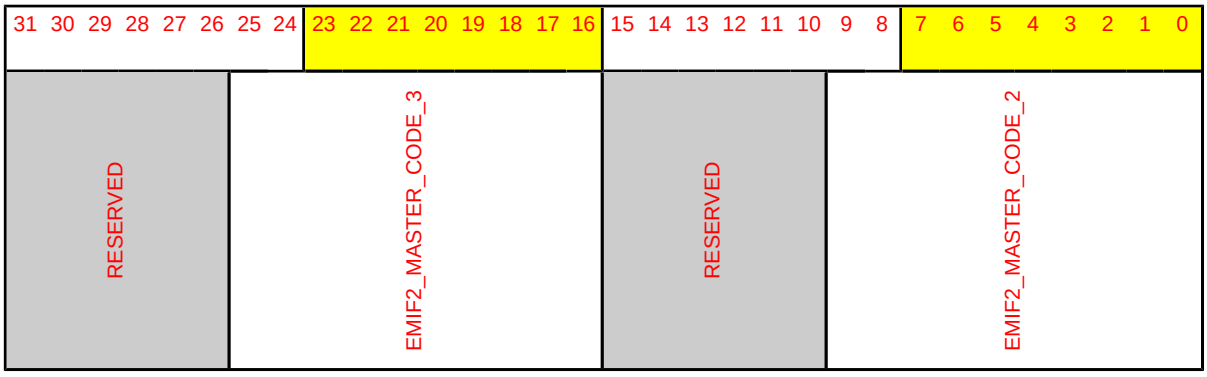
Table 18.34. Register Call Summary for Register CONTROL_EMIF2_MASTER_CODE_0

Control Module Functional Description

- General Core Control Module Instance:[0]
- Functional Register Description:[1]

Table 18.35. CONTROL_EMIF2_MASTER_CODE_1

Address Offset	0x0000 0374		
Physical Address	0x4A00 2374	**Instance**	SYSCTRL_GENERAL_CORE
Description	Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		



Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25:16	EMIF2_MASTER_CODE_3	EMIF2 DLL Master3 code	R	0x000
15:10	RESERVED		R	0x00
9:0	EMIF2_MASTER_CODE_2	EMIF2 DLL Master2 code	R	0x000

Table 18.36. Register Call Summary for Register CONTROL_EMIF2_MASTER_CODE_1

Control Module Functional Description

- General Core Control Module Instance:[0]
- Functional Register Description:[1]

Table 18.37. CONTROL_BANDGAP_CTRL

Address Offset	0x0000 0378		
Physical Address	0x4A00 2378	**Instance**	SYSCTRL_GENERAL_CORE
Description	bandgap control Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SINGLE_MODE	RESERVED																													MASK_HOT	MASK_COLD

Bits	Field Name	Description	Type	Reset
31	SINGLE_MODE	Toggles between single mode or continuous mode (repeated single mode) 0x0: Single mode selected 0x1: Continuous mode selected	RW	0
30:2	RESERVED		R	0x0000 0000
1	MASK_HOT	Mask for hot events 0x0: hot event is masked 0x1:	RW	0
0	MASK_COLD	Mask for cold events 0x0: cold event is masked 0x1:	RW	0

Table 18.38. Register Call Summary for Register CONTROL_BANDGAP_CTRL

Control Module Functional Description

- General Core Control Module Instance:[0]
- Band Gap Voltage and Temperature Sensor:[1][2]
- Temperature Sensor Control Register:[3]

Table 18.39. CONTROL_BANDGAP_COUNTER

Address Offset	0x0000 037C		
Physical Address	0x4A00 237C	**Instance**	SYSCTRL_GENERAL_CORE
Description	bandgap counter Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								COUNTER																							

Bits	Field Name	Description	Type	Reset
31:24	RESERVED		R	0x00
23:0	COUNTER	Counter for continous mode	RW	0x000000

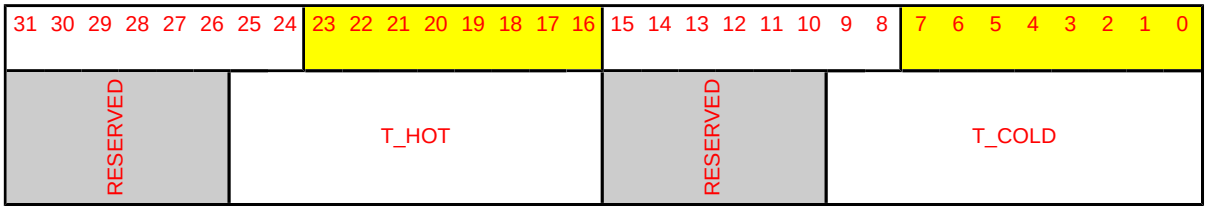
Table 18.40. Register Call Summary for Register CONTROL_BANDGAP_COUNTER

Control Module Functional Description

- General Core Control Module Instance:[0]
- Band Gap Voltage and Temperature Sensor:[1]
- Temperature Sensor Control Register:[2]

Table 18.41. CONTROL_BANDGAP_THRESHOLD

Address Offset	0x0000 0380		
Physical Address	0x4A00 2380	**Instance**	SYSCTRL_GENERAL_CORE
Description	bandgap threshold Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25:16	T_HOT	Threshold for hot temperature	RW	0x000
15:10	RESERVED		R	0x00
9:0	T_COLD	Threshold for cold temperature	RW	0x000

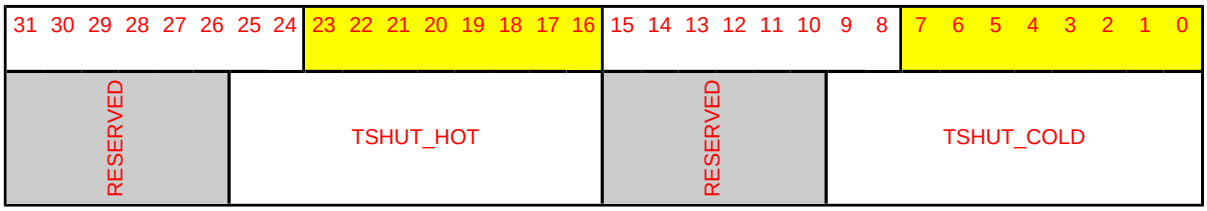
Table 18.42. Register Call Summary for Register CONTROL_BANDGAP_THRESHOLD

Control Module Functional Description

- General Core Control Module Instance:[0]
- Band Gap Voltage and Temperature Sensor:[1]
- Temperature Sensor Control Register:[2]

Table 18.43. CONTROL_TSHUT_THRESHOLD

Address Offset	0x0000 0384		
Physical Address	0x4A00 2384	**Instance**	SYSCTRL_GENERAL_CORE
Description	bandgap tshut threshold Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:26	RESERVED		R	0x00
25:16	TSHUT_HOT	Tshut Threshold for hot temperature. Code value must not exceed the device junction (hottest spot) maximal allowed temperature minus the device temperature sensor offset estimated at current conditions.	RW	0x000
15:10	RESERVED		R	0x00
9:0	TSHUT_COLD	Tshut Threshold for cold temperature	RW	0x000

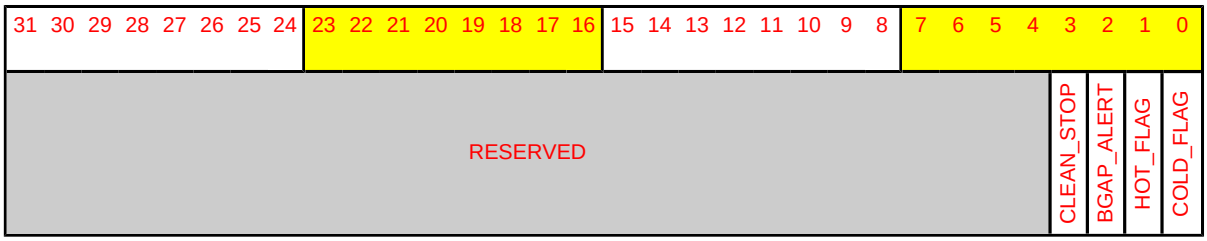
Table 18.44. Register Call Summary for Register CONTROL_TSHUT_THRESHOLD

Control Module Functional Description

- General Core Control Module Instance:[0]
- Band Gap Voltage and Temperature Sensor:[1]
- Temperature Sensor Control Register:[2]

Table 18.45. CONTROL_BANDGAP_STATUS

Address Offset	0x0000 0388		
Physical Address	0x4A00 2388	**Instance**	SYSCTRL_GENERAL_CORE
Description	bandgap status Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		



Bits	Field Name	Description	Type	Reset
31:4	RESERVED		R	0x0000000
3	CLEAN_STOP	Show when clean stop	R	1
2	BGAP_ALERT	Show when hot or cold event	R	0
1	HOT_FLAG	Show when hot event	R	0
0	COLD_FLAG	Show when cold event	R	0

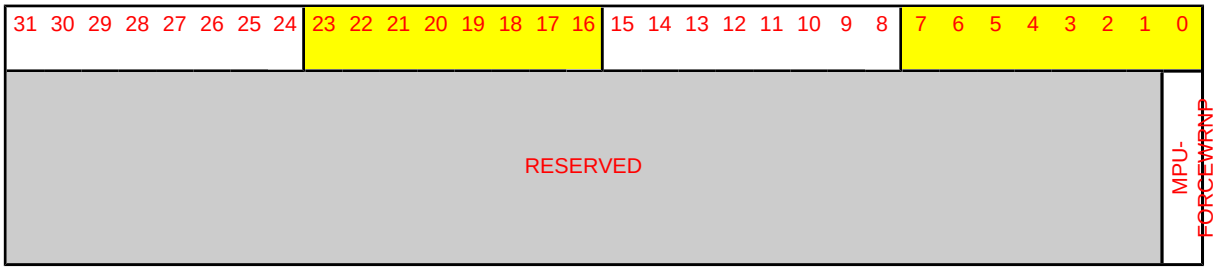
Table 18.46. Register Call Summary for Register CONTROL_BANDGAP_STATUS

Control Module Functional Description

- General Core Control Module Instance:[0]
- Band Gap Voltage and Temperature Sensor:[1][2]
- Temperature Sensor Control Register:[3]

Table 18.47. CONTROL_FORCEWRNP

Address Offset	0x0000 03C0		
Physical Address	0x4A00 23C0	**Instance**	SYSCTRL_GENERAL_CORE
Description	Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:1	RESERVED		R	0x0000 0000
0	MPUFORCEWRNP	0x0:Non-posted write attribute is defined by Cortex-A9 CPU 0x1: Forces only non-posted write commands from MPUSS to the L3 interconnect	RW	0

Table 18.48. Register Call Summary for Register CONTROL_FORCEWRNP

Control Module Functional Description

- General Core Control Module Instance:[0]
- Functional Register Description:[1]

18.6.4. SYSCTRL_GENERAL_WKUP Register Summary

Refer to OMAP4460 Silicon Revision 1.x TRM.

18.6.5. SYSCTRL_GENERAL_WKUP Register Description

Refer to OMAP4460 Silicon Revision 1.x TRM.

18.6.6. SYSCTRL_PADCONF_CORE Register Summary

Table 18.49. SYSCTRL_PADCONF_CORE Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	SYSCTRL_PADCONF_CORE Physical Address
CONTROL_PADCONF_CORE_REVISION	R	32	0x00000000	0x4A10 0000
CONTROL_PADCONF_CORE_HWINFO	R	32	0x00000004	0x4A10 0004
CONTROL_PADCONF_CORE_SYSCONFIG	RW	32	0x00000010	0x4A10 0010
CONTROL_CORE_PAD0_GPMC_AD0_PAD1_GPMC_AD1	RW	32	0x00000040	0x4A10 0040
CONTROL_CORE_PAD0_GPMC_AD2_PAD1_GPMC_AD3	RW	32	0x00000044	0x4A10 0044
CONTROL_CORE_PAD0_GPMC_AD4_PAD1_GPMC_AD5	RW	32	0x00000048	0x4A10 0048
CONTROL_CORE_PAD0_GPMC_AD6_PAD1_GPMC_AD7	RW	32	0x0000004C	0x4A10 004C
CONTROL_CORE_PAD0_GPMC_AD8_PAD1_GPMC_AD9	RW	32	0x00000050	0x4A10 0050

Register Name	Type	Register Width (Bits)	Address Offset	SYSCTRL_PADCONF_CORE Physical Address
CONTROL_CORE_PAD0_GPMC_AD10_PAD1_GPMC_AD11	RW	32	0x00000054	0x4A10 0054
CONTROL_CORE_PAD0_GPMC_AD12_PAD1_GPMC_AD13	RW	32	0x00000058	0x4A10 0058
CONTROL_CORE_PAD0_GPMC_AD14_PAD1_GPMC_AD15	RW	32	0x0000005C	0x4A10 005C
CONTROL_CORE_PAD0_GPMC_A16_PAD1_GPMC_A17	RW	32	0x00000060	0x4A10 0060
CONTROL_CORE_PAD0_GPMC_A18_PAD1_GPMC_A19	RW	32	0x00000064	0x4A10 0064
CONTROL_CORE_PAD0_GPMC_A20_PAD1_GPMC_A21	RW	32	0x00000068	0x4A10 0068
CONTROL_CORE_PAD0_GPMC_A22_PAD1_GPMC_A23	RW	32	0x0000006C	0x4A10 006C
CONTROL_CORE_PAD0_GPMC_A24_PAD1_GPMC_A25	RW	32	0x00000070	0x4A10 0070
CONTROL_CORE_PAD0_GPMC_NCS0_PAD1_GPMC_NCS1	RW	32	0x00000074	0x4A10 0074
CONTROL_CORE_PAD0_GPMC_NCS2_PAD1_GPMC_NCS3	RW	32	0x00000078	0x4A10 0078
CONTROL_CORE_PAD0_GPMC_NWP_PAD1_GPMC_CLK	RW	32	0x0000007C	0x4A10 007C
CONTROL_CORE_PAD0_GPMC_NADV_ALE_PAD1_GPMC_NOE	RW	32	0x00000080	0x4A10 0080
CONTROL_CORE_PAD0_GPMC_NWE_PAD1_GPMC_NBE0_CLE	RW	32	0x00000084	0x4A10 0084
CONTROL_CORE_PAD0_GPMC_NBE1_PAD1_GPMC_WAIT0	RW	32	0x00000088	0x4A10 0088
CONTROL_CORE_PAD0_GPMC_WAIT1_PAD1_GPMC_WAIT2	RW	32	0x0000008C	0x4A10 008C
CONTROL_CORE_PAD0_GPMC_NCS4_PAD1_GPMC_NCS5	RW	32	0x00000090	0x4A10 0090
CONTROL_CORE_PAD0_GPMC_NCS6_PAD1_GPMC_NCS7	RW	32	0x00000094	0x4A10 0094
CONTROL_CORE_PAD0_GPIO63_PAD1_GPIO64	RW	32	0x00000098	0x4A10 0098
CONTROL_CORE_PAD0_GPIO65_PAD1_GPIO66	RW	32	0x0000009C	0x4A10 009C

Register Name	Type	Register Width (Bits)	Address Offset	SYSCTRL_PADCONF_CORE Physical Address
CONTROL_CORE_PAD0_CSI21_DX0_PAD1_CSI21_DY0	RW	32	0x000000A0	0x4A10 00A0
CONTROL_CORE_PAD0_CSI21_DX1_PAD1_CSI21_DY1	RW	32	0x000000A4	0x4A10 00A4
CONTROL_CORE_PAD0_CSI21_DX2_PAD1_CSI21_DY2	RW	32	0x000000A8	0x4A10 00A8
CONTROL_CORE_PAD0_CSI21_DX3_PAD1_CSI21_DY3	RW	32	0x000000AC	0x4A10 00AC
CONTROL_CORE_PAD0_CSI21_DX4_PAD1_CSI21_DY4	RW	32	0x000000B0	0x4A10 00B0
CONTROL_CORE_PAD0_CSI22_DX0_PAD1_CSI22_DY0	RW	32	0x000000B4	0x4A10 00B4
CONTROL_CORE_PAD0_CSI22_DX1_PAD1_CSI22_DY1	RW	32	0x000000B8	0x4A10 00B8
CONTROL_CORE_PAD0_CAM_SHUTTER_PAD1_CAM_STROBE	RW	32	0x000000BC	0x4A10 00BC
CONTROL_CORE_PAD0_CAM_GLOBALRESET_PAD1_USBB1_ULPITLL_CLK	RW	32	0x000000C0	0x4A10 00C0
CONTROL_CORE_PAD0_USBB1_ULPITLL_STP_PAD1_USBB1_ULPITLL_DIR	RW	32	0x000000C4	0x4A10 00C4
CONTROL_CORE_PAD0_USBB1_ULPITLL_NXT_PAD1_USBB1_ULPITLL_DAT0	RW	32	0x000000C8	0x4A10 00C8
CONTROL_CORE_PAD0_USBB1_ULPITLL_DAT1_PAD1_USBB1_ULPITLL_DAT2	RW	32	0x000000CC	0x4A10 00CC
CONTROL_CORE_PAD0_USBB1_ULPITLL_DAT3_PAD1_USBB1_ULPITLL_DAT4	RW	32	0x000000D0	0x4A10 00D0
CONTROL_CORE_PAD0_USBB1_ULPITLL_DAT5_PAD1_USBB1_ULPITLL_DAT6	RW	32	0x000000D4	0x4A10 00D4
CONTROL_CORE_PAD0_USBB1_ULPITLL_DAT7_PAD1_USBB1_HSIC_DATA	RW	32	0x000000D8	0x4A10 00D8
CONTROL_CORE_PAD0_USBB1_HSIC_STROBE_PAD1_USBC1_ICUSB_DP	RW	32	0x000000DC	0x4A10 00DC
CONTROL_CORE_PAD0_USBC1_ICUSB_DM_PAD1_SDMMC1_CLK	RW	32	0x000000E0	0x4A10 00E0

Register Name	Type	Register Width (Bits)	Address Offset	SYSCTRL_PADCONF_CORE Physical Address
CONTROL_CORE_PAD0_SDMMC1_CMD_PAD1_SDMMC1_DAT0	RW	32	0x000000E4	0x4A10 00E4
CONTROL_CORE_PAD0_SDMMC1_DAT1_PAD1_SDMMC1_DAT2	RW	32	0x000000E8	0x4A10 00E8
CONTROL_CORE_PAD0_SDMMC1_DAT3_PAD1_SDMMC1_DAT4	RW	32	0x000000EC	0x4A10 00EC
CONTROL_CORE_PAD0_SDMMC1_DAT5_PAD1_SDMMC1_DAT6	RW	32	0x000000F0	0x4A10 00F0
CONTROL_CORE_PAD0_SDMMC1_DAT7_PAD1_ABE_MCBSP2_CLKX	RW	32	0x000000F4	0x4A10 00F4
CONTROL_CORE_PAD0_ABE_MCBSP2_DR_PAD1_ABE_MCBSP2_DX	RW	32	0x000000F8	0x4A10 00F8
CONTROL_CORE_PAD0_ABE_MCBSP2_FSX_PAD1_ABE_MCBSP1_CLKX	RW	32	0x000000FC	0x4A10 00FC
CONTROL_CORE_PAD0_ABE_MCBSP1_DR_PAD1_ABE_MCBSP1_DX	RW	32	0x00000100	0x4A10 0100
CONTROL_CORE_PAD0_ABE_MCBSP1_FSX_PAD1_ABE_PDM_UL_DATA	RW	32	0x00000104	0x4A10 0104
CONTROL_CORE_PAD0_ABE_PDM_DL_DATA_PAD1_ABE_PDM_FRAME	RW	32	0x00000108	0x4A10 0108
CONTROL_CORE_PAD0_ABE_PDM_LB_CLK_PAD1_ABE_CLKS	RW	32	0x0000010C	0x4A10 010C
CONTROL_CORE_PAD0_ABE_DMIC_CLK1_PAD1_ABE_DMIC_DIN1	RW	32	0x00000110	0x4A10 0110
CONTROL_CORE_PAD0_ABE_DMIC_DIN2_PAD1_ABE_DMIC_DIN3	RW	32	0x00000114	0x4A10 0114
CONTROL_CORE_PAD0_UART2_CTS_PAD1_UART2_RTS	RW	32	0x00000118	0x4A10 0118

Register Name	Type	Register Width (Bits)	Address Offset	SYSCTRL_PADCONF_CORE Physical Address
CONTROL_CORE_PAD0_UART2_RX_PAD1_UART2_TX	RW	32	0x0000011C	0x4A10 011C
CONTROL_CORE_PAD0_HDQ_SIO_PAD1_I2C1_SCL	RW	32	0x00000120	0x4A10 0120
CONTROL_CORE_PAD0_I2C1_SDA_PAD1_I2C2_SCL	RW	32	0x00000124	0x4A10 0124
CONTROL_CORE_PAD0_I2C2_SDA_PAD1_I2C3_SCL	RW	32	0x00000128	0x4A10 0128
CONTROL_CORE_PAD0_I2C3_SDA_PAD1_I2C4_SCL	RW	32	0x0000012C	0x4A10 012C
CONTROL_CORE_PAD0_I2C4_SDA_PAD1_MCSPI1_CLK	RW	32	0x00000130	0x4A10 0130
CONTROL_CORE_PAD0_MCSPI1_SOMI_PAD1_MCSPI1_SIMO	RW	32	0x00000134	0x4A10 0134
CONTROL_CORE_PAD0_MCSPI1_CS0_PAD1_MCSPI1_CS1	RW	32	0x00000138	0x4A10 0138
CONTROL_CORE_PAD0_MCSPI1_CS2_PAD1_MCSPI1_CS3	RW	32	0x0000013C	0x4A10 013C
CONTROL_CORE_PAD0_UART3_CTS_RCTX_PAD1_UART3_RTS_SD	RW	32	0x00000140	0x4A10 0140
CONTROL_CORE_PAD0_UART3_RX_IRRX_PAD1_UART3_TX_IRTX	RW	32	0x00000144	0x4A10 0144
CONTROL_CORE_PAD0_SDMMC5_CLK_PAD1_SDMMC5_CMD	RW	32	0x00000148	0x4A10 0148
CONTROL_CORE_PAD0_SDMMC5_DAT0_PAD1_SDMMC5_DAT1	RW	32	0x0000014C	0x4A10 014C
CONTROL_CORE_PAD0_SDMMC5_DAT2_PAD1_SDMMC5_DAT3	RW	32	0x00000150	0x4A10 0150
CONTROL_CORE_PAD0_MCSPI4_CLK_PAD1_MCSPI4_SIMO	RW	32	0x00000154	0x4A10 0154
CONTROL_CORE_PAD0_MCSPI4_SOMI_PAD1_MCSPI4_CS0	RW	32	0x00000158	0x4A10 0158
CONTROL_CORE_PAD0_UART4_RX_PAD1_UART4_TX	RW	32	0x0000015C	0x4A10 015C
CONTROL_CORE_PAD0_USBB2_ULPITLL_CLK_PAD1_USBB2_ULPITLL_STP	RW	32	0x00000160	0x4A10 0160

Register Name	Type	Register Width (Bits)	Address Offset	SYSCTRL_PADCONF_CORE Physical Address
CONTROL_CORE_PAD0_USBB2_ULPITLL_DIR_PAD1_USBB2_ULPITLL_NXT	RW	32	0x00000164	0x4A10 0164
CONTROL_CORE_PAD0_USBB2_ULPITLL_DAT0_PAD1_USBB2_ULPITLL_DAT1	RW	32	0x00000168	0x4A10 0168
CONTROL_CORE_PAD0_USBB2_ULPITLL_DAT2_PAD1_USBB2_ULPITLL_DAT3	RW	32	0x0000016C	0x4A10 016C
CONTROL_CORE_PAD0_USBB2_ULPITLL_DAT4_PAD1_USBB2_ULPITLL_DAT5	RW	32	0x00000170	0x4A10 0170
CONTROL_CORE_PAD0_USBB2_ULPITLL_DAT6_PAD1_USBB2_ULPITLL_DAT7	RW	32	0x00000174	0x4A10 0174
CONTROL_CORE_PAD0_USBB2_HSIC_DATA_PAD1_USBB2_HSIC_STROBE	RW	32	0x00000178	0x4A10 0178
CONTROL_CORE_PAD0_KPD_COL3_PAD1_KPD_COL4	RW	32	0x0000017C	0x4A10 017C
CONTROL_CORE_PAD0_KPD_COL5_PAD1_KPD_COL0	RW	32	0x00000180	0x4A10 0180
CONTROL_CORE_PAD0_KPD_COL1_PAD1_KPD_COL2	RW	32	0x00000184	0x4A10 0184
CONTROL_CORE_PAD0_KPD_ROW3_PAD1_KPD_ROW4	RW	32	0x00000188	0x4A10 0188
CONTROL_CORE_PAD0_KPD_ROW5_PAD1_KPD_ROW0	RW	32	0x0000018C	0x4A10 018C
CONTROL_CORE_PAD0_KPD_ROW1_PAD1_KPD_ROW2	RW	32	0x00000190	0x4A10 0190
CONTROL_CORE_PAD0_USBA0_OTG_CE_PAD1_USBA0_OTG_DP	RW	32	0x00000194	0x4A10 0194
CONTROL_CORE_PAD0_USBA0_OTG_DM_PAD1_FREF_CLK1_OUT	RW	32	0x00000198	0x4A10 0198
CONTROL_CORE_PAD0_FREF_CLK2_OUT_PAD1_SYS_NIRQ1	RW	32	0x0000019C	0x4A10 019C
CONTROL_CORE_PAD0_SYS_NIRQ2_PAD1_SYS_BOOT0	RW	32	0x000001A0	0x4A10 01A0

Register Name	Type	Register Width (Bits)	Address Offset	SYSCTRL_PADCONF_CORE Physical Address
CONTROL_CORE_PAD0_SYS_BOOT1_PAD1_SYS_BOOT2	RW	32	0x000001A4	0x4A10 01A4
CONTROL_CORE_PAD0_SYS_BOOT3_PAD1_SYS_BOOT4	RW	32	0x000001A8	0x4A10 01A8
CONTROL_CORE_PAD0_SYS_BOOT5_PAD1_DPM_EMU0	RW	32	0x000001AC	0x4A10 01AC
CONTROL_CORE_PAD0_DPM_EMU1_PAD1_DPM_EMU2	RW	32	0x000001B0	0x4A10 01B0
CONTROL_CORE_PAD0_DPM_EMU3_PAD1_DPM_EMU4	RW	32	0x000001B4	0x4A10 01B4
CONTROL_CORE_PAD0_DPM_EMU5_PAD1_DPM_EMU6	RW	32	0x000001B8	0x4A10 01B8
CONTROL_CORE_PAD0_DPM_EMU7_PAD1_DPM_EMU8	RW	32	0x000001BC	0x4A10 01BC
CONTROL_CORE_PAD0_DPM_EMU9_PAD1_DPM_EMU10	RW	32	0x000001C0	0x4A10 01C0
CONTROL_CORE_PAD0_DPM_EMU11_PAD1_DPM_EMU12	RW	32	0x000001C4	0x4A10 01C4
CONTROL_CORE_PAD0_DPM_EMU13_PAD1_DPM_EMU14	RW	32	0x000001C8	0x4A10 01C8
CONTROL_CORE_PAD0_DPM_EMU15_PAD1_DPM_EMU16	RW	32	0x000001CC	0x4A10 01CC
CONTROL_CORE_PAD0_DPM_EMU17_PAD1_DPM_EMU18	RW	32	0x000001D0	0x4A10 01D0
~~CONTROL_CORE_PAD0_DPM_EMU19~~ CONTROL_CORE_PAD0_DPM_EMU19_PAD1_CSI22_DX2	RW	32	0x000001D4	0x4A10 01D4
CONTROL_PADCONF_WAKEUP-EVENT_0	R	32	0x000001D8	0x4A10 01D8
CONTROL_PADCONF_WAKEUP-EVENT_1	R	32	0x000001DC	0x4A10 01DC
CONTROL_PADCONF_WAKEUP-EVENT_2	R	32	0x000001E0	0x4A10 01E0
CONTROL_PADCONF_WAKEUP-EVENT_3	R	32	0x000001E4	0x4A10 01E4
CONTROL_PADCONF_WAKEUP-EVENT_4	R	32	0x000001E8	0x4A10 01E8
CONTROL_PADCONF_WAKEUP-EVENT_5	R	32	0x000001EC	0x4A10 01EC
CONTROL_PADCONF_WAKEUP-EVENT_6	R	32	0x000001F0	0x4A10 01F0
CONTROL_CORE_PAD0_CSI22_DY2	RW	32	0x000001F4	0x4A10 01F4
CONTROL_PADCONF_GLOBAL	RW	32	0x000005A0	0x4A10 05A0

Register Name	Type	Register Width (Bits)	Address Offset	SYSCTRL_PADCONF_CORE Physical Address
CONTROL_CORE_PADCONF_MODE	RW	32	0x000005A4	0x4A10 05A4
CONTROL_SMART1IO_PADCONF_0	RW	32	0x000005A8	0x4A10 05A8
CONTROL_SMART1IO_PADCONF_1	RW	32	0x000005AC	0x4A10 05AC
CONTROL_SMART2IO_PADCONF_0	RW	32	0x000005B0	0x4A10 05B0
CONTROL_SMART2IO_PADCONF_1	RW	32	0x000005B4	0x4A10 05B4
CONTROL_SMART3IO_PADCONF_0	RW	32	0x000005B8	0x4A10 05B8
CONTROL_SMART3IO_PADCONF_1	RW	32	0x000005BC	0x4A10 05BC
CONTROL_SMART3IO_PADCONF_2	RW	32	0x000005C0	0x4A10 05C0
CONTROL_USBB_HSIC	RW	32	0x000005C4	0x4A10 05C4
CONTROL_SMART3IO_PADCONF_3	RW	32	0x000005C8	0x4A10 05C8
CONTROL_SMART2IO_PADCONF_2	RW	32	0x000005CC	0x4A10 05CC
CONTROL_SMART1IO_PADCONF_2	RW	32	0x000005D0	0x4A10 05D0
CONTROL_SMART1IO_PADCONF_3	RW	32	0x000005D4	0x4A10 05D4
CONTROL_C2CIO_PADCONF_0	RW	32	0x000005D8	0x4A10 05D8
CONTROL_PBIASLITE	RW	32	0x00000600	0x4A10 0600
CONTROL_I2C_0	RW	32	0x00000604	0x4A10 0604
CONTROL_CAMERA_RX	RW	32	0x00000608	0x4A10 0608
CONTROL_AVDAC	RW	32	0x0000060C	0x4A10 060C
RESERVED	RW	32	0x00000610	0x4A10 0610
CONTROL_MMC2	RW	32	0x00000614	0x4A10 0614
CONTROL_DSIPHY	RW	32	0x00000618	0x4A10 0618
CONTROL_MCBSPLP	RW	32	0x0000061C	0x4A10 061C
CONTROL_USB2PHYCORE	RW	32	0x00000620	0x4A10 0620
CONTROL_I2C_1	RW	32	0x00000624	0x4A10 0624
CONTROL_MMC1	RW	32	0x00000628	0x4A10 0628
CONTROL_HSI	RW	32	0x0000062C	0x4A10 062C
CONTROL_USB	RW	32	0x00000630	0x4A10 0630
CONTROL_HDQ	RW	32	0x00000634	0x4A10 0634
CONTROL_LPDDR2IO1_0	RW	32	0x00000638	0x4A10 0638
CONTROL_LPDDR2IO1_1	RW	32	0x0000063C	0x4A10 063C
CONTROL_LPDDR2IO1_2	RW	32	0x00000640	0x4A10 0640
CONTROL_LPDDR2IO1_3	RW	32	0x00000644	0x4A10 0644
CONTROL_LPDDR2IO2_0	RW	32	0x00000648	0x4A10 0648

Register Name	Type	Register Width (Bits)	Address Offset	SYSCTRL_PADCONF_CORE Physical Address
CONTROL_LPDDR2IO2_1	RW	32	0x0000064C	0x4A10 064C
CONTROL_LPDDR2IO2_2	RW	32	0x00000650	0x4A10 0650
CONTROL_LPDDR2IO2_3	RW	32	0x00000654	0x4A10 0654
CONTROL_BUS_HOLD	RW	32	0x00000658	0x4A10 0658
CONTROL_C2C	RW	32	0x0000065C	0x4A10 065C
CONTROL_CORE_CONTROL_SPARE_RW	RW	32	0x00000660	0x4A10 0660
CONTROL_CORE_CONTROL_SPARE_R	R	32	0x00000664	0x4A10 0664
CONTROL_CORE_CONTROL_SPARE_R_C0	RW	32	0x00000668	0x4A10 0668
CONTROL_CORE_CONTROL_SPARE_RW1	RW	32	0x0000066C	0x4A10 066C
CONTROL_CORE_CONTROL_SPARE_RW2	RW	32	0x00000670	0x4A10 0670
CONTROL_CORE_CONTROL_SPARE_RW3	RW	32	0x00000674	0x4A10 0674
CONTROL_CORE_CONTROL_SPARE_RW4	RW	32	0x00000678	0x4A10 0678
CONTROL_CORE_CONTROL_SPARE_RW5	RW	32	0x0000067C	0x4A10 067C
CONTROL_CORE_CONTROL_SPARE_RW6	RW	32	0x00000680	0x4A10 0680
CONTROL_CORE_CONTROL_SPARE_RW7	RW	32	0x00000684	0x4A10 0684
CONTROL_CORE_CONTROL_SPARE_RW8	RW	32	0x00000688	0x4A10 0688
CONTROL_CORE_CONTROL_SPARE_RW9	RW	32	0x0000068C	0x4A10 068C
CONTROL_CORE_CONTROL_SPARE_R1	R	32	0x0000068C	0x4A10 068C
RESERVED	RW	32	0x00000694	0x4A10 0694
CONTROL_EFUSE_1	RW	32	0x00000700	0x4A10 0700
CONTROL_EFUSE_2	RW	32	0x00000704	0x4A10 0704
CONTROL_EFUSE_3	R	32	0x00000708	0x4A10 0708
CONTROL_EFUSE_4	RW	32	0x0000070C	0x4A10 070C

The Video DAC (VDAC) functionality is not supported

18.6.7. SYSCTRL_PADCONF_CORE Register Description

Note

This section contains only modified registers.

Table 18.50. CONTROL_CORE_PAD0_CSI21_DX3_PAD1_CSI21_DY3

Address Offset	0x0000 00AC		
Physical Address	See Table 18.49	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads csi21_dx3 and csi21_dy3 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CSI21_DY3_WAKEUPEVENT	CSI21_DY3_WAKEUPENABLE	RESERVED					CSI21_DY3_INPUTENABLE	RESERVED			CSI21_DY3_PULLTYPESELECT	CSI21_DY3_PULLUDENABLE	CSI21_DY3_MUXMODE			CSI21_DX3_WAKEUPEVENT	CSI21_DX3_WAKEUPENABLE	RESERVED				CSI21_DX3_INPUTENABLE	RESERVED					CSI21_DX3_PULLTYPESELECT	CSI21_DX3_PULLUDENABLE	CSI21_DX3_MUXMODE	

Bits	Field Name	Description	Type	Reset
31	CSI21_DY3_WAKE-UPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	CSI21_DY3_WAKE-UPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x00
24	CSI21_DY3_INPUTENABLE	Input enable value for pad csi21_dy3 0x0: Input buffere of I/O cell is disabled 0x1: Input buffere of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	CSI21_DY3_PULL-TYPESELECT	pullup/down selection for pad csi21_dy3 0x0: pulldown selected 0x1: pullup selected	RW	0
19	CSI21_DY3_PULLUDENAB LE	pullup/down enable for pad csi21_dy3 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	CSI21_DY3_MUXMODE	Functional multiplexing selection for pad csi21_dy3 0x0: Select csi21_dy3 0x1: Select cam2_d6 0x3: Select gpi_74 0x7: Select safe_mode	RW	0x7

Bits	Field Name	Description	Type	Reset
15	CSI21_DX3_WAKE-UPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	CSI21_DX3_WAKE-UPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x00
8	CSI21_DX3_INPUTENABLE	Input enable value for pad csi21_dx3 0x0: Input buffere of I/O cell is disabled 0x1: Input buffere of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	CSI21_DX3_PULL-TYPESELECT	pullup/down selection for pad csi21_dx3 0x0: pulldown selected 0x1: pullup selected	RW	0
3	CSI21_DX3_PULLUDENABLE	pullup/down enable for pad csi21_dx3 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	CSI21_DX3_MUXMODE	Functional multiplexing selection for pad csi21_dx3 0x0: Select csi21_dx3 0x1: Select cam2_d7 0x3: Select gpi_73 0x7: Select safe_mode	RW	0x7

Table 18.51. Register Call Summary for Register CONTROL_CORE_PAD0_CSI21_DX3_PAD1_CSI21_DY3

Control Module Functional Description

- PAD Functional Multiplexing and Configuration:[0]

Table 18.52. CONTROL_CORE_PAD0_CSI21_DX4_PAD1_CSI21_DY4

Address Offset	0x0000 00B0		
Physical Address	SeeTable 18.49	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads csi21_dx4 and csi21_dy4 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CSI21_DY4_WAKEUPEVENT	CSI21_DY4_WAKEUPENABLE	RESERVED					CSI21_DY4_INPUTENABLE	RESERVED			CSI21_DY4_PULLTYPESELECT	CSI21_DY4_PULLUDENABLE	CSI21_DY4_MUXMODE			CSI21_DX4_WAKEUPEVENT	CSI21_DX4_WAKEUPENABLE	RESERVED				CSI21_DX4_INPUTENABLE	RESERVED					CSI21_DX4_PULLTYPESELECT	CSI21_DX4_PULLUDENABLE	CSI21_DX4_MUXMODE	

Bits	Field Name	Description	Type	Reset
31	CSI21_DY4_WAKE-UPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	CSI21_DY4_WAKE-UPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x00
24	CSI21_DY4_INPUTENABLE	Input enable value for pad csi21_dy4 0x0: Input buffere of I/O cell is disabled 0x1: Input buffere of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	CSI21_DY4_PULL-TYPESELECT	pullup/down selection for pad csi21_dy4 0x0: pulldown selected 0x1: pullup selected	RW	0
19	CSI21_DY4_PULLUDENABLE	pullup/down enable for pad csi21_dy4 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	CSI21_DY4_MUXMODE	Functional multiplexing selection for pad csi21_dy4 0x0: Select csi21_dy4 0x1: Select cam2_d4 0x3: Select gpi_76 0x7: Select safe_mode	RW	0x7
15	CSI21_DX4_WAKE-UPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	CSI21_DX4_WAKE-UPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x00
8	CSI21_DX4_INPUTENABLE	Input enable value for pad csi21_dx4 0x0: Input buffere of I/O cell is disabled 0x1: Input buffere of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	CSI21_DX4_PULL-TYPESELECT	pullup/down selection for pad csi21_dx4 0x0: pulldown selected 0x1: pullup selected	RW	0
3	CSI21_DX4_PULLUDENABLE	pullup/down enable for pad csi21_dx4 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	CSI21_DX4_MUXMODE	Functional multiplexing selection for pad csi21_dx4 0x0: Select csi21_dx4 0x1: Select cam2_d5 0x3: Select gpi_75 0x7: Select safe_mode	RW	0x7

Table 18.53. Register Call Summary for Register CONTROL_CORE_PAD0_CSI21_DX4_PAD1_CSI21_DY4

Control Module Functional Description

- PAD Functional Multiplexing and Configuration:[0]

Table 18.54. CONTROL_CORE_PAD0_CSI22_DX0_PAD1_CSI22_DY0

Address Offset	0x0000 00B4		
Physical Address	SeeTable 18.49	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads csi22_dx0 and csi22_dy0 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CSI22_DY0_WAKEUPEVENT	CSI22_DY0_WAKEUPENABLE	RESERVED					CSI22_DY0_INPUTENABLE	RESERVED			CSI22_DY0_PULLTYPESELECT	CSI22_DY0_PULLUDENABLE	CSI22_DY0_MUXMODE			CSI22_DX0_WAKEUPEVENT	CSI22_DX0_WAKEUPENABLE	RESERVED				CSI22_DX0_INPUTENABLE	RESERVED				CSI22_DX0_PULLTYPESELECT	CSI22_DX0_PULLUDENABLE	CSI22_DX0_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	CSI22_DY0_WAKE-UPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	CSI22_DY0_WAKE-UPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x00
24	CSI22_DY0_INPUTENABLE	Input enable value for pad csi22_dy0 0x0: Input buffere of I/O cell is disabled 0x1: Input buffere of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	CSI22_DY0_PULL-TYPESELECT	pullup/down selection for pad csi22_dy0 0x0: pulldown selected 0x1: pullup selected	RW	0
19	CSI22_DY0_PULLUDENAB LE	pullup/down enable for pad csi22_dy0 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	CSI22_DY0_MUXMODE	Functional multiplexing selection for pad csi22_dy0 0x0: Select csi22_dy0 0x1: Select cam2_d2 0x2: Select cam2_d13 0x3: Select gpi_78 0x7: Select safe_mode	RW	0x7

Bits	Field Name	Description	Type	Reset
15	CSI22_DX0_WAKE-UPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	CSI22_DX0_WAKE-UPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x00
8	CSI22_DX0_INPUTENABLE	Input enable value for pad csi22_dx0 0x0: Input buffere of I/O cell is disabled 0x1: Input buffere of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	CSI22_DX0_PULL-TYPESELECT	pullup/down selection for pad csi22_dx0 0x0: pulldown selected 0x1: pullup selected	RW	0
3	CSI22_DX0_PULLUDENABLE	pullup/down enable for pad csi22_dx0 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	CSI22_DX0_MUXMODE	Functional multiplexing selection for pad csi22_dx0 0x0: Select csi22_dx0 0x1: Select cam2_d3 0x2: Select cam2_d12 0x3: Select gpi_77 0x7: Select safe_mode	RW	0x7

Table 18.55. Register Call Summary for Register CONTROL_CORE_PAD0_CSI22_DX0_PAD1_CSI22_DY0

Control Module Functional Description

- PAD Functional Multiplexing and Configuration:[0][1]

Table 18.56. CONTROL_CORE_PAD0_CSI22_DX1_PAD1_CSI22_DY1

Address Offset	0x0000 00B8		
Physical Address	SeeTable 18.49	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads csi22_dx1 and csi22_dy1 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CSI22_DY1_WAKEUPEVENT	CSI22_DY1_WAKEUPENABLE	RESERVED					CSI22_DY1_INPUTENABLE	RESERVED			CSI22_DY1_PULLTYPESELECT	CSI22_DY1_PULLUDENABLE	CSI22_DY1_MUXMODE			CSI22_DX1_WAKEUPEVENT	CSI22_DX1_WAKEUPENABLE	RESERVED					CSI22_DX1_INPUTENABLE	RESERVED					CSI22_DX1_PULLTYPESELECT	CSI22_DX1_PULLUDENABLE	CSI22_DX1_MUXMODE	

Bits	Field Name	Description	Type	Reset
31	CSI22_DY1_WAKE-UPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	CSI22_DY1_WAKE-UPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x00
24	CSI22_DY1_INPUTENABLE	Input enable value for pad csi22_dy1 0x0: Input buffere of I/O cell is disabled 0x1: Input buffere of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	CSI22_DY1_PULL-TYPESELECT	pullup/down selection for pad csi22_dy1 0x0: pulldown selected 0x1: pullup selected	RW	0
19	CSI22_DY1_PULLUDENABLE	pullup/down enable for pad csi22_dy1 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	CSI22_DY1_MUXMODE	Functional multiplexing selection for pad csi22_dy1 0x0: Select csi22_dy1 0x1: Select cam2_d0 0x2: Select cam2_d15 0x3: Select gpi_80 0x7: Select safe_mode	RW	0x7
15	CSI22_DX1_WAKE-UPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	CSI22_DX1_WAKE-UPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x00
8	CSI22_DX1_INPUTENABLE	Input enable value for pad csi22_dx1 0x0: Input buffere of I/O cell is disabled 0x1: Input buffere of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	CSI22_DX1_PULL-TYPESELECT	pullup/down selection for pad csi22_dx1 0x0: pulldown selected 0x1: pullup selected	RW	0
3	CSI22_DX1_PULLUDENABLE	pullup/down enable for pad csi22_dx1 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	CSI22_DX1_MUXMODE	Functional multiplexing selection for pad csi22_dx1 0x0: Select csi22_dx1 0x1: Select cam2_d1 0x2: Select cam2_d14 0x3: Select gpi_79 0x7: Select safe_mode	RW	0x7

Table 18.57. Register Call Summary for Register CONTROL_CORE_PAD0_CSI22_DX1_PAD1_CSI22_DY1

Control Module Functional Description

- PAD Functional Multiplexing and Configuration:[0][1]

Table 18.58. CONTROL_CORE_PAD0_CAM_SHUTTER_PAD1_CAM_STROBE

Address Offset	0x0000 00BC		
Physical Address	See Table 18.49	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads cam_shutter and cam_strobe Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAM_STROBE_WAKEUPEVENT	CAM_STROBE_WAKEUPENABLE	CAM_STROBE_OFFMODEPULLTYPESELECT	CAM_STROBE_OFFMODEPULLUDENABLE	CAM_STROBE_OFFMODEOUTVALUE	CAM_STROBE_OFFMODEOUTENABLE	CAM_STROBE_OFFMODEENABLE	CAM_STROBE_INPUTENABLE	RESERVED			CAM_STROBE_PULLTYPESELECT	CAM_STROBE_PULLUDENABLE	CAM_STROBE_MUXMODE			CAM_SHUTTER_WAKEUPEVENT	CAM_SHUTTER_WAKEUPENABLE	CAM_SHUTTER_OFFMODEPULLTYPESELECT	CAM_SHUTTER_OFFMODEPULLUDENABLE	CAM_SHUTTER_OFFMODEOUTVALUE	CAM_SHUTTER_OFFMODEOUTENABLE	CAM_SHUTTER_OFFMODEENABLE	CAM_SHUTTER_INPUTENABLE	RESERVED			CAM_SHUTTER_PULLTYPESELECT	CAM_SHUTTER_PULLUDENABLE	CAM_SHUTTER_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	CAM_STROBE_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	CAM_STROBE_WAKEUPE-NABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	CAM_STROBE_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad cam_strobe 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	CAM_STROBE_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad cam_strobe 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	CAM_STROBE_OFFMODE-OUTVALUE	OffMode mode output value for pad cam_strobe 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	CAM_STROBE_OFFMODE-OUTENABLE	OffMode mode output enable value for pad cam_strobe. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0

Bits	Field Name	Description	Type	Reset
25	CAM_STROBE_OFF-MODEENABLE	OffMode mode override control for pad cam_strobe 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	CAM_STROBE_INPUTENABLE	Input enable value for pad cam_strobe 0x0: Input buffere of I/O cell is disabled 0x1: Input buffere of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	CAM_STROBE_PULLTYPESELECT	pullup/down selection for pad cam_strobe 0x0: pulldown selected 0x1: pullup selected	RW	0
19	CAM_STROBE_PULLUDE-NABLE	pullup/down enable for pad cam_strobe 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	CAM_STROBE_MUXMODE	Functional multiplexing selection for pad cam_strobe 0x0: Select cam_strobe 0x2: Select cam2_vs 0x3: Select gpio_82 0x7: Select safe_mode	RW	0x7
15	CAM_SHUTTER_WAKEUP-EVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	CAM_SHUTTER_WAKEUP-ENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	CAM_SHUTTER_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad cam_shutter 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	CAM_SHUTTER_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad cam_shutter 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	CAM_SHUTTER_OFFMODEOUTVALUE	OffMode mode output value for pad cam_shutter 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	CAM_SHUTTER_OFFMODEOUTENABLE	OffMode mode output enable value for pad cam_shutter. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	CAM_SHUTTER_OFFMODEENABLE	OffMode mode override control for pad cam_shutter 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	CAM_SHUTTER_IN-PUTENABLE	Input enable value for pad cam_shutter 0x0: Input buffere of I/O cell is disabled	RW	1

Bits	Field Name	Description	Type	Reset
		0x1: Input buffere of I/O cell is enabled		
7:5	RESERVED		R	0x0
4	CAM_SHUTTER_ PULLTYPESELECT	pullup/down selection for pad cam_shutter 0x0: pulldown selected 0x1: pullup selected	RW	0
3	CAM_SHUTTER_ PULLUDENABLE	pullup/down enable for pad cam_shutter 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	CAM_SHUTTER_ MUXMODE	Functional multiplexing selection for pad cam_shutter 0x0: Select cam_shutter 0x2: Select cam2_hs 0x3: Select gpio_81 0x7: Select safe_mode	RW	0x7

Table 18.59. Register Call Summary for Register CONTROL_CORE_PAD0_CAM_SHUTTER_PAD1_CAM_STROBE

Control Module Functional Description

- PAD Functional Multiplexing and Configuration:[0]

Table 18.60. CONTROL_CORE_PAD0_CAM_GLOBALRESET_PAD1_USBB1_ULPITLL_CLK

Address Offset	0x0000 00C0		
Physical Address	SeeTable 18.49	**Instance**	SYSCTRL_PADCONF_ CORE
Description	Register control for Pads cam_globalreset and usbb1_ulpitll_clk Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USBB1_ULPITLL_CLK_WAKEUPEVENT	USBB1_ULPITLL_CLK_WAKEUPENABLE	USBB1_ULPITLL_CLK_OFFMODEPULLTYPESELECT	USBB1_ULPITLL_CLK_OFFMODEPULLUDENABLE	USBB1_ULPITLL_CLK_OFFMODEOUTVALUE	USBB1_ULPITLL_CLK_OFFMODEOUTENABLE	USBB1_ULPITLL_CLK_OFFMODEENABLE	USBB1_ULPITLL_CLK_INPUTENABLE	RESERVED			USBB1_ULPITLL_CLK_PULLTYPESELECT	USBB1_ULPITLL_CLK_PULLUDENABLE	USBB1_ULPITLL_CLK_MUXMODE			CAM_GLOBALRESET_WAKEUPEVENT	CAM_GLOBALRESET_WAKEUPENABLE	CAM_GLOBALRESET_OFFMODEPULLTYPESELECT	CAM_GLOBALRESET_OFFMODEPULLUDENABLE	CAM_GLOBALRESET_OFFMODEOUTVALUE	CAM_GLOBALRESET_OFFMODEOUTENABLE	CAM_GLOBALRESET_OFFMODEENABLE	CAM_GLOBALRESET_INPUTENABLE	RESERVED			CAM_GLOBALRESET_PULLTYPESELECT	CAM_GLOBALRESET_PULLUDENABLE	CAM_GLOBALRESET_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	US-BB1_ULPITLL_CLK_WAKE-UPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0

Bits	Field Name	Description	Type	Reset
30	USBB1_ULPITLL_CLK_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	USBB1_ULPITLL_CLK_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad usbb1_ulpitll_clk 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	USBB1_ULPITLL_CLK_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad usbb1_ulpitll_clk 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	USBB1_ULPITLL_CLK_OFFMODEOUTVALUE	OffMode mode output value for pad usbb1_ulpitll_clk 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	USBB1_ULPITLL_CLK_OFFMODEOUTENABLE	OffMode mode output enable value for pad usb b1_ulpitll_clk. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	USBB1_ULPITLL_CLK_OFFMODEENABLE	OffMode mode override control for pad usbb1_ulpitll_clk 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	USBB1_ULPITLL_CLK_INPUTENABLE	Input enable value for pad usbb1_ulpitll_clk 0x0: Input buffere of I/O cell is disabled 0x1: Input buffere of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	USBB1_ULPITLL_CLK_PULLTYPESELECT	pullup/down selection for pad usbb1_ulpitll_clk 0x0: pulldown selected 0x1: pullup selected	RW	0
19	USBB1_ULPITLL_CLK_PULLUDENABLE	pullup/down enable for pad usbb1_ulpitll_clk 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	USBB1_ULPITLL_CLK_MUXMODE	Functional multiplexing selection for pad usbb1_ulpitll_clk 0x0: Select usbb1_ulpitll_clk 0x1: Select hsi1_cawake 0x3: Select gpio_84 0x4: Select usbb1_ulpiphy_clk 0x6: Select hw_dbg20 0x7: Select safe_mode	RW	0x7
15	CAM_GLOBALRESET_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	CAM_GLOBALRESET_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0

Bits	Field Name	Description	Type	Reset
13	CAM_GLOBALRESET_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad cam_globalreset 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	CAM_GLOBALRESET_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad cam_globalreset 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	CAM_GLOBALRESET_OFFMODEOUTVALUE	OffMode mode output value for pad cam_global reset 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	CAM_GLOBALRESET_OFFMODEOUTENABLE	OffMode mode output enable value for pad cam_globalreset. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	CAM_GLOBALRESET_OFFMODEENABLE	OffMode mode override control for pad cam_global reset 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	CAM_GLOBALRESET_INPUTENABLE	Input enable value for pad cam_globalreset 0x0: Input buffere of I/O cell is disabled 0x1: Input buffere of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	CAM_GLOBALRESET_PULLTYPESELECT	pullup/down selection for pad cam_globalreset 0x0: pulldown selected 0x1: pullup selected	RW	0
3	CAM_GLOBALRESET_PULLUDENABLE	pullup/down enable for pad cam_globalreset 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	CAM_GLOBALRESET_MUXMODE	Functional multiplexing selection for pad cam_globalreset 0x0: Select cam_globalreset 0x2: Select cam2_pclk 0x3: Select gpio_83 0x7: Select safe_mode	RW	0x7

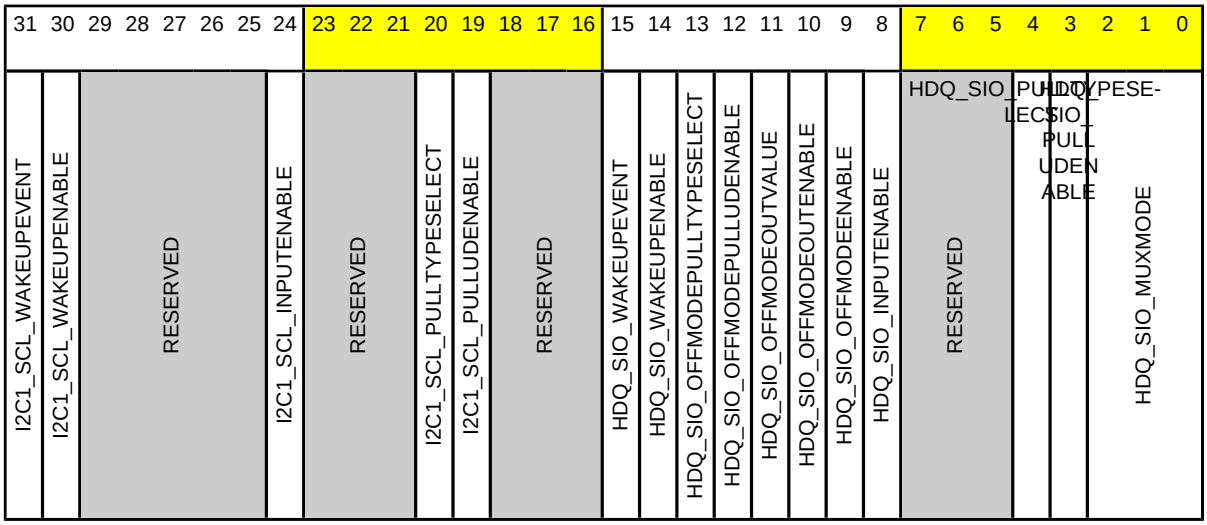
Table 18.61. Register Call Summary for Register CONTROL_CORE_PAD0_CAM_GLOBALRESET_PAD1_USBB1_ULPITLL_CLK

Control Module Functional Description

- PAD Functional Multiplexing and Configuration:[0]

Table 18.62. CONTROL_CORE_PAD0_HDQ_SIO_PAD1_I2C1_SCL

Address Offset	0x0000 0120		
Physical Address	SeeTable 18.49	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads hdq_sio and i2c1_scl Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		



Bits	Field Name	Description	Type	Reset
31	I2C1_SCL_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	I2C1_SCL_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x00
24	I2C1_SCL_INPUTENABLE	Input enable value for pad i2c1_scl 0x0: Input buffere of I/O cell is disabled 0x1: Input buffere of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	I2C1_SCL_PULLTYPES-ELECT	pullup/down selection for pad i2c1_scl 0x0: pulldown selected 0x1: pullup selected	RW	~~1~~0x0
19	I2C1_SCL_PULLUDENABLE	pullup/down enable for pad i2c1_scl 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	~~1~~0x0
18:16	RESERVED		R	0x0
15	HDQ_SIO_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	HDQ_SIO_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	HDQ_SIO_OFFMODEPULLTYPESELECT	OffMode mode Pull-Up/Down selection for pad hdq_sio 0x0: Offmode Pull-Down selected 0x1: Offmode Pull-Up selected	RW	0x0
12	HDQ_SIO_OFFMODEPUL-LUDENABLE	OffMode mode Pull-Up/Down enable for pad hdq_sio 0x0: Offmode Pull-Up/Down disabled 0x1: Offmode Pull-Up/Down enabled	RW	0x0

Bits	Field Name	Description	Type	Reset
11	HDQ_SIO_OFFMODEOUT-VALUE	OffMode mode output value for pad hdq_sio 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	HDQ_SIO_OFFMODEOUTENABLE	OffMode mode output enable value for pad hdq_sio . This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	HDQ_SIO_OFFMODEENABLE	OffMode mode override control for pad hdq_sio 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	HDQ_SIO_INPUTENABLE	Input enable value for pad hdq_sio 0x0: Input buffere of I/O cell is disabled 0x1: Input buffere of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	HDQ_SIO_PULLTYPESE-LECT	Pull-Up/Down selection for pad hdq_sio 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0x0
3	HDQ_SIO_PULLUDENABLE	Pull-Up/Down enable for pad hdq_sio 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	0x0
2:0	HDQ_SIO_MUXMODE	Functional multiplexing selection for pad hdq_sio 0x0: Select hdq_sio 0x1: Select i2c3_sccb 0x2: Select i2c2_sccb 0x3: Select gpio_127 0x7: Select safe_mode	RW	0x7

Table 18.63. Register Call Summary for Register CONTROL_CORE_PAD0_HDQ_SIO_PAD1_I2C1_SCL

Control Module Functional Description

- PAD Functional Multiplexing and Configuration:[0]

Table 18.64. CONTROL_CORE_PAD0_UART3_CTS_RCTX_PAD1_UART3_RTS_SD

Address Offset	0x0000 0140		
Physical Address	0x4A10 0140	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads uart3_cts_rctx and uart3_rts_sd Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UART3_RTS_SD_WAKEUPEVENT	UART3_RTS_SD_WAKEUPENABLE	UART3_RTS_SD_OFFMODEPULLTYPESELECT	UART3_RTS_SD_OFFMODEPULLUDENABLE	UART3_RTS_SD_OFFMODEOUTVALUE	UART3_RTS_SD_OFFMODEOUTENABLE	UART3_RTS_SD_OFFMODEENABLE	UART3_RTS_SD_INPUTENABLE	RESERVED			UART3_RTS_SD_PULLTYPESELECT	UART3_RTS_SD_PULLUDENABLE	UART3_RTS_SD_MUXMODE			UART3_CTS_RCTX_WAKEUPEVENT	UART3_CTS_RCTX_WAKEUPENABLE	UART3_CTS_RCTX_OFFMODEPULLTYPESELECT	UART3_CTS_RCTX_OFFMODEPULLUDENABLE	UART3_CTS_RCTX_OFFMODEOUTVALUE	UART3_CTS_RCTX_OFFMODEOUTENABLE	UART3_CTS_RCTX_OFFMODEENABLE	UART3_CTS_RCTX_INPUTENABLE	RESERVED			UART3_CTS_RCTX_PULLTYPESELECT	UART3_CTS_RCTX_PULLUDENABLE	UART3_CTS_RCTX_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	UART3_RTS_SD_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	UART3_RTS_SD_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	UART3_RTS_SD_OFFMODEPULL-TYPESELECT	OffMode mode pullup/down selection for pad uart3_rts_sd 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	UART3_RTS_SD_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad uart3_rts_sd 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	UART3_RTS_SD_OFFMODEOUTVALUE	OffMode mode output value for pad uart3_rts_sd 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	UART3_RTS_SD_OFFMODEOUTENABLE	OffMode mode output enable value for pad uart3_rts_sd. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	UART3_RTS_SD_OFFMODEENABLE	OffMode mode override control for pad uart3_rts_sd 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	UART3_RTS_SD_INPUTENABLE	Input enable value for pad uart3_rts_sd 0x0: Input buffere of I/O cell is disabled 0x1: Input buffere of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20		pullup/down selection for pad uart3_rts_sd	RW	1

Bits	Field Name	Description	Type	Reset
	UART3_RTS_SD_PULLTYPESELECT	0x0: pulldown selected 0x1: pullup selected		
19	UART3_RTS_SD_PULLUDENABLE	pullup/down enable for pad uart3_rts_sd 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	UART3_RTS_SD_MUXMODE	Functional multiplexing selection for pad uart3_rts_sd 0x0: Select uart3_rts_sd 0x2: Select cam_globalreset 0x3: Select gpio_142 0x7: Select safe_mode	RW	0x7
15	UART3_CTS_RCTX_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	UART3_CTS_RCTX_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	UART3_CTS_RCTX_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad uart3_cts_rctx 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	UART3_CTS_RCTX_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad uart3_cts_rctx 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	UART3_CTS_RCTX_OFF-MODEOUTVALUE	OffMode mode output value for pad uart3_cts_rctx 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	UART3_CTS_RCTX_OFF-MODEOUTENABLE	OffMode mode output enable value for pad uart3_cts_rctx. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	UART3_CTS_RCTX_OFF-MODEENABLE	OffMode mode override control for pad uart3_cts_rctx 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	UART3_CTS_RCTX_INPUTENABLE	Input enable value for pad uart3_cts_rctx 0x0: Input buffere of I/O cell is disabled 0x1: Input buffere of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	UART3_CTS_RCTX_PULLTYPESELECT	pullup/down selection for pad uart3_cts_rctx 0x0: pulldown selected 0x1: pullup selected	RW	1
3	UART3_CTS_RCTX_PUL-LUDENABLE	pullup/down enable for pad uart3_cts_rctx 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1

Bits	Field Name	Description	Type	Reset
2:0	UART3_CTS_RCTX_MUX-MODE	Functional multiplexing selection for pad uart3_cts_rctx 0x0: Select uart3_cts_rctx 0x1: Select uart1_tx 0x3: Select gpio_141 0x7: Select safe_mode	RW	0x7

Table 18.65. Register Call Summary for Register CONTROL_CORE_PAD0_UART3_CTS_RCTX_PAD1_UART3_RTS_SD

Control Module Functional Description

- PAD Functional Multiplexing and Configuration:[0]

Table 18.66. CONTROL_CORE_PAD0_UART3_RX_IRRX_PAD1_UART3_TX_IRTX

Address Offset	0x0000 0144		
Physical Address	0x4A10 0144	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Pads uart3_rx_irrx and uart3_tx_irtx Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UART3_TX_IRTX_WAKEUPEVENT	UART3_TX_IRTX_WAKEUPENABLE	UART3_TX_IRTX_OFFMODEPULLTYPESELECT	UART3_TX_IRTX_OFFMODEPULLUDENABLE	UART3_TX_IRTX_OFFMODEOUTVALUE	UART3_TX_IRTX_OFFMODEOUTENABLE	UART3_TX_IRTX_OFFMODEENABLE	UART3_TX_IRTX_INPUTENABLE	RESERVED			UART3_TX_IRTX_PULLTYPESELECT	UART3_TX_IRTX_PULLUDENABLE	UART3_TX_IRTX_MUXMODE			UART3_RX_IRRX_WAKEUPEVENT	UART3_RX_IRRX_WAKEUPENABLE	UART3_RX_IRRX_OFFMODEPULLTYPESELECT	UART3_RX_IRRX_OFFMODEPULLUDENABLE	UART3_RX_IRRX_OFFMODEOUTVALUE	UART3_RX_IRRX_OFFMODEOUTENABLE	UART3_RX_IRRX_OFFMODEENABLE	UART3_RX_IRRX_INPUTENABLE	RESERVED			UART3_RX_IRRX_PULLTYPESELECT	UART3_RX_IRRX_PULLUDENABLE	UART3_RX_IRRX_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	UART3_TX_IRTX_WAKE-UPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	UART3_TX_IRTX_WAKE-UPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	UART3_TX_IRTX_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad uart3_tx_irtx 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	UART3_TX_IRTX_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad uart3_tx_irtx	RW	0

Bits	Field Name	Description	Type	Reset
		0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled		
27	UART3_TX_IRTX_OFFMODEOUTVALUE	OffMode mode output value for pad uart3_tx_irtx 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	UART3_TX_IRTX_OFFMODEOUTENABLE	OffMode mode output enable value for pad uart3_tx_irtx. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	UART3_TX_IRTX_OFFMODEENABLE	OffMode mode override control for pad uart3_tx_irtx 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	UART3_TX_IRTX_INPUTENABLE	Input enable value for pad uart3_tx_irtx 0x0: Input buffere of I/O cell is disabled 0x1: Input buffere of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	UART3_TX_IRTX_PULL-TYPESELECT	pullup/down selection for pad uart3_tx_irtx 0x0: pulldown selected 0x1: pullup selected	RW	1
19	UART3_TX_IRTX_PULLUDENABLE	pullup/down enable for pad uart3_tx_irtx 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	UART3_TX_IRTX_MUXMODE	Functional multiplexing selection for pad uart3_tx_irtx 0x0: Select uart3_tx_irtx 0x1: Select dmtimer9_pwm_evt 0x2: Select cam_strobe 0x3: Select gpio_144 0x7: Select safe_mode	RW	0x7
15	UART3_RX_IRRX_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	UART3_RX_IRRX_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	UART3_RX_IR-RX_OFFMODEPULLTYPESE-LECT	OffMode mode pullup/down selection for pad uart3_rx_irrx 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	UART3_RX_IRRX_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad uart3_rx_irrx 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	UART3_RX_IRRX_OFFMODEOUTVALUE	OffMode mode output value for pad uart3_rx_irrx 0x0: Set value at 0 0x1: Set value at 1	RW	0

Bits	Field Name	Description	Type	Reset
10	UART3_RX_IR-RX_OFFMODEOUTENABLE	OffMode mode output enable value for pad uart3_rx_irrx. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	UART3_RX_IRRX_OFFMODEENABLE	OffMode mode override control for pad uart3_rx_irrx 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	UART3_RX_IRRX_INPUTENABLE	Input enable value for pad uart3_rx_irrx 0x0: Input buffere of I/O cell is disabled 0x1: Input buffere of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	UART3_RX_IRRX_PULL-TYPESELECT	pullup/down selection for pad uart3_rx_irrx 0x0: pulldown selected 0x1: pullup selected	RW	1
3	UART3_RX_IRRX_PULLUDENABLE	pullup/down enable for pad uart3_rx_irrx 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	UART3_RX_IRRX_MUXMODE	Functional multiplexing selection for pad uart3_rx_irrx 0x0: Select uart3_rx_irrx 0x1: Select dmtimer8_pwm_evt 0x2: Select cam_shutter 0x3: Select gpio_143 0x7: Select safe_mode	RW	0x7

Table 18.67. Register Call Summary for Register CONTROL_CORE_PAD0_UART3_RX_IRRX_PAD1_UART3_TX_IRTX

Control Module Functional Description

- PAD Functional Multiplexing and Configuration:[0]

Table 18.68. CONTROL_CORE_PAD0_KPD_COL3_PAD1_KPD_COL4

Address Offset	0x0000 017C		
Physical Address	SeeTable 18.49	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Padskpd_col3andkpd_col4 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
KPD_COL4_WAKEUPEVENT	KPD_COL4_WAKEUPENABLE	KPD_COL4_OFFMODEPULLTYPESELECT	KPD_COL4_OFFMODEPULLUDENABLE	KPD_COL4_OFFMODEOUTVALUE	KPD_COL4_OFFMODEOUTENABLE	KPD_COL4_OFFMODEENABLE	KPD_COL4_INPUTENABLE	RESERVED			KPD_COL4_PULLTYPESELECT	KPD_COL4_PULLUDENABLE	KPD_COL4_MUXMODE			KPD_COL3_WAKEUPEVENT	KPD_COL3_WAKEUPENABLE	KPD_COL3_OFFMODEPULLTYPESELECT	KPD_COL3_OFFMODEPULLUDENABLE	KPD_COL3_OFFMODEOUTVALUE	KPD_COL3_OFFMODEOUTENABLE	KPD_COL3_OFFMODEENABLE	KPD_COL3_INPUTENABLE	RESERVED			KPD_COL3_PULLTYPESELECT	KPD_COL3_PULLUDENABLE	KPD_COL3_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	KPD_COL4_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	KPD_COL4_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	KPD_COL4_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad kpd_col4 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	KPD_COL4_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad kpd_col4 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	KPD_COL4_OFFMODE OUTVALUE	OffMode mode output value for pad kpd_col4 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	KPD_COL4_OFFMODE OUTENABLE	OffMode mode output enable value for pad kpd_col4. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	KPD_COL4_OFFMODE ENABLE	OffMode mode override control for pad kpd_col4 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	KPD_COL4_INPUTENABLE	Input enable value for pad kpd_col4 0x0: Input buffere of I/O cell is disabled 0x1: Input buffere of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	KPD_COL4_PULLTYPES-ELECT	pullup/down selection for pad kpd_col4	RW	0

Bits	Field Name	Description	Type	Reset
		0x0: pulldown selected 0x1: pullup selected		
19	KPD_COL4_PULLUDENABLE	pullup/down enable for pad kpd_col4 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	KPD_COL4_MUXMODE	Functional multiplexing selection for pad kpd_col4 0x0: Selectkpd_col4 0x1: Select kpd_col1 0x2: Select cam2_d1 0x3: Select gpio_172 0x7: Select safe_mode	RW	0x7
15	KPD_COL3_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	KPD_COL3_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	KPD_COL3_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad kpd_col3 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	KPD_COL3_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad kpd_col3 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	KPD_COL3_ OFFMODEOUTVALUE	OffMode mode output value for pad kpd_col3 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	KPD_COL3_ OFFMODEOUTENABLE	OffMode mode output enable value for pad kpd_col3. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	KPD_COL3_ OFFMODEENABLE	OffMode mode override control for pad kpd_col3 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	KPD_COL3_ INPUTENABLE	Input enable value for pad kpd_col3 0x0: Input buffere of I/O cell is disabled 0x1: Input buffere of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	KPD_COL3_ PULLTYPESELECT	pullup/down selection for pad kpd_col3 0x0: pulldown selected 0x1: pullup selected	RW	0

Bits	Field Name	Description	Type	Reset
3	KPD_COL3_ PULLUDENABLE	pullup/down enable for pad kpd_col3 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	KPD_COL3_ MUXMODE	Functional multiplexing selection for pad kpd_col3 0x0: Selectkpd_col3 0x1: Select kpd_col0 0x2: Select cam2_d0 0x3: Select gpio_171 0x7: Select safe_mode	RW	0x7

Table 18.69. Register Call Summary for Register CONTROL_CORE_PAD0_KPD_COL3_PAD1_KPD_COL4

Control Module Functional Description

- PAD Functional Multiplexing and Configuration:[0]

Table 18.70. CONTROL_CORE_PAD0_KPD_COL5_PAD1_KPD_COL0

Address Offset	0x0000 0180		
Physical Address	SeeTable 18.49	**Instance**	SYSCTRL_PADCONF_ CORE
Description	Register control for Padskpd_col5andkpd_col0 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
KPD_COL0_WAKEUPEVENT	KPD_COL0_WAKEUPENABLE	KPD_COL0_OFFMODEPULLTYPESELECT	KPD_COL0_OFFMODEPULLUDENABLE	KPD_COL0_OFFMODEOUTVALUE	KPD_COL0_OFFMODEOUTENABLE	KPD_COL0_OFFMODEENABLE	KPD_COL0_INPUTENABLE	RESERVED			KPD_COL0_PULLTYPESELECT	KPD_COL0_PULLUDENABLE	KPD_COL0_MUXMODE			KPD_COL5_WAKEUPEVENT	KPD_COL5_WAKEUPENABLE	KPD_COL5_OFFMODEPULLTYPESELECT	KPD_COL5_OFFMODEPULLUDENABLE	KPD_COL5_OFFMODEOUTVALUE	KPD_COL5_OFFMODEOUTENABLE	KPD_COL5_OFFMODEENABLE	KPD_COL5_INPUTENABLE	RESERVED			KPD_COL5_PULLTYPESELECT	KPD_COL5_PULLUDENABLE	KPD_COL5_MUXMODE	

Bits	Field Name	Description	Type	Reset
31	KPD_COL0_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	KPD_COL0_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	KPD_COL0_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad kpd_col0 0x0: Offmode pulldown selected	RW	0

Bits	Field Name	Description	Type	Reset
		0x1: Offmode pullup selected		
28	KPD_COL0_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad kpd_col0 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	KPD_COL0_ OFFMODEOUTVALUE	OffMode mode output value for pad kpd_col0 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	KPD_COL0_ OFFMODEOUTENABLE	OffMode mode output enable value for pad kpd_col0. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	KPD_COL0_ OFFMODEENABLE	OffMode mode override control for pad kpd_col0 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	KPD_COL0_INPUTENABLE	Input enable value for pad kpd_col0 0x0: Input buffere of I/O cell is disabled 0x1: Input buffere of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	KPD_COL0_PULLTYPES-ELECT	pullup/down selection for pad kpd_col0 0x0: pulldown selected 0x1: pullup selected	RW	0
19	KPD_COL0_PULLUDENABLE	pullup/down enable for padkpd_col0 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	KPD_COL0_MUXMODE	Functional multiplexing selection for pad kpd_col0 0x0: Selectkpd_col0 0x1: Select kpd_col3 0x2: Select cam2_d3 0x3: Select gpio_174 0x7: Select safe_mode	RW	0x7
15	KPD_COL5_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	KPD_COL5_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	KPD_COL5_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad kpd_col5 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	KPD_COL5_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad kpd_col5 0x0: Offmode pullup/down disabled	RW	0

Bits	Field Name	Description	Type	Reset
		0x1: Offmode pullup/down enabled		
11	KPD_COL5_ OFFMODEOUTVALUE	OffMode mode output value for pad kpd_col5 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	KPD_COL5_ OFFMODEOUTENABLE	OffMode mode output enable value for pad kpd_col5. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	KPD_COL5_ OFFMODEENABLE	OffMode mode override control for pad kpd_col5 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	KPD_COL5_ INPUTENABLE	Input enable value for pad kpd_col5 0x0: Input buffere of I/O cell is disabled 0x1: Input buffere of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	KPD_COL5_ PULLTYPESELECT	pullup/down selection for pad kpd_col5 0x0: pulldown selected 0x1: pullup selected	RW	0
3	KPD_COL5_ PULLUDENABLE	pullup/down enable for pad kpd_col5 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	KPD_COL5_ MUXMODE	Functional multiplexing selection for pad kpd_col5 0x0: Selectkpd_col5 0x1: Select kpd_col2 0x2: Select cam2_d2 0x3: Select gpio_173 0x7: Select safe_mode	RW	0x7

Table 18.71. Register Call Summary for Register CONTROL_CORE_PAD0_KPD_COL5_PAD1_KPD_COL0

Control Module Functional Description
• PAD Functional Multiplexing and Configuration:[0]

Table 18.72. CONTROL_CORE_PAD0_KPD_COL1_PAD1_KPD_COL2

Address Offset	0x0000 0184		
Physical Address	SeeTable 18.49	**Instance**	SYSCTRL_PADCONF_ CORE
Description	Register control for Padskpd_col1andkpd_col2 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
KPD_COL2_WAKEUPEVENT	KPD_COL2_WAKEUPENABLE	KPD_COL2_OFFMODEPULLTYPESELECT	KPD_COL2_OFFMODEPULLUDENABLE	KPD_COL2_OFFMODEOUTVALUE	KPD_COL2_OFFMODEOUTENABLE	KPD_COL2_OFFMODEENABLE	KPD_COL2_INPUTENABLE	RESERVED			KPD_COL2_PULLTYPESELECT	KPD_COL2_PULLUDENABLE	KPD_COL2_MUXMODE			KPD_COL1_WAKEUPEVENT	KPD_COL1_WAKEUPENABLE	KPD_COL1_OFFMODEPULLTYPESELECT	KPD_COL1_OFFMODEPULLUDENABLE	KPD_COL1_OFFMODEOUTVALUE	KPD_COL1_OFFMODEOUTENABLE	KPD_COL1_OFFMODEENABLE	KPD_COL1_INPUTENABLE	RESERVED			KPD_COL1_PULLTYPESELECT	KPD_COL1_PULLUDENABLE	KPD_COL1_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	KPD_COL2_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	KPD_COL2_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	KPD_COL2_OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad kpd_col2 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
28	KPD_COL2_OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad kpd_col2 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
27	KPD_COL2_OFFMODEOUTVALUE	OffMode mode output value for pad kpd_col2 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	KPD_COL2_OFFMODEOUTENABLE	OffMode mode output enable value for pad kpd_col2. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	KPD_COL2_OFFMODEENABLE	OffMode mode override control for pad kpd_col2 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
24	KPD_COL2_INPUTENABLE	Input enable value for pad kpd_col2 0x0: Input buffere of I/O cell is disabled 0x1: Input buffere of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	KPD_COL2_PULLTYPESELECT	pullup/down selection for pad kpd_col2	RW	0

Bits	Field Name	Description	Type	Reset
		0x0: pulldown selected 0x1: pullup selected		
19	KPD_COL2_ PULLUDENABLE	pullup/down enable for pad kpd_col2 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	KPD_COL2_ MUXMODE	Functional multiplexing selection for pad kpd_col2 0x0: Selectkpd_col2 0x1: Select kpd_col5 0x2: Select cam2_d10 0x3: Select gpio_1 0x7: Select safe_mode	RW	0x7
15	KPD_COL1_ WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	KPD_COL1_ WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	KPD_COL1_ OFFMODEPULLTYPESELECT	OffMode mode pullup/down selection for pad kpd_col1 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0
12	KPD_COL1_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad kpd_col1 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	KPD_COL1_ OFFMODEOUTVALUE	OffMode mode output value for pad kpd_col1 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	KPD_COL1_ OFFMODEOUTENABLE	OffMode mode output enable value for pad kpd_col1. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	KPD_COL1_ OFFMODEENABLE	OffMode mode override control for pad kpd_col1 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	KPD_COL1_ INPUTENABLE	Input enable value for pad kpd_col1 0x0: Input buffere of I/O cell is disabled 0x1: Input buffere of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	KPD_COL1_ PULLTYPESELECT	pullup/down selection for pad kpd_col1 0x0: pulldown selected 0x1: pullup selected	RW	0

Bits	Field Name	Description	Type	Reset
3	KPD_COL1_ PULLUDENABLE	pullup/down enable for pad kpd_col1 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	KPD_COL1_ MUXMODE	Functional multiplexing selection for pad kpd_col1 0x0: Selectkpd_col1 0x1: Select kpd_col4 0x2: Select cam2_d8 0x3: Select gpio_0 0x7: Select safe_mode	RW	0x7

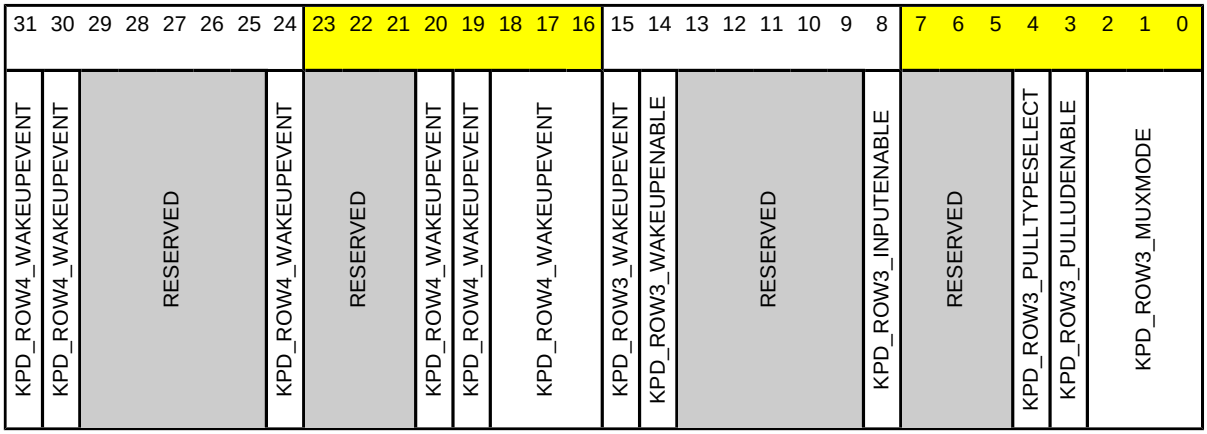
Table 18.73. Register Call Summary for Register CONTROL_CORE_PAD0_KPD_COL1_PAD1_KPD_COL2

Control Module Functional Description

- PAD Functional Multiplexing and Configuration:[0]

Table 18.74. CONTROL_CORE_PAD0_KPD_ROW3_PAD1_KPD_ROW4

Address Offset	0x0000 0188		
Physical Address	SeeTable 18.49	**Instance**	SYSCTRL_PADCONF_ CORE
Description	Register control for Padskpd_row3andkpd_row4 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		



Bits	Field Name	Description	Type	Reset
31	KPD_ROW4_WAKEUPE VENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	KPD_ROW4_WAKEUPE NABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	KPD_ROW4_OFFMODEPULLTYPESE LECT	OffMode mode Pull-Up/Down selection for pad kpd_row4 0x0: Offmode Pull-Down selected 0x1: Offmode Pull-Up selected	RW	0
28	KPD_ROW4_OFFMODE PULLUDENABLE	OffMode mode Pull-Up/Down enable for pad kpd _row4	RW	0

Bits	Field Name	Description	Type	Reset
		0x0: Offmode Pull-Up/Down disabled 0x1: Offmode Pull-Up/Down enabled		
27	KPD_ROW4_OFFMODE OUTVALUE	OffMode mode output value for pad kpd_row4 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	KPD_ROW4_OFFMODE OUTENABLE	OffMode mode output enable value for pad kpd _row4. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	KPD_ROW4_OFFMODE ENABLE	OffMode mode override control for pad kpd_row4 0x0: IO state keeps its previous state when OFF mode is active 0x1: IO state is forced to OFF mode value when O FF mode is active	RW	0
24	KPD_ROW4_INPUTENABLE	Input enable value for pad kpd_row4 0x0: Input buffere of I/O cell is disabled 0x1: Input buffere of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	KPD_ROW4_PULLTYPES-ELECT	pullup/down selection for pad kpd_row4 0x0: pulldown selected 0x1: pullup selected	RW	1
19	KPD_ROW4_PULLUDENABL E	pullup/down enable for pad kpd_row4 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	KPD_ROW4_MUXMODE	Functional multiplexing selection for pad kpd_row4 0x0: Selectkpd_row4 0x1: Select kpd_row1 0x2: Select cam2_d5 0x3: Selectgpio_176 0x7: Select safe_mode	RW	0x7
15	KPD_ROW3_WAKEUPE VENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	KPD_ROW3_WAKEUPE NABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	KPD_ROW3_OFFMODEPULLTYPESE LECT	Offmode mode Pull-Up/Down selection for pad kpd_row3 0x0: Offmode Pull-Down selected 0x1: Offmode Pull-Up selected	RW	0
12	KPD_ROW3_OFFMODE PULLUDENABLE	OffMode mode Pull-Up/Down enable for pad kpd _row3 0x0: Offmode Pull-Up/Down disabled 0x1: Offmode Pull-Up/Down enabled	RW	0
11	KPD_ROW3_OFFMODE OUTVALUE	OffMode mode output value for pad kpd_row3 0x0: Set value at 0	RW	0

Bits	Field Name	Description	Type	Reset
		0x1: Set value at 1		
10	KPD_ROW3_OFFMODE OUTENABLE	OffMode mode output enable value for pad kpd _row3. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	KPD_ROW3_OFFMODE ENABLE	OffMode mode override control for pad kpd_row3 0x0: IO state keeps its previous state when OFF mode is active 0x1: IO state is forced to OFF mode value when O FF mode is active	RW	0
8	KPD_ROW3_INPUTENABLE	Input enable value for pad kpd_row3 0x0: Input buffere of I/O cell is disabled 0x1: Input buffere of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	KPD_ROW3_PULLTYPES-ELECT	pullup/down selection for pad kpd_row3 0x0: pulldown selected 0x1: pullup selected	RW	1
3	KPD_ROW3_PULLUDENABL E	pullup/down enable for pad kpd_row3 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	KPD_ROW3_MUXMODE	Functional multiplexing selection for pad kpd_row3 0x0: Selectkpd_row3 0x1: Select kpd_row0 0x2: Select cam2_d4 0x3: Selectgpio_175 0x7: Select safe_mode	RW	0x7

Table 18.75. Register Call Summary for Register CONTROL_CORE_PAD0_KPD_ROW3_PAD1_KPD_ROW4

Control Module Functional Description
• PAD Functional Multiplexing and Configuration:[0]

Table 18.76. CONTROL_CORE_PAD0_KPD_ROW5_PAD1_KPD_ROW0

Address Offset	0x0000 018C		
Physical Address	SeeTable 18.49	**Instance**	SYSCTRL_PADCONF_ CORE
Description	Register control for Padskpd_row5andkpd_row0 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
KPD_ROW0_WAKEUPEVENT	KPD_ROW0_WAKEUPENABLE	RESERVED					KPD_ROW0_INPUTENABLE	RESERVED			KPD_ROW0_PULLTYPESELECT	KPD_ROW0_PULLUDENABLE	KPD_ROW0_MUXMODE			KPD_ROW5_WAKEUPEVENT	KPD_ROW5_WAKEUPENABLE	RESERVED				KPD_ROW5_INPUTENABLE	RESERVED			KPD_ROW5_PULLTYPESELECT	KPD_ROW5_PULLUDENABLE	KPD_ROW5_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	KPD_ROW0_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	KPD_ROW0_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	KPD_ROW0_OFFMODEPULLTYPESELECT	OffMode mode Pull-Up/Down selection for pad kpd_row0 0x0: Offmode Pull-Down selected 0x1: Offmode Pull-Up selected	RW	0
28	KPD_ROW0_OFFMODEPULLUDENABLE	OffMode mode Pull-Up/Down enable for pad kpd_row0 0x0: Offmode Pull-Up/Down disabled 0x1: Offmode Pull-Up/Down enabled	RW	0
27	KPD_ROW0_OFFMODEOUTVALUE	OffMode mode output value for pad kpd_row0 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	KPD_ROW0_OFFMODEOUTENABLE	OffMode mode output enable value for pad kpd_row0. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
25	KPD_ROW0_OFFMODEENABLE	OffMode mode override control for pad kpd_row0 0x0: IO state keeps its previous state when OFF mode is active 0x1: IO state is forced to OFF mode value when OFF mode is active	RW	0
24	KPD_ROW0_INPUTENABLE	Input enable value for pad kpd_row0 0x0: Input buffere of I/O cell is disabled 0x1: Input buffere of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	KPD_ROW0_PULLTYPES-ELECT	pullup/down selection for pad kpd_row0 0x0: pulldown selected 0x1: pullup selected	RW	1
19	KPD_ROW0_PULLUDENABLE	pullup/down enable for pad kpd_row0 0x0: pullup/down disabled	RW	1

Bits	Field Name	Description	Type	Reset
		0x1: pullup/down enabled		
18:16	KPD_ROW0_MUXMODE	Functional multiplexing selection for pad kpd_row0 0x0: Selectkpd_row0 0x1: Select kpd_row3 0x2: Select cam2_d7 0x3: Selectgpio_178 0x7: Select safe_mode	RW	0x7
15	KPD_ROW5_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	KPD_ROW5_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	KPD_ROW5_OFFMODEPULLTYPESELECT	OffMode mode Pull-Up/Down selection for pad kpd_row5 0x0: Offmode Pull-Down selected 0x1: Offmode Pull-Up selected	RW	0
12	KPD_ROW5_OFFMODEPULLUDENABLE	OffMode mode Pull-Up/Down enable for pad kpd_row5 0x0: Offmode Pull-Up/Down disabled 0x1: Offmode Pull-Up/Down enabled	RW	0
11	KPD_ROW5_OFFMODEOUTVALUE	OffMode mode output value for pad kpd_row5 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	KPD_ROW5_OFFMODEOUTENABLE	OffMode mode output enable value for pad kpd_row5. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	KPD_ROW5_OFFMODEENABLE	OffMode mode override control for pad kpd_row5 0x0: IO state keeps its previous state when OFF mode is active 0x1: IO state is forced to OFF mode value when OFF mode is active	RW	0
8	KPD_ROW5_INPUTENABLE	Input enable value for pad kpd_row5 0x0: Input buffer of I/O cell is disabled 0x1: Input buffer of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	KPD_ROW5_PULLTYPES-ELECT	pullup/down selection for pad kpd_row5 0x0: pulldown selected 0x1: pullup selected	RW	1
3	KPD_ROW5_PULLUDENABLE	pullup/down enable for pad kpd_row5 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	KPD_ROW5_MUXMODE	Functional multiplexing selection for pad kpd_row5 0x0: Selectkpd_row5	RW	0x7

Bits	Field Name	Description	Type	Reset
		0x1: Select kpd_row2 0x2: Select cam2_d6 0x3: Selectgpio_177 0x7: Select safe_mode		

Table 18.77. Register Call Summary for Register CONTROL_CORE_PAD0_KPD_ROW5_PAD1_KPD_ROW0

Control Module Functional Description

- PAD Functional Multiplexing and Configuration:[0]

Table 18.78. CONTROL_CORE_PAD0_KPD_ROW1_PAD1_KPD_ROW2

Address Offset	0x0000 0190		
Physical Address	See Table 18.49	**Instance**	SYSCTRL_PADCONF_CORE
Description	Register control for Padskpd_row1andkpd_row2 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
KPD_ROW2_WAKEUPEVENT	KPD_ROW2_WAKEUPENABLE	RESERVED					KPD_ROW2_INPUTENABLE	RESERVED			KPD_ROW2_PULLTYPESELECT	KPD_ROW2_PULLUDENABLE	KPD_ROW2_MUXMODE			KPD_ROW1_WAKEUPEVENT	KPD_ROW1_WAKEUPENABLE	RESERVED				KPD_ROW1_INPUTENABLE	RESERVED				KPD_ROW1_PULLTYPESELECT	KPD_ROW1_PULLUDENABLE	KPD_ROW1_MUXMODE	

Bits	Field Name	Description	Type	Reset
31	KPD_ROW2_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	KPD_ROW2_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29	KPD_ROW2_OFFMODEPULLTYPESELECT	OffMode mode Pull-Up/Down selection for pad kpd_row2 0x0: Offmode Pull-Down selected 0x1: Offmode Pull-Up selected	RW	0
28	KPD_ROW2_OFFMODEPULLUDENABLE	OffMode mode Pull-Up/Down enable for pad kpd_row2 0x0: Offmode Pull-Up/Down disabled 0x1: Offmode Pull-Up/Down enabled	RW	0
27	KPD_ROW2_OFFMODEOUTVALUE	OffMode mode output value for pad kpd_row2 0x0: Set value at 0 0x1: Set value at 1	RW	0
26	KPD_ROW2_OFFMODEOUTENABLE	OffMode mode output enable value for pad kpd_row2. This is an active low signal	RW	0

Bits	Field Name	Description	Type	Reset
		0x0: Output enable 0x1: Output disable		
25	KPD_ROW2_OFFMODE ENABLE	OffMode mode override control for pad kpd_row2 0x0: IO state keeps its previous state when OFF mode is active 0x1: IO state is forced to OFF mode value when O FF mode is active	RW	0
24	KPD_ROW2_INPUTENABLE	Input enable value for pad kpd_row2 0x0: Input buffere of I/O cell is disabled 0x1: Input buffere of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	KPD_ROW2_PULLTYPES- ELECT	pullup/down selection for pad kpd_row2 0x0: pulldown selected 0x1: pullup selected	RW	1
19	KPD_ROW2_PULLUDENABL E	pullup/down enable for pad kpd_row2 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	KPD_ROW2_MUXMODE	Functional multiplexing selection for pad kpd_row2 0x0: Selectkpd_row2 0x1: Select kpd_row5 0x2: Select cam2_d11 0x3: Selectgpio_3 0x7: Select safe_mode	RW	0x7
15	KPD_ROW1_WAKEUPE VENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	KPD_ROW1_WAKEUPE NABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	KPD_ROW1_OFFMODEPULLTYPESE LECT	OffMode mode Pull-Up/Down selection for pad kpd_row1 0x0: Offmode Pull-Down selected 0x1: Offmode Pull-Up selected	RW	0
12	KPD_ROW1_OFFMODE PULLUDENABLE	OffMode mode Pull-Up/Down enable for pad kpd _row1 0x0: Offmode Pull-Up/Down disabled 0x1: Offmode Pull-Up/Down enabled	RW	0
11	KPD_ROW1_OFFMODE OUTVALUE	OffMode mode output value for pad kpd_row1 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	KPD_ROW1_OFFMODE OUTENABLE	OffMode mode output enable value for pad kpd _row1. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0

Bits	Field Name	Description	Type	Reset
9	KPD_ROW1_OFFMODE ENABLE	OffMode mode override control for pad kpd_row1 0x0: IO state keeps its previous state when OFF mode is active 0x1: IO state is forced to OFF mode value when O FF mode is active	RW	0
8	KPD_ROW1_INPUTENABLE	Input enable value for pad kpd_row1 0x0: Input buffere of I/O cell is disabled 0x1: Input buffere of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	KPD_ROW1_PULLTYPES-ELECT	pullup/down selection for pad kpd_row1 0x0: pulldown selected 0x1: pullup selected	RW	1
3	KPD_ROW1_PULLUDENABL E	pullup/down enable for pad kpd_row1 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	KPD_ROW1_MUXMODE	Functional multiplexing selection for pad kpd_row1 0x0: Selectkpd_row1 0x1: Select kpd_row4 0x2: Select cam2_d9 0x3: Selectgpio_2 0x7: Select safe_mode	RW	0x7

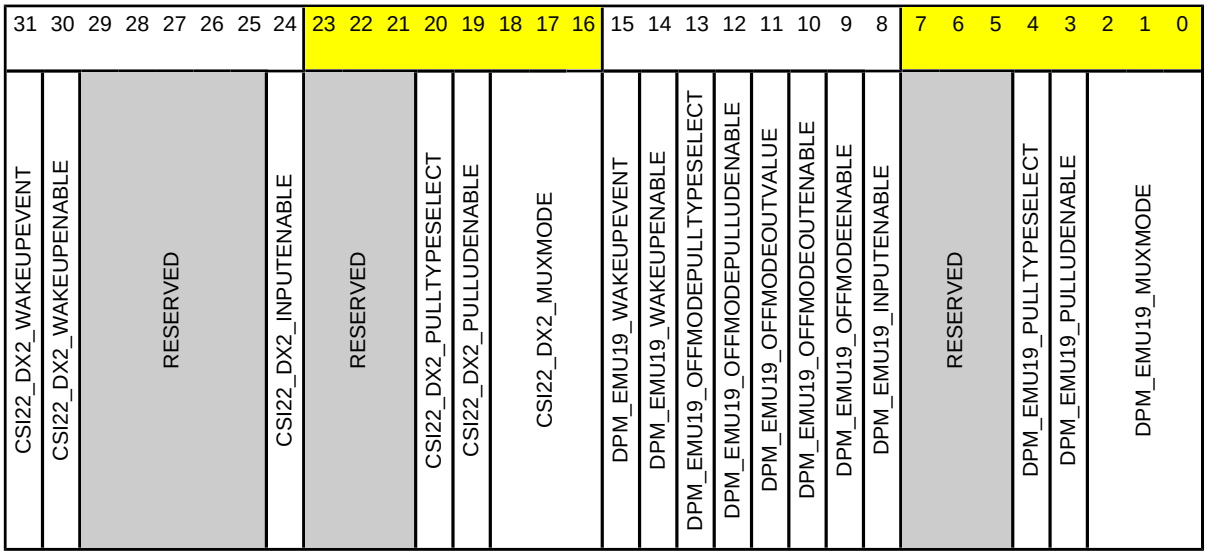
Table 18.79. Register Call Summary for Register CONTROL_CORE_PAD0_KPD_ROW1_PAD1_KPD_ROW2

Control Module Functional Description

- PAD Functional Multiplexing and Configuration:[0]

Table 18.80. CONTROL_CORE_PAD0_DPM_EMU19_PAD1_CSI22_DX2

Address Offset	0x0000 01D4		
Physical Address	SeeTable 18.49	**Instance**	SYSCTRL_PADCONF_ CORE
Description	Register control for Pad dpm_emu19and Pad csi22_dx2 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		



Bits	Field Name	Description	Type	Reset
~~31:16~~	~~RESERVED~~	-	~~R~~	~~0x00~~
31	CSI22_DX2_WAKE-UPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	CSI22_DX2_WAKE-UPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x00
24	CSI22_DX2_INPUTENABLE	Input enable value for pad csi22_dx2 0x0: Input buffere of IO cell is disabled 0x1: Input buffere of IO cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	CSI22_DX2_PULL-TYPESELECT	Pull-Up/Down selection for pad csi22_dx2 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
19	CSI22_DX2_PULLUDENAB LE	Pull-Up/Down enable for pad csi22_dx2 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
18:16	CSI22_DX2_MUXMODE	Functional multiplexing selection for pad csi22_dx2 0x0: Select csi22_dx2 0x2: Select cam2_fid 0x7: Select safe_mode	RW	0x7
15	DPM_EMU19_WAKE-UPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	DPM_EMU19_WAKE-UPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13	DPM_EMU19_ OFFMODEPULLTYPESELEC T	OffMode mode pullup/down selection for pad dpm_emu19 0x0: Offmode pulldown selected 0x1: Offmode pullup selected	RW	0

Bits	Field Name	Description	Type	Reset
12	DPM_EMU19_ OFFMODEPULLUDENABLE	OffMode mode pullup/down enable for pad dpm_ emu19 0x0: Offmode pullup/down disabled 0x1: Offmode pullup/down enabled	RW	0
11	DPM_EMU19_ OFFMODEOUTVALUE	OffMode mode output value for pad dpm_emu19 0x0: Set value at 0 0x1: Set value at 1	RW	0
10	DPM_EMU19_ OFFMODEOUTENABLE	OffMode mode output enable value for pad dpm _emu19. This is an active low signal 0x0: Output enable 0x1: Output disable	RW	0
9	DPM_EMU19_OFFMOD EENABLE	OffMode mode override control for pad dpm_em u19 0x0: I/O state keeps its previous state when OFF mode is active 0x1: I/O state is forced to OFF mode value when OFF mode is active	RW	0
8	DPM_EMU19_INPUTENABL E	Input enable value for pad dpm_emu19 0x0: Input buffere of I/O cell is disabled 0x1: Input buffere of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	DPM_EMU19_PULL-TYPESELECT	pullup/down selection for pad dpm_emu19 0x0: pulldown selected 0x1: pullup selected	RW	0
3	DPM_EMU19_PULLUDENAB LE	pullup/down enable for pad dpm_emu19 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	DPM_EMU19_MUXMODE	Functional multiplexing selection for pad dpm_emu19 0x0: Select dpm_emu19 0x1: Select dmtimer11_pwm_evt 0x2: Select dsi2_te1 0x3: Select gpio_191 0x4: Select rfbi_data0 0x5: Select dispc2_data0 0x6: Select hw_dbg19 0x7: Select safe_mode	RW	0x7

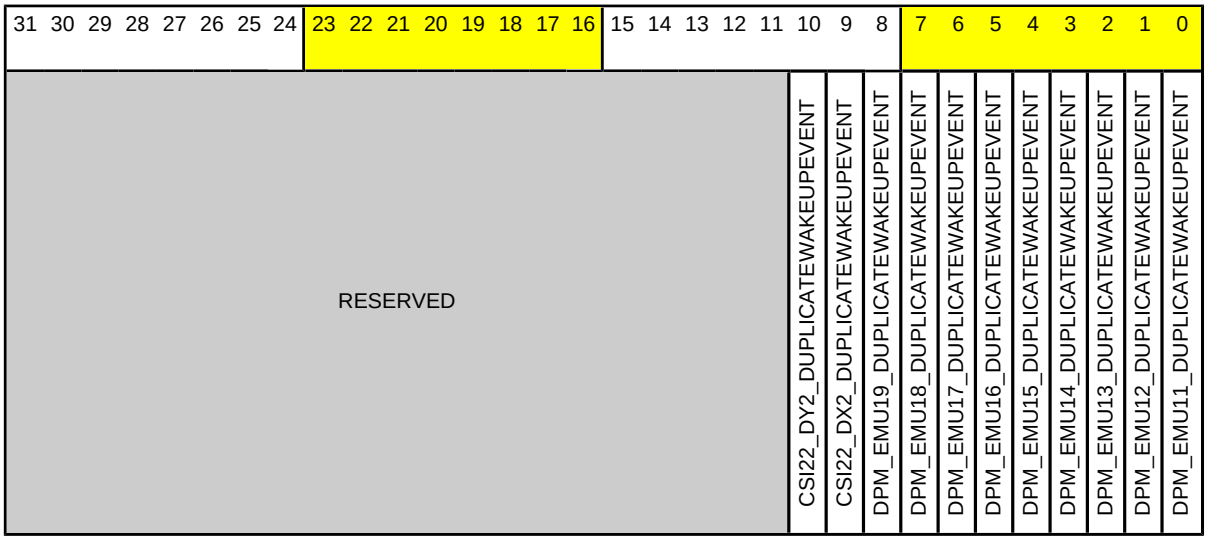
Table 18.81. Register Call Summary for Register CONTROL_CORE_PAD0_DPM_EMU19_PAD1_CSI22_DX2

Control Module Functional Description

- Device Core Control Module Instance:[0]

Table 18.82. CONTROL_PADCONF_WAKEUPEVENT_6

Address Offset	0x0000 01F0		
Physical Address	SeeTable 18.49	**Instance**	SYSCTRL_PADCONF_ CORE
Description	Access conditions. Read: unrestricted, Write: unrestricted		
Type	R		



Bits	Field Name	Description	Type	Reset
31:911	RESERVED		R	0x000000
10	CSI22_DY2_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad csi22_dy2 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
9	CSI22_DX2_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad csi22_dx2 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0
8	DPM_EMU19_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the IO for pad dpm_emu19 Read 0x1: A wakeup event occurred Read 0x0: No wakeup event occurred	R	0x000000
7	DPM_EMU18_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad dpm_emu18 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
6	DPM_EMU17_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad dpm_emu17 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
5	DPM_EMU16_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad dpm_emu16 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
4	DPM_EMU15_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad dpm_emu15 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
3	DPM_EMU14_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad dpm_emu14 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
2	DPM_EMU13_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad dpm_emu13 Read 0x0: No wake-up event occurred	R	0

Bits	Field Name	Description	Type	Reset
		Read 0x1: A wake-up event occurred		
1	DPM_EMU12_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad dpm_emu12 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
0	DPM_EMU11_DUPLICATEWAKEUPEVENT	Wake-up event status latched in the I/O for pad dpm_emu11 Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0

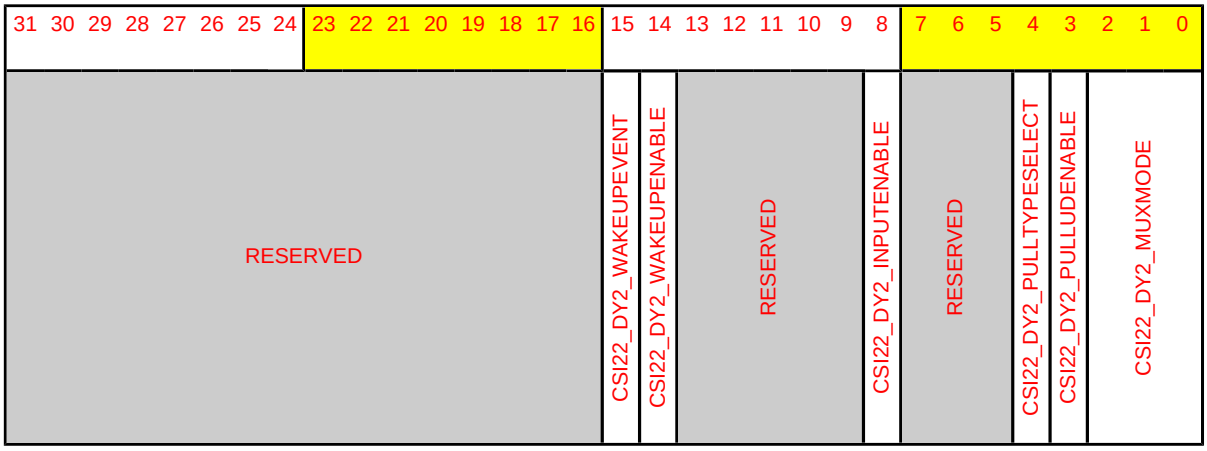
Table 18.83. Register Call Summary for Register CONTROL_PADCONF_WAKEUPEVENT_6

Control Module Functional Description

- PAD Functional Multiplexing and Configuration:[0]

Table 18.84. CONTROL_CORE_PAD0_CSI22_DY2

Address Offset	0x0000 01F4		
Physical Address	Please refer toTable 18.49	**Instance**	OMAP4460_CONTROL_CORE
Description	Register control for Pad csi22_dy2 Access conditions. Read: unrestricted, Write: pi_padconfaccdisable = '0' OR (pi_mreqsecure = '1' AND pi_mreqsupervisor = '1')		
Type	RW		



Bits	Field Name	Description	Type	Reset
31:16	RESERVED		R	0x0000
15	CSI22_DY2_WAKE-UPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	CSI22_DY2_WAKE-UPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x00
8	CSI22_DY2_INPUTENABLE	Input enable value for pad csi22_dy2 0x0: Input buffere of IO cell is disabled 0x1: Input buffere of IO cell is enabled	RW	1

Bits	Field Name	Description	Type	Reset
7:5	RESERVED		R	0x0
4	CSI22_DY2_PULL-TYPESELECT	Pull-Up/Down selection for pad csi22_dy2 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	CSI22_DY2_PULLUDENABLE	Pull-Up/Down enable for pad csi22_dy2 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	CSI22_DY2_MUXMODE	Functional multiplexing selection for pad csi22_dy2 0x0: Select csi22_dy2 0x2: Select cam2_wen 0x7: Select safe_mode	RW	0x7

Table 18.85. Register Call Summary for Register CONTROL_CORE_PAD0_CSI22_DY2

Control Module Functional Description

- Device Core Control Module Instance:[0]

Table 18.86. CONTROL_I2C_0

Address Offset	0x0000 0604		
Physical Address	SeeTable 18.49	**Instance**	SYSCTRL_PADCONF_CORE
Description	I2C pads control 0 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I2C4_SDA_GLFENB	I2C4_SDA_LOAD_BITS		I2C4_SDA_PULLUPRESX	I2C3_SDA_GLFENB	I2C3_SDA_LOAD_BITS		I2C3_SDA_PULLUPRESX	I2C2_SDA_GLFENB	I2C2_SDA_LOAD_BITS		I2C2_SDA_PULLUPRESX	I2C1_SDA_GLFENB	I2C1_SDA_LOAD_BITS		I2C1_SDA_PULLUPRESX	I2C4_SCL_GLFENB	I2C4_SCL_LOAD_BITS		I2C4_SCL_PULLUPRESX	I2C3_SCL_GLFENB	I2C3_SCL_LOAD_BITS		I2C3_SCL_PULLUPRESX	I2C2_SCL_GLFENB	I2C2_SCL_LOAD_BITS		I2C2_SCL_PULLUPRESX	I2C1_SCL_GLFENB	I2C1_SCL_LOAD_BITS		I2C1_SCL_PULLUPRESX

Bits	Field Name	Description	Type	Reset
31	I2C4_SDA_GLFENB	Active_high glitch free operation enable pin for i2c4 receiver 0x0: Disable i2c4 glitch free operation 0x1: Enable i2c4 glitch free operation	RW	0
30:29	I2C4_SDA_LOAD_BITS	Internal Pull up resistor in Fast or Standard mode / High_speed mode for i2c4 0x0: 4.5 kOhm (5-15 pF) / 1.66 kOhm (5-12 pF) 0x1: 2.1 kOhm (15-50 pF) / 920 Ohm (12-25 pF) 0x2: 860 Ohm (50-150 pF) / 500 Ohm (25-50 pF) 0x3: N.A / 300 Ohm (50-80 pF)	RW	0x1
28	I2C4_SDA_PULLUPRESX	Active_low internal pull_up resistor enabled for i2c4 0x0: Enable Internal Pull up resistor 0x1: Disable Internal Pull up resisitor	RW	0
27	I2C3_SDA_GLFENB	Active_high glitch free operation enable pin for i2c3 receiver	RW	0

Bits	Field Name	Description	Type	Reset
		0x0: Disable i2c4 glitch free operation 0x1: Enable i2c4 glitch free operation		
26:25	I2C3_SDA_LOAD_BITS	Internal Pull up resistor in Fast or Standard mode / High_speed mode for i2c3 0x0: 4.5 kOhm (5-15 pF) / 1.66 kOhm (5-12 pF) 0x1: 2.1 kOhm (15-50 pF) / 920 Ohm (12-25 pF) 0x2: 860 Ohm (50-150 pF) / 500 Ohm (25-50 pF) 0x3: N.A / 300 Ohm (50-80 pF)	RW	0x1
24	I2C3_SDA_PULLUPRESX	Active_low internal pull_up resistor enabled for i2c3 0x0: Enable Internal Pull up resistor 0x1: Disable Internal Pull up resisitor	RW	0
23	I2C2_SDA_GLFENB	Active_high glitch free operation enable pin for i2c2 receiver 0x0: Disable i2c4 glitch free operation 0x1: Enable i2c4 glitch free operation	RW	0
22:21	I2C2_SDA_LOAD_BITS	Internal Pull up resistor in Fast or Standard mode / High_speed mode for i2c2 0x0: 4.5 kOhm (5-15 pF) / 1.66 kOhm (5-12 pF) 0x1: 2.1 kOhm (15-50 pF) / 920 Ohm (12-25 pF) 0x2: 860 Ohm (50-150 pF) / 500 Ohm (25-50 pF) 0x3: N.A / 300 Ohm (50-80 pF)	RW	0x1
20	I2C2_SDA_PULLUPRESX	Active_low internal pull_up resistor enabled for i2c2 0x0: Enable Internal Pull up resistor 0x1: Disable Internal Pull up resisitor	RW	0
19	I2C1_SDA_GLFENB	Active_high glitch free operation enable pin for i2c1 receiver 0x0: Disable i2c4 glitch free operation 0x1: Enable i2c4 glitch free operation	RW	0
18:17	I2C1_SDA_LOAD_BITS	Internal Pull up resistor in Fast or Standard mode / High_speed mode for i2c1 0x0: 4.5 kOhm (5-15 pF) / 1.66 kOhm (5-12 pF) 0x1: 2.1 kOhm (15-50 pF) / 920 Ohm (12-25 pF) 0x2: 860 Ohm (50-150 pF) / 500 Ohm (25-50 pF) 0x3: N.A / 300 Ohm (50-80 pF)	RW	~~0x1~~0x2
16	I2C1_SDA_PULLUPRESX	Active_low internal pull_up resistor enabled for i2c1 0x0: Enable Internal Pull up resistor 0x1: Disable Internal Pull up resisitor	RW	0
15	I2C4_SCL_GLFENB	Active_high glitch free operation enable pin for i2c4 receiver 0x0: Disable i2c4 glitch free operation 0x1: Enable i2c4 glitch free operation	RW	0
14:13	I2C4_SCL_LOAD_BITS	Internal Pull up resistor in Fast or Standard mode / High_speed mode for i2c4 0x0: 4.5 kOhm (5-15 pF) / 1.66 kOhm (5-12 pF) 0x1: 2.1 kOhm (15-50 pF) / 920 Ohm (12-25 pF) 0x2: 860 Ohm (50-150 pF) / 500 Ohm (25-50 pF) 0x3: N.A / 300 Ohm (50-80 pF)	RW	0x1
12	I2C4_SCL_PULLUPRESX	Active_low internal pull_up resistor enabled for i2c4 0x0: Enable Internal Pull up resistor 0x1: Disable Internal Pull up resisitor	RW	0

Bits	Field Name	Description	Type	Reset
11	I2C3_SCL_GLFENB	Active_high glitch free operation enable pin for i2c3 receiver 0x0: Disable i2c4 glitch free operation 0x1: Enable i2c4 glitch free operation	RW	0
10:9	I2C3_SCL_LOAD_BITS	Internal Pull up resistor in Fast or Standard mode / High_speed mode for i2c3 0x0: 4.5 kOhm (5-15 pF) / 1.66 kOhm (5-12 pF) 0x1: 2.1 kOhm (15-50 pF) / 920 Ohm (12-25 pF) 0x2: 860 Ohm (50-150 pF) / 500 Ohm (25-50 pF) 0x3: N.A / 300 Ohm (50-80 pF)	RW	0x1
8	I2C3_SCL_PULLUPRESX	Active_low internal pull_up resistor enabled for i2c3 0x0: Enable Internal Pull up resistor 0x1: Disable Internal Pull up resisitor	RW	0
7	I2C2_SCL_GLFENB	Active_high glitch free operation enable pin for i2c2 receiver 0x0: Disable i2c4 glitch free operation 0x1: Enable i2c4 glitch free operation	RW	0
6:5	I2C2_SCL_LOAD_BITS	Internal Pull up resistor in Fast or Standard mode / High_speed mode for i2c2 0x0: 4.5 kOhm (5-15 pF) / 1.66 kOhm (5-12 pF) 0x1: 2.1 kOhm (15-50 pF) / 920 Ohm (12-25 pF) 0x2: 860 Ohm (50-150 pF) / 500 Ohm (25-50 pF) 0x3: N.A / 300 Ohm (50-80 pF)	RW	0x1
4	I2C2_SCL_PULLUPRESX	Active_low internal pull_up resistor enabled for i2c2 0x0: Enable Internal Pull up resistor 0x1: Disable Internal Pull up resisitor	RW	0
3	I2C1_SCL_GLFENB	Active_high glitch free operation enable pin for i2c1 receiver 0x0: Disable i2c4 glitch free operation 0x1: Enable i2c4 glitch free operation	RW	0
2:1	I2C1_SCL_LOAD_BITS	Internal Pull up resistor in Fast or Standard mode / High_speed mode for i2c1 0x0: 4.5 kOhm (5-15 pF) / 1.66 kOhm (5-12 pF) 0x1: 2.1 kOhm (15-50 pF) / 920 Ohm (12-25 pF) 0x2: 860 Ohm (50-150 pF) / 500 Ohm (25-50 pF) 0x3: N.A / 300 Ohm (50-80 pF)	RW	~~0x1~~0x2
0	I2C1_SCL_PULLUPRESX	Active_low internal pull_up resistor enabled for i2c1 0x0: Enable Internal Pull up resistor 0x1: Disable Internal Pull up resisitor	RW	0

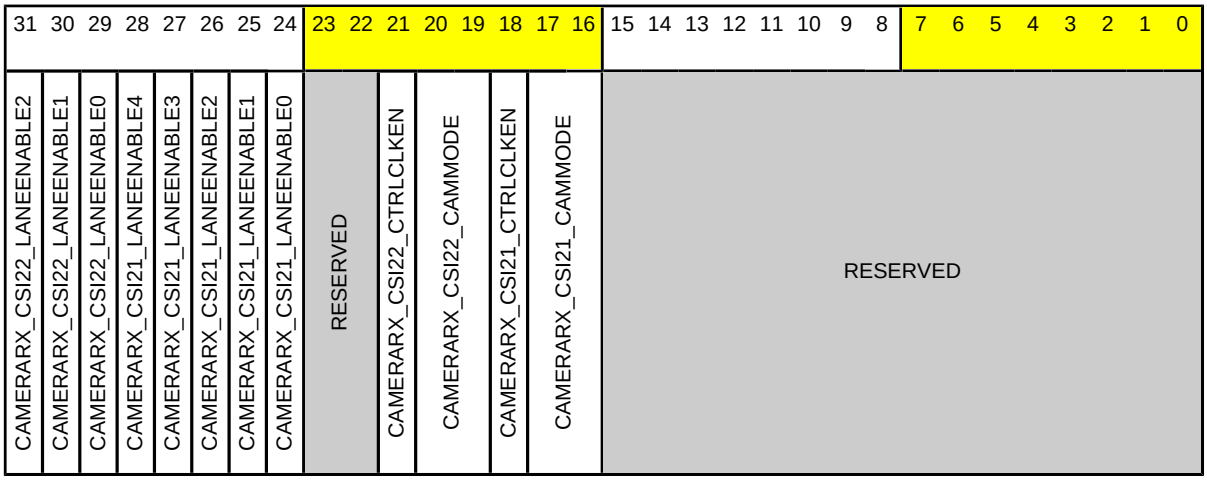
Table 18.87. Register Call Summary for Register CONTROL_I2C_0

Control Module Functional Description

- PAD Functional Multiplexing and Configuration:[0]

Table 18.88. CONTROL_CAMERA_RX

Address Offset	0x0000 0608		
Physical Address	SeeTable 18.49	**Instance**	SYSCTRL_PADCONF_CORE
Description	CAMERA RX control Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		



Bits	Field Name	Description	Type	Reset
31	~~RESERVED~~ CAMERARX_CSI22_LANEENABLE2	CSI22 CAMERARX Lane 2 Enable (CSI22_DX2, CSI22_DY2) 0x0: Lane module disabled 0x1: Lane module enabled	~~R~~RW	0
30	CAMERARX_CSI22_LANEENABLE1	CSI22 CAMERARX Lane 1 Enable (CSI22_DX1, CSI22_DY1) 0x0: Lane module disabled 0x1: Lane module enabled	RW	0x0
29	CAMERARX_CSI22_LANEENABLE0	CSI22 CAMERARX Lane 0 Enable (CSI22_DX0, CSI22_DY0) 0x0: Lane module disabled 0x1: Lane module enabled	RW	0x0
28	CAMERARX_CSI21_LANEENABLE4	CSI21 CAMERARX Lane 4 Enable (CSI21_DX4, CSI21_DY4) 0x0: Lane module disabled 0x1: Lane module enabled	RW	0x00
27	CAMERARX_CSI21_LANEENABLE3	CSI21 CAMERARX Lane 3 Enable (CSI21_DX3, CSI21_DY3) 0x0: Lane module disabled 0x1: Lane module enabled	RW	0x00
26	CAMERARX_CSI21_LANEENABLE2	CSI21 CAMERARX Lane 2 Enable (CSI21_DX2, CSI21_DY2) 0x0: Lane module disabled 0x1: Lane module enabled	RW	0x00
25	CAMERARX_CSI21_LANEENABLE1	CSI21 CAMERARX Lane 1 Enable (CSI21_DX1, CSI21_DY1) 0x0: Lane module disabled 0x1: Lane module enabled	RW	0x00
24	CAMERARX_CSI21_LANEENABLE0	CSI21 CAMERARX Lane 0 Enable (CSI21_DX0, CSI21_DY0) 0x0: Lane module disabled 0x1: Lane module enabled	RW	0x00
23:22	RESERVED		R	0x0
21	CAMERARX_CSI22_CTRLCLKEN	CSI22 CAMERARX clock enable control 0x0: Disable for CTRLCLK 0x1: Active high enable for CTRLCLK	RW	0
20:19		CSI22 CAMERARX CAMMODE control	RW	0x3

Bits	Field Name	Description	Type	Reset
	CAMERARX_CSI22_CAM-MODE	0x0: DPHY mode (CSI2 mode) 0x1: Data/Strobe Transmission Format (CCP2 mode) 0x2: Data/Clock Transmission Format (CCP2/CSI1 mode) 0x3:~~Reserved~~GPI mode (Parallel Interface mode)		
18	CAMERARX_CSI21_CTRLCLKEN	CSI21 CAMERARX clock enable control 0x0: Disable for CTRLCLK 0x1: Active high enable for CTRLCLK	RW	0
17:16	CAMERARX_CSI21_CAM-MODE	CSI21 CAMERARX CAMMODE control 0x0: DPHY mode (CSI2 mode) 0x1: Data/Strobe Transmission Format (CCP2 mode) 0x2: Data/Clock Transmission Format (CCP2/CSI1 mode) 0x3:~~Reserved~~GPI mode (Parallel Interface mode)	RW	0x3
15:0	RESERVED		R	0x0000

Table 18.89. Register Call Summary for Register CONTROL_CAMERA_RX

Control Module Functional Description

- PAD Functional Multiplexing and Configuration:[0]

18.6.8. SYSCTRL_PADCONF_WKUP Register Summary

Table 18.90. SYSCTRL_PADCONF_WKUP Register Mapping Summary

Register Name	Type	Register Width (Bits)	Address Offset	SYSCTRL_PADCONF_WKUP Physical Address
CONTROL_PADCONF_WKUP_REVISION	R	32	0x0000 0000	0x4A31 E000
CONTROL_PADCONF_WKUP_HWINFO	R	32	0x0000 0004	0x4A31 E004
CONTROL_PADCONF_WKUP_SYSCONFIG	RW	32	0x0000 0010	0x4A31 E010
CONTROL_WKUP_PAD0_GPIO_WK0_PAD1_GPIO_WK1	RW	32	0x0000 0040	0x4A31 E040
CONTROL_WKUP_PAD0_GPIO_WK2_PAD1_GPIO_WK3	RW	32	0x0000 0044	0x4A31 E044
CONTROL_WKUP_PAD0_GPIO_WK4_PAD1_SR_SCL	RW	32	0x0000 0048	0x4A31 E048
CONTROL_WKUP_PAD0_SR_SDA_PAD1_FREF_XTAL_IN	RW	32	0x0000 004C	0x4A31 E04C
CONTROL_WKUP_PAD0_FREF_SLICER_IN_PAD1_FREF_CLK_IOREQ	RW	32	0x0000 0050	0x4A31 E050
CONTROL_WKUP_PAD0_FREF_CLK0_OUT_PAD1_FREF_CLK3_REQ	RW	32	0x0000 0054	0x4A31 E054

Register Name	Type	Register Width (Bits)	Address Offset	SYSCTRL_PADCONF_WKUP Physical Address
CONTROL_WKUP_PAD0_FREF_CLK3_OUT_PAD1_FREF_CLK4_REQ	RW	32	0x0000 0058	0x4A31 E058
CONTROL_WKUP_PAD0_FREF_CLK4_OUT_PAD1_SYS_32K	RW	32	0x0000 005C	0x4A31 E05C
CONTROL_WKUP_PAD0_SYS_NRESPWRON_PAD1_SYS_NRESWARM	RW	32	0x0000 0060	0x4A31 E060
CONTROL_WKUP_PAD0_SYS_PWR_REQ_PAD1_SYS_PWRON_RESET_OUT	RW	32	0x0000 0064	0x4A31 E064
CONTROL_WKUP_PAD0_SYS_BOOT6_PAD1_SYS_BOOT7	RW	32	0x0000 0068	0x4A31 E068
CONTROL_WKUP_PAD0_JTAG_NTRST_PAD1_JTAG_TCK	RW	32	0x0000 006C	0x4A31 E06C
CONTROL_WKUP_PAD0_JTAG_RTCK_PAD1_JTAG_TMS_TMSC	RW	32	0x0000 0070	0x4A31 E070
CONTROL_WKUP_PAD0_JTAG_TDI_PAD1_JTAG_TDO	RW	32	0x0000 0074	0x4A31 E074
CONTROL_WKUP_PADCONF_WAKEUPEVENT_0	R	32	0x0000 007C	0x4A31 E07C
CONTROL_SMART1NOPMIO_PADCONF_0	RW	32	0x0000 05A0	0x4A31 E5A0
CONTROL_SMART1NOPMIO_PADCONF_1	RW	32	0x0000 05A4	0x4A31 E5A4
CONTROL_WKUP_PADCONF_MODE	RW	32	0x0000 05A8	0x4A31 E5A8
CONTROL_XTAL_OSCILLATOR	RW	32	0x0000 05AC	0x4A31 E5AC
CONTROL_SMART3NOPMIO_PADCONF_0	RW	32	0x0000 05B0	0x4A31 E5B0
CONTROL_SMART3NOPMIO_PADCONF_1	RW	32	0x0000 05B4	0x4A31 E5B4
CONTROL_GPIOWK	RW	32	0x0000 0600	0x4A31 E600
CONTROL_I2C_2	RW	32	0x0000 0604	0x4A31 E604
CONTROL_JTAG	RW	32	0x0000 0608	0x4A31 E608
CONTROL_SYS	RW	32	0x0000 060C	0x4A31 E60C
CONTROL_WKUP_CONTROL_SPARE_RW	RW	32	0x0000 0614	0x4A31 E614
CONTROL_WKUP_CONTROL_SPARE_R	R	32	0x0000 0618	0x4A31 E618
CONTROL_WKUP_CONTROL_SPARE_R_C0	RW	32	0x0000 061C	0x4A31 E61C

Register Name	Type	Register Width (Bits)	Address Offset	SYSCTRL_PADCONF_WKUP Physical Address
CONTROL_WKUP_CONTROL_SPARE_RW1	RW	32	0x0000 0620	0x4A31 E620
CONTROL_WKUP_CONTROL_SPARE_RW2	RW	32	0x0000 0624	0x4A31 E624
CONTROL_WKUP_CONTROL_SPARE_RW3	RW	32	0x0000 0628	0x4A31 E628
CONTROL_WKUP_CONTROL_SPARE_RW4	RW	32	0x0000 062C	0x4A31 E62C
CONTROL_WKUP_CONTROL_SPARE_RW5	RW	32	0x0000 0630	0x4A31 E630
CONTROL_WKUP_CONTROL_SPARE_RW6	RW	32	0x0000 0634	0x4A31 E634
CONTROL_WKUP_CONTROL_SPARE_RW7	RW	32	0x0000 0638	0x4A31 E638
CONTROL_WKUP_CONTROL_SPARE_RW8	RW	32	0x0000 063C	0x4A31 E63C
CONTROL_WKUP_CONTROL_SPARE_RW9	RW	32	0x0000 0640	0x4A31 E640
CONTROL_WKUP_CONTROL_SPARE_R1	R	32	0x0000 064C	0x4A31 E64C

18.6.9. SYSCTRL_PADCONF_WKUP Register Summary

Note

This section contains only modified registers.

Table 18.91. CONTROL_WKUP_PAD0_GPIO_WK0_PAD1_GPIO_WK1

Address Offset	0x0000 0040		
Physical Address	See Table 18.90	**Instance**	SYSCTRL_PADCONF_WKUP
Description	Register control for Pads gpio_wk0 and gpio_wk1 Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPIO_WK1_WAKEUPEVENT	GPIO_WK1_WAKEUPENABLE	RESERVED					GPIO_WK1_INPUTENABLE	RESERVED			GPIO_WK1_PULLTYPESELECT	GPIO_WK1_PULLUDENABLE	GPIO_WK1_MUXMODE			GPIO_WK0_WAKEUPEVENT	GPIO_WK0_WAKEUPENABLE	RESERVED					GPIO_WK0_INPUTENABLE	RESERVED			GPIO_WK0_PULLTYPESELECT	GPIO_WK0_PULLUDENABLE	GPIO_WK0_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	GPIO_WK1_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	GPIO_WK1_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x00
24	GPIO_WK1_INPUTENABLE	Input enable value for pad gpio_wk1 0x0: Input buffere of I/O cell is disabled 0x1: Input buffere of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	GPIO_WK1_PULLTYPES-ELECT	pullup/down selection for pad gpio_wk1 0x0: pulldown selected 0x1: pullup selected	RW	0
19	GPIO_WK1_PULLUDENABLE	pullup/down enable for pad gpio_wk1 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	GPIO_WK1_MUXMODE	Functional multiplexing selection for pad gpio_wk1 0x0: Reserved 0x3: Select gpio_wk1 0x6: Select hw_dbg2 0x7: Select safe_mode	RW	0x7
15	GPIO_WK0_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	GPIO_WK0_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x00
8	GPIO_WK0_INPUTENABLE	Input enable value for pad gpio_wk0 0x0: Input buffere of I/O cell is disabled 0x1: Input buffere of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	GPIO_WK0_PULLTYPES-ELECT	pullup/down selection for pad gpio_wk0	RW	0

Bits	Field Name	Description	Type	Reset
		0x0: pulldown selected 0x1: pullup selected		
3	GPIO_WK0_PULLUDENABLE	pullup/down enable for pad gpio_wk0 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	GPIO_WK0_MUXMODE	Functional multiplexing selection for pad gpio_wk0 0x0: Reserved 0x3: Select gpio_wk0 0x4: Select c2c_pwkup 0x6: Select hw_dbg1 0x7: Select safe_mode	RW	0x7

Table 18.92. Register Call Summary for Register CONTROL_WKUP_PAD0_GPIO_WK0_PAD1_GPIO_WK1

Control Module Functional Description

- PAD Functional Multiplexing and Configuration:[0]

Table 18.93. CONTROL_WKUP_PAD0_GPIO_WK4_PAD1_SR_SCL

Address Offset	0x0000 0048		
Physical Address	Please refer toTable 18.90	**Instance**	SYSCTRL_PADCONF_WKUP
Description	Register control for Pads gpio_wk4 and sr_scl Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SR_SCL_WAKEUPEVENT	SR_SCL_WAKEUPENABLE	RESERVED					SR_SCL_INPUTENABLE	RESERVED			SR_SCL_PULLTYPESELECT	SR_SCL_PULLUDENABLE	RESERVED			GPIO_WK4_WAKEUPEVENT	GPIO_WK4_WAKEUPENABLE	RESERVED				GPIO_WK4_INPUTENABLE	RESERVED				GPIO_WK4_PULLTYPESELECT	GPIO_WK4_PULLUDENABLE	GPIO_WK4_MUXMODE		

Bits	Field Name	Description	Type	Reset
31	SR_SCL_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
30	SR_SCL_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection on low level 0x1: wake-up detection on high level	RW	0
29:25	RESERVED		R	0x00
24	SR_SCL_INPUTENABLE	Input enable value for pad sr_scl 0x0: Input buffere of IO cell is disabled	RW	1

Bits	Field Name	Description	Type	Reset
		0x1: Input buffere of IO cell is enabled		
23:21	RESERVED		R	0x0
20	SR_SCL_PULLTYPESELECT	Pull-Up/Down selection for pad sr_scl 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	~~1~~0
19	SR_SCL_PULLUDENABLE	Pull-Up/Down enable for pad sr_scl 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	~~1~~0
18:16	RESERVED		R	0x0
15	GPIO_WK4_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	GPIO_WK4_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection on low level 0x1: wake-up detection on high level	RW	0
13:9	RESERVED		R	0x00
8	GPIO_WK4_INPUTENABLE	Input enable value for pad gpio_wk4 0x0: Input buffere of IO cell is disabled 0x1: Input buffere of IO cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	GPIO_WK4_PULLTYPES-ELECT	Pull-Up/Down selection for pad gpio_wk4 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	0
3	GPIO_WK4_PULLUDENABLE	Pull-Up/Down enable for pad gpio_wk4 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	1
2:0	GPIO_WK4_MUXMODE	Functional multiplexing selection for pad gpio_wk4 0x0: Reserved 0x3: Select gpio_wk4 0x6: Select hw_dbg5 0x7: Select safe_mode	RW	0x7

Table 18.94. Register Call Summary for Register CONTROL_WKUP_PAD0_GPIO_WK4_PAD1_SR_SCL

Control Module Functional Description

- PAD Functional Multiplexing and Configuration:[0][1]

Table 18.95. CONTROL_WKUP_PAD0_SR_SDA_PAD1_FREF_XTAL_IN

Address Offset	0x0000 004C		
Physical Address	Please refer toTable 18.90	**Instance**	SYSCTRL_PADCONF_WKUP
Description	Register control for Pads sr_sda and fref_xtal_in Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								FREF_XTAL_IN_MUXMODE								SR_SDA_WAKEUPEVENT	SR_SDA_WAKEUPENABLE	RESERVED						SR_SDA_INPUTENABLE	RESERVED				SR_SDA_PULLTYPESELECT	SR_SDA_PULLUDENABLE	RESERVED		

Bits	Field Name	Description	Type	Reset
31:19	RESERVED		R	0x0000
18:16	FREF_XTAL_IN_MUXMODE	Functional multiplexing selection for pad fref_xtal_in 0x0: Select fref_xtal_in 0x4: Select c2c_wakereqin	RW	0x0
15	SR_SDA_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x1: A wake-up event occurred Read 0x0: No wake-up event occurred	R	0
14	SR_SDA_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection on low level 0x1: wake-up detection on high level	RW	0
13:9	RESERVED		R	0x00
8	SR_SDA_INPUTENABLE	Input enable value for pad sr_sda 0x0: Input buffere of IO cell is disabled 0x1: Input buffere of IO cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	SR_SDA_PULLTYPESELECT	Pull-Up/Down selection for pad sr_sda 0x0: Pull-Down selected 0x1: Pull-Up selected	RW	~~1~~0
3	SR_SDA_PULLUDENABLE	Pull-Up/Down enable for pad sr_sda 0x0: Pull-Up/Down disabled 0x1: Pull-Up/Down enabled	RW	~~1~~0
2:0	RESERVED		R	0x0

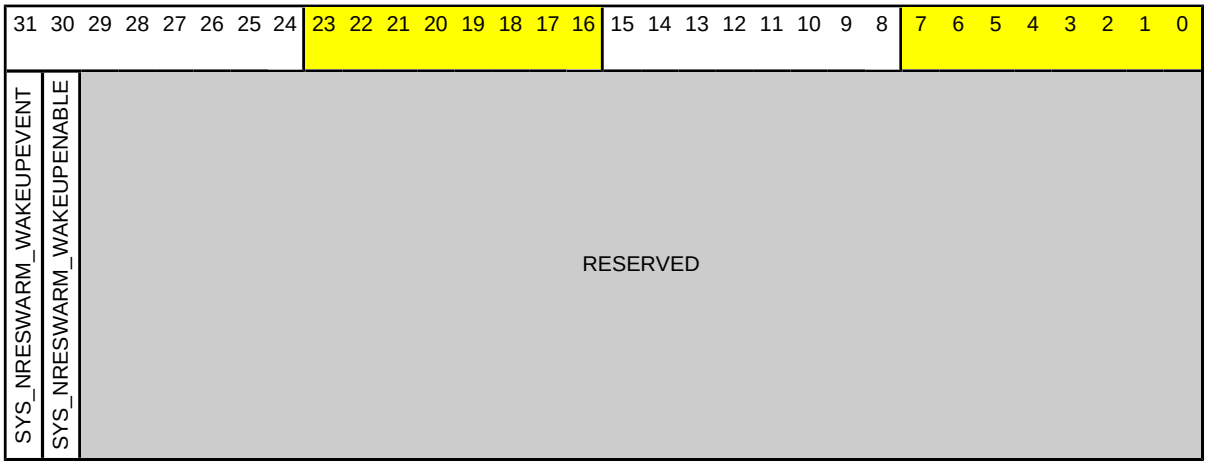
Table 18.96. Register Call Summary for Register CONTROL_WKUP_PAD0_SR_SDA_PAD1_FREF_XTAL_IN

Control Module Functional Description

- PAD Functional Multiplexing and Configuration:[0][1]

Table 18.97. CONTROL_WKUP_PAD0_SYS_NRESPWRON_PAD1_SYS_NRESWARM

Address Offset	0x0000 0060		
Physical Address	SeeTable 18.49	**Instance**	SYSCTRL_PADCONF_WKUP
Description	Register control for Pads~~sys_nrespwron and~~sys_nreswarm Access conditions. Read: unrestricted, Write: unrestricted		
Type	RW		



Bits	Field Name	Description	Type	Reset
31	SYS_NRESWARM_WAKEUPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	SYS_NRESWARM_WAKEUPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:50	RESERVED		R	0x0000000
~~4~~	~~SYS_NRESPWRON_PULLTYPESELECT~~	~~pullup/down selection for pad sys_nrespwron~~ ~~0x0: pulldown selected~~ ~~0x1: pullup selected~~	~~RW~~	~~0~~
~~3~~	~~SYS_NRESPWRON_PULLUDENABLE~~	~~pullup/down enable for pad sys_nrespwron~~ ~~0x0: pullup/down disabled~~ ~~0x1: pullup/down enabled~~	~~RW~~	~~0~~
~~2:0~~	~~RESERVED~~	-	~~R~~	~~0x0~~

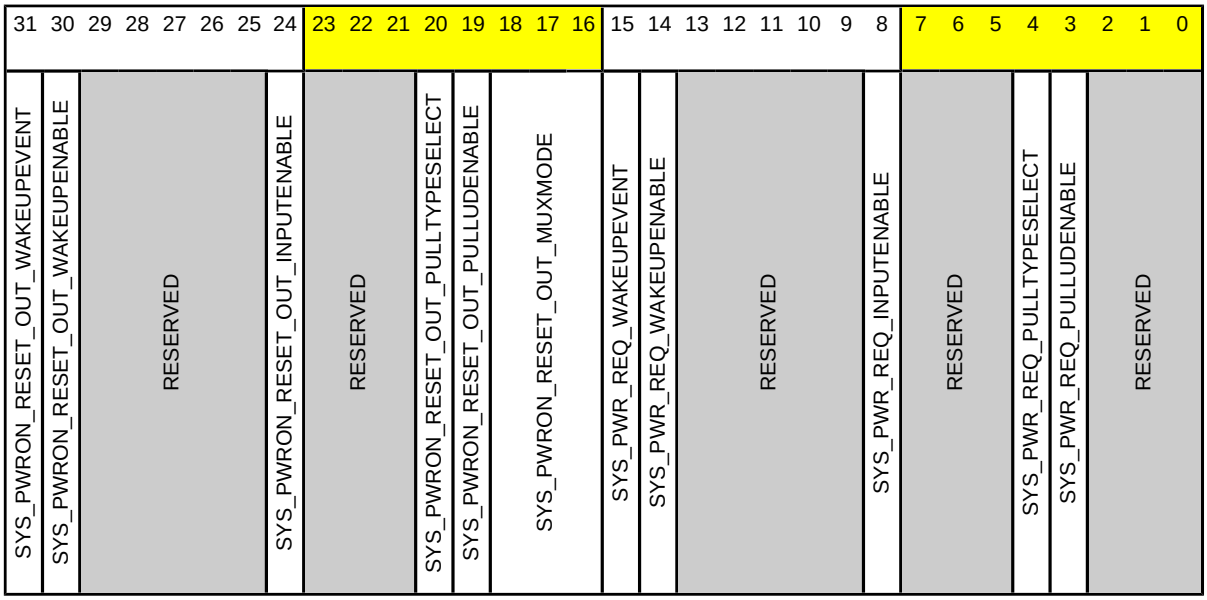
Table 18.98. Register Call Summary for Register CONTROL_WKUP_PAD0_SYS_NRESPWRON_PAD1_SYS_NRESWARM

Control Module Functional Description

- PAD Functional Multiplexing and Configuration:[0]

Table 18.99. CONTROL_WKUP_PAD0_SYS_PWR_REQ_PAD1_SYS_PWRON_RESET_OUT

Address Offset	0x0000 0064		
Physical Address	SeeTable 18.90	**Instance**	SYSCTRL_PADCONF_WKUP
Description	Register control for Pads sys_pwr_req and sys_pwron_reset_out Access conditions. Read: unrestricted, Write: pi_padconfaccdisable = 0		
Type	RW		



31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SYS_PWRON_RESET_OUT_WAKEUPEVENT	SYS_PWRON_RESET_OUT_WAKEUPENABLE	RESERVED					SYS_PWRON_RESET_OUT_INPUTENABLE	RESERVED			SYS_PWRON_RESET_OUT_PULLTYPESELECT	SYS_PWRON_RESET_OUT_PULLUDENABLE	SYS_PWRON_RESET_OUT_MUXMODE			SYS_PWR_REQ_WAKEUPEVENT	SYS_PWR_REQ_WAKEUPENABLE	RESERVED					SYS_PWR_REQ_INPUTENABLE	RESERVED				SYS_PWR_REQ_PULLTYPESELECT	SYS_PWR_REQ_PULLUDENABLE	RESERVED		

Bits	Field Name	Description	Type	Reset
31	SYS_PWRON_ RESET_OUT_WAKE-UPEVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
30	SYS_PWRON_ RESET_OUT_WAKE-UPENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
29:25	RESERVED		R	0x00
24	SYS_PWRON_ RESET_OUT_INPUTENABLE	Input enable value for pad sys_pwron_reset_out 0x0: Input buffere of I/O cell is disabled 0x1: Input buffere of I/O cell is enabled	RW	1
23:21	RESERVED		R	0x0
20	SYS_PWRON_ RESET_OUT_PULL-TYPESELECT	pullup/down selection for pad sys_pwron_reset_out 0x0: pulldown selected 0x1: pullup selected	RW	0
19	SYS_PWRON_RESET_ OUT_PULLUDENABLE	pullup/down enable for pad sys_pwron_reset_out 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
18:16	SYS_PWRON_RESET_ OUT_MUXMODE	Functional multiplexing selection for pad sys_pwron_reset_out 0x0: Select sys_pwron_reset_out 0x3: Select gpio_wk29 0x5: Select hw_dbg0 0x6: Select hw_dbg11	RW	0x0
15	SYS_PWR_REQ_WAKEUP-EVENT	Pad_x wake-up event status latched in the IO Read 0x0: No wake-up event occurred Read 0x1: A wake-up event occurred	R	0
14	SYS_PWR_REQ_WAKEUP-ENABLE	Input pad wake-up enable (and OFF mode input enable value) 0x0: wake-up detection is disabled 0x1: wake-up detection is enabled	RW	0
13:9	RESERVED		R	0x00

Bits	Field Name	Description	Type	Reset
8	SYS_PWR_REQ_IN-PUTENABLE	Input enable value for pad sys_pwr_req 0x0: Input buffere of I/O cell is disabled 0x1: Input buffere of I/O cell is enabled	RW	1
7:5	RESERVED		R	0x0
4	SYS_PWR_ REQ_PULLTYPESELECT	pullup/down selection for pad sys_pwr_req 0x0: pulldown selected 0x1: pullup selected	RW	1
3	SYS_PWR_REQ_PULL UDENABLE	pullup/down enable for pad sys_pwr_req 0x0: pullup/down disabled 0x1: pullup/down enabled	RW	1
2:0	RESERVED		R	0x0

Table 18.100. Register Call Summary for Register CONTROL_WKUP_PAD0_SYS_PWR_REQ_PAD1_SYS_PWRON_RESET_OUT

Control Module Functional Description

- PAD Functional Multiplexing and Configuration:[0]

Chapter 19. Mailbox

This chapter describes the differences in the Mailbox between the OMAP4430 Silicon Revision 2.x and OMAP4460 Silicon Revision 1.x multimedia devices.

Note

This chapter has not changed. Refer to OMAP4460 Silicon Revision 1.x TRM.

Chapter 20. Memory Management Units

This chapter describes the differences in the Memory Management Units between the OMAP4430 Silicon Revision 2.x and OMAP4460 Silicon Revision 1.x multimedia devices.

Note

This chapter has not changed. Refer to OMAP4460 Silicon Revision 1.x TRM.

Chapter 21. Spinlock

This chapter describes the differences in the Spinlock between the OMAP4430 Silicon Revision 2.x and OMAP4460 Silicon Revision 1.x multimedia devices.

Note

This chapter has not changed. Refer to OMAP4460 Silicon Revision 1.x TRM.

Chapter 22. Timers

This chapter describes the differences in the Timers between the OMAP4430 Silicon Revision 2.x and OMAP4460 Silicon Revision 1.x multimedia devices.

Note

This chapter has not changed. Refer to OMAP4460 Silicon Revision 1.x TRM.

Chapter 23. Serial Communication Interface

This chapter describes the differences in the Serial Communication Interfaces between the OMAP4430 Silicon Revision 2.x and OMAP4460 Silicon Revision 1.x multimedia devices.

23.1. Multimaster High-Speed I2C Controller

Note

This section has not changed. Refer to OMAP4460 Silicon Revision 1.x TRM.

23.2. HDQ/1-Wire

23.2.1. HDQ/1-Wire Overview

Refer to OMAP4460 Silicon Revision 1.x TRM.

23.2.2. HDQ/1-Wire Environment

Refer to OMAP4460 Silicon Revision 1.x TRM.

23.2.3. HDQ/1-Wire Integration

Refer to OMAP4460 Silicon Revision 1.x TRM.

23.2.4. HDQ/1-Wire Functional Description

- In OMAP4430, after the first successful presence detection, before a new 1-Wire initialization is performed, the user must execute a software reset on the HDQ/1-Wire module. This limitation is no longer present in OMAP4460.
- In OMAP4430, if interrupts are masked, the HDQ_CTRL_STATUS[4] GO bit does not self-clear after the operation completes. Software must clear the GO bit. This limitation is no longer present in OMAP4460.

23.2.5. HDQ/1-Wire Programming Models

Refer to OMAP4460 Silicon Revision 1.x TRM.

23.2.6. HDQ/1-Wire Register Manual

Refer to OMAP4460 Silicon Revision 1.x TRM.

23.3. UART/IrDA/CIR

Note

This section has not changed. Refer to OMAP4460 Silicon Revision 1.x TRM.

23.4. Multichannel Serial Port Interface (MCSPI)

Note

This section has not changed. Refer to OMAP4430 Silicon Revision 2.0 TRM.

23.5. Multichannel Buffered Serial Port (MCBSP)

Note

This section has not changed. Refer to OMAP4460 Silicon Revision 1.x TRM.

23.6. Multichannel PDM Controller

Note

This section has not changed. Refer to OMAP4460 Silicon Revision 1.x TRM.

23.7. Digital Microphone Module

Note

This section has not changed. Refer to OMAP4460 Silicon Revision 1.x TRM.

23.8. Multichannel Audio Serial Port

Note

This section has not changed. Refer to OMAP4460 Silicon Revision 1.x TRM.

23.9. Serial Low-Power Inter-Chip Media Bus Controller

Note

This section has not changed. Refer to OMAP4460 Silicon Revision 1.x TRM.

23.10. MIPI High-Speed Synchronous Serial Interface

Note

This section has not changed. Refer to OMAP4460 Silicon Revision 1.x TRM.

23.11. High-Speed Multiport USB Host Subsystem

Note

Note

This section has not changed. Refer to OMAP4460 Silicon Revision 1.x TRM.

23.12. High-Speed USB OTG Controller

Note

The High-Speed USB OTG Controller is an instantiation of the MUSBMHDRC from Mentor Graphics Corporation.

Note

This section has not changed. Refer to OMAP4460 Silicon Revision 1.x TRM.

23.13. Full-Speed USB Host Controller

Note

Note

This section has not changed. Refer to OMAP4460 Silicon Revision 1.x TRM.

Chapter 24. MMC/SD/SDIO

This chapter describes the differences in the MMC/SD/SDIO between the OMAP4430 Silicon Revision 2.x and OMAP4460 Silicon Revision 1.x multimedia devices.

Note

This chapter has not changed. Refer to OMAP4460 Silicon Revision 1.x TRM.

Chapter 25. General-Purpose Interface

This chapter describes the differences in the General-Purpose Interface between the OMAP4430 Silicon Revision 2.x and OMAP4460 Silicon Revision 1.x multimedia devices.

Note

This chapter has not changed. Refer to OMAP4460 Silicon Revision 1.x TRM.

Chapter 26. Keyboard Controller

This chapter describes the differences in the Keyboard Controller between the OMAP4430 Silicon Revision 2.x and OMAP4460 Silicon Revision 1.x multimedia devices.

Note

This chapter has not changed. Refer to OMAP4460 Silicon Revision 1.x TRM.

Chapter 27. Initialization

This chapter describes differences in initialization between the OMAP4430 Silicon Revision 2.x and OMAP4460 Silicon Revision 1.x multimedia devices.

27.1. Initialization Overview

Refer to OMAP4460 Silicon Revision 1.x TRM

27.2. Preinitialization

- A discrete DC-DC power regulator is added to replace the TWL6030 VCORE1 power resource. This is described in figures *Power Supply Connections* and *Clock, Reset and Control Environment*.
- New booting option is introduced: USB(2) (USBA0-USBPHY interface) with no VBUS monitoring from TWL6030. The ROM code continues with the USB procedure even if TWL6030 is not detected and the USB cable is not detected to be plugged. This enables USB boot with internal PHY when an alternate power IC is used. In that case, the internal transceiver must be powered and configured upon start up and does not require any action from the ROM code for its configuration.
- Booting from EMIF (LPDDR2-NVM) device is not supported
- Tables *Memory Preferred Booting* and *Peripheral Preferred Booting* are updated with sys_boot[4:0] booting options:
  - 0b00100
  - 0b01001
  - 0b01100
  - 0b10011
  - 0b11101

27.3. Power, Clocks, and Reset Power-Up Sequence

Refer to OMAP4460 Silicon Revision 1.x TRM

27.4. Device Initialization by ROM Code

- The ROM code base address is moved from 0x28000 to 0x30000 (32 Kbytes)
- ASIC-ID descriptor has been updated to discriminate OMAP4460 from other devices. Device identifier is 0x4440.
- USB Device Descriptor's field Product ID has been updated to discriminate OMAP4460 from other devices during USB boot. idProduct is 0xD010. Product ID String Descriptor is OMAP4440.

Support for SDRAM temperature monitoring at device reset is added. ROM code can wait for a predefined time for SDRAM temperature to fall to a safe value in case of a termal failure reset. This timeout can be controlled through the configuration header (CH) CHRAM item. Bits [8:11] at oofset 0054h have the following meaning:

- 0x0: no temperature monitoring
- 0x1: timeout 1 second
- 0x2: timeout 2 seconds
- 0x3: timeout 3 seconds
- 0x5: timeout 5 seconds
- 0xA: timeout 10 seconds

27.5. Services for HLOS Support

Refer to OMAP4460 Silicon Revision 1.x TRM

Chapter 28. On-Chip Debug Support

This chapter describes the differences in the On-Chip Debug Support between OMAP4430 Silicon Revision 2.x and OMAP4460 Silicon Revision 1.x.

28.1. Introduction

Refer to OMAP4460 Silicon Revision 1.x TRM.

28.2. Debug Ports

Refer to OMAP4460 Silicon Revision 1.x TRM.

28.3. Debugger Connection

Refer to OMAP4460 Silicon Revision 1.x TRM.

28.4. Primary Debug Support

Refer to OMAP4460 Silicon Revision 1.x TRM.

28.5. Power, Reset, and Clock Management Debug Support

Refer to OMAP4460 Silicon Revision 1.x TRM.

28.6. Performance Monitoring

28.6.1. Cortex-A9 MPU Subsystem Performance Monitoring

The PMUIRQ output of each Cortex-A9 CPUx PMU (where x = 0, 1) is directly routed to a Cortex-A9 MPU INTC input (MA_IRQ_54 for Cortex-A9 CPU0 PMU; MA_IRQ_55 for Cortex-A9 CPU1 PMU), along with being mapped to the CTIx TRIGIN[1] input.

28.6.2. Cortex-M3 MPU Subsystem Performance Monitoring

Refer to OMAP4460 Silicon Revision 1.x TRM.

28.6.3. DSP Subsystem Performance Monitoring

Refer to OMAP4460 Silicon Revision 1.x TRM.

28.7. Processor Trace

Refer to OMAP4460 Silicon Revision 1.x TRM.

28.8. System Instrumentation

28.8.1. MIPI STM

Refer to OMAP4460 Silicon Revision 1.x TRM.

28.8.2. Software Instrumentation

Refer to OMAP4460 Silicon Revision 1.x TRM.

28.8.3. OCP Watch-Point

Refer to OMAP4460 Silicon Revision 1.x TRM.

28.8.4. IVA-HD Pipeline

Refer to OMAP4460 Silicon Revision 1.x TRM.

28.8.5. NoC Statistics Collector

- The SDRAM statistics collector (SC_SDRAM) has the following functional updates:
  - Two additional probes from Memory Adapter (MA) module embedded in Cortex-A9 MPU subsystem; as a consequence, probe mapping is changed as follows:
    - Probe 0 – EMIF1 (DMM-EMIF1 port)
    - Probe 1 – EMIF2 (DMM-EMIF2 port)
    - Probe 2 – ~~EMIF modem (C2C-EMIF1 port)~~ Memory Adapter 1 (MA-EMIF1 port)
    - Probe 3 – Memory Adapter 2 (MA-EMIF2 port)
    - Probe 4 – EMIF modem (C2C-EMIF1 port)
  - Three additional data counters; as a consequence, counters configuration is changed as follows:
    - Counter 1 with one filter
    - Counter 2 with two filters
    - Counter 3 with one filter
    - Counter 4 ~~without any~~ with one filter
    - Counter 5 with one filter
    - Counter 6 without any filter
    - Counter 7 without any filter
  - OCP address filtering added as a filtering option

28.8.6. PM Instrumentation (PMI)

Refer to OMAP4460 Silicon Revision 1.x TRM.

28.8.7. CM Instrumentation (CMI)

Refer to OMAP4460 Silicon Revision 1.x TRM.

28.9. Concurrent Debug Modes

Refer to OMAP4460 Silicon Revision 1.x TRM.

28.10. Memory Mapping

Refer to OMAP4460 Silicon Revision 1.x TRM.