OMAP™

OMAP543x Multimedia Device
Engineering Samples ES2.0
Texas Instruments OMAP™ Family of Products

Data Manual Operating Condition Addendum
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HISTORY

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Note:

1. Creation.

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1 INTRODUCTION

The aim of this document is to describe the operating conditions of the all OMAP543x ES2.0 devices.

This document contains the description of each OPP (Operating Performance Point) for processors clocks and device core clocks.

Table 1-1 describes the supported operating performance point (OPP) on MPU for each OMAP543x devices.

Table 1-1. OMAP543x vdd_mpu Operating Points (1)

OMAP543x Devices	OPP_LOW_MPU	OPP_NOM_MPU	OPP_HIGH_MPU	OPP_SPEEDBIN_MPU
OMAP5430-SB	√	√	√	√
OMAP5430	√	√	√	
OMAP5432-SB	√	√	√	√
OMAP5432	√	√	√	

(1) This table is specific to vdd_mpu with AVS feature enabled.

Table 1-2 describes the supported operating performance point (OPP) on MM for each OMAP543x devices.

Table 1-2. OMAP543x vdd_mm Operating Points (1)

OMAP543x Devices	OPP_LOW_MM	OPP_NOM_MM	OPP_OD_MM
OMAP5430-SB	√	√	√
OMAP5430	√	√	√
OMAP5432-SB	√	√	√
OMAP5432	√	√	√

(1) This table is specific to vdd_mm with AVS feature enabled.

Table 1-3 describes the supported operating performance point (OPP) on CORE for each OMAP543x devices.

Table 1-3. OMAP543x vdd_core Operating Points (1)

OMAP543x Devices	OPP_NOM_CORE
OMAP5430-SB	√
OMAP5430	√
OMAP5432-SB	√
OMAP5432	√

(1) This table is specific to vdd_core with AVS feature enabled.

1.1 Device Support Nomenclature

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2 RECOMMENDED OPERATION

NOTE

All clocks frequencies mentioned in this document assume a system clock of 19.2MHz.

2.1 Micro Processor Unit (MPU)

CAUTION

The OPP voltage and frequency values may change following the silicon characterization result.

Table 2-1 shows the recommended vdd_mpu voltages ranges (MPU voltage at ball level) with AVS disabled.

Table 2-1: MPU Voltages with AVS disabled (1) (2) (3)

	RETENTION	OPP_BOOT_MPU		
	MIN	MIN	INITIAL SAFE	MAX
Vdd_mpu (V)	0.65	1.0	1.05	1.1

(1) Initial Safe voltage value documented in this table corresponds to the initial voltage to be applied at power IC level. Whereas, minimum and maximum voltage values correspond to the possible voltage at OMAP ball level.
(2) These vdd_mpu voltage ranges are defined with AVS feature disabled for Retention and OPP_BOOT_MPU operating points.
(3) Minimum OPP voltage values defined in this table include any voltage transient.

Table 2-2 shows the recommended vdd_mpu voltages ranges (MPU voltage at ball level) during operation.

Table 2-2: MPU Voltages during Operation (1)

	OPP_LOW_MPU (2)			OPP_NOM_MPU			OPP_HIGH_MPU			OPP_SPEEDBIN_MPU (3)		
	MIN	INITIAL SAFE	MAX	MIN	INITIAL SAFE	MAX	MIN	INITIAL SAFE	MAX	MIN	INITIAL SAFE	MAX
Vdd_mpu (V)	0.83	0.88	0.92	0.85	1.06	1.1	1.05	1.25	1.31	1.05	1.25	1.31

(1) Initial Safe voltage value documented in this table corresponds to the initial voltage to be applied at power IC level. Whereas, minimum and maximum voltage values correspond to the possible voltage at OMAP ball level.
(2) For all OPPs (except OPP_LOW where AVS is not supported), AVS has to be enabled to avoid impact on device reliability and lifetime POH (Power-On-Hours).
(3) OPP_SPEEDBIN_MPU operating point provides a higher guaranteed frequency in OPP_HIGH_MPU mode by performing binning during production test for the MPU. This operating point will only be available with some orderable part codes. For more information, please, contact your T.I. representatives.

Table 2-3 describes the standard processors clocks speed characteristics vs vdd_mpu (MPU voltage at ball level).

Table 2-3: MPU Clocks AC Performances (2) (3)

		OPP_LOW_MPU		OPP_NOM_MPU		OPP_HIGH_MPU		OPP_SPEEDBIN_MPU (1)	
Description	**Source Clock**	**Max Freq. (MHz)**	**Ratio**	**Max Freq. (MHz)**	**Ratio**	**Max Freq. (MHz)**	**Ratio**	**Max Freq. (MHz)**	**Ratio**
DPLL_MPU Locked Frequency	-	998	-	2200	-	1500	-	1699.2	-
MPU_GCLK (CLKOUT_M2)	DPLL_MPU Locked Frequency	499.2	2 * (M2 = 1) (DCC disabled) (4)	1000	2 * (M2 = 1) (DCC disabled) (4)	1500	M2 = 1 (DCC enabled) (4)	1699.2	M2 = 1 (DCC enabled) (4)

(1) OPP_SPEEDBIN_MPU operating point provides a higher guaranteed frequency in OPP_HIGH_MPU mode by performing binning during production test for the MPU. This operating point will only be available with some orderable part codes. For more information, please, contact your T.I. representatives.
(2) The DPLL ratios are configurable by software programming. For more information regarding the recommended DPLL ratios, including M2 above, see the *DPLL_MPU Preferred Settings* section of the OMAP543x TRM.
(3) The DPLL ratios documented in this table are recommended ratios. Other values may apply.
(4) For more information on the Duty Cycle Correction feature, see the PRCM chapter of the OMAP543x TRM.

NOTE

The programmable divider for the asynchronous bridge to Audio Back-end (ABE) must be set to:
- MPU_GCLK / 16 when MPU_GCLK clock is running at OPP_HIGH_MPU or OPP_SPEEDBIN_MPU.
- MPU_GCLK / 8 when MPU_GCLK clock is running at OPP_NOM_MPU or OPP_LOW_MPU.

The programmable divider for the asynchronous bridge to L3 must be set to:
- MPU_GCLK / 8 when MPU_GCLK clock is running at OPP_HIGH_MPU or OPP_SPEEDBIN_MPU.
- MPU_GCLK / 4 when MPU_GCLK clock is running at OPP_LOW_MPU or OPP_NOM_MPU.

For more information on the programmable dividers for the asynchronous bridges, see the CM_MPU_MPU_CLKCTRL register, CLKSEL_ABE_DIV_MODE and CLKSEL_EMIF_DIV_MODE bits, in the OMAP543x TRM.

Please make sure to set the corresponding register bits (increasing the divider value) before increasing the MPU_GCLK clock frequency (by sequence to a higher OPP).
Please make sure to decrease the MPU_GCLK clock frequency (by sequence to a lower OPP) before setting the corresponding register bits (decreasing the divider value).

CAUTION

During MPU DVFS sequencing to a higher OPP, please make sure to increase the voltage prior to the clocks frequencies.
During MPU DVFS sequencing to a lower OPP, please make sure to decrease the clocks frequencies prior to the voltage.
Not respecting this MPU DVFS sequencing may lead to internal timing violations.

2.2 MultiMedia (MM) and 3D Graphic Accelerator (GPU)

CAUTION

The OPP voltage and frequency values may change following the silicon characterization result.

2.2.1 MultiMedia (MM)

Table 2-4 shows the recommended vdd_mm voltages ranges (MultiMedia voltage at ball level) with AVS disabled.

Table 2-4: MultiMedia Voltages with AVS disabled[(1) (2) (3)]

	RETENTION	OPP_BOOT_MM		
	MIN	MIN	INITIAL SAFE	MAX
Vdd_mm (V)	0.65	1.0	1.05	1.1

(1) Initial Safe voltage value documented in this table corresponds to the initial voltage to be applied at power IC level. Whereas, minimum and maximum voltage values correspond to the possible voltage at OMAP ball level.
(2) These vdd_mm voltage ranges are defined with AVS feature disabled for Retention and OPP_BOOT_MM operating points.
(3) Minimum OPP voltage values defined in this table include any voltage transient.

Table 2-5 shows the recommended vdd_mm voltages ranges (MultiMedia voltage at ball level) during operation.

Table 2-5: MultiMedia Voltages during operation [(1)]

	OPP_LOW_MM [(2)]			OPP_NOM_MM			OPP_OD_MM		
	MIN	INITIAL SAFE	MAX	MIN	INITIAL SAFE	MAX	MIN	INITIAL SAFE	MAX
Vdd_mm (V)	0.83	0.88	0.92	0.82	1.025	1.07	0.93	1.12	1.17

(1) Initial Safe voltage value documented in this table corresponds to the initial voltage to be applied at power IC level. Whereas, minimum and maximum voltage values correspond to the possible voltage at OMAP ball level.
(2) For all OPPs (except OPP_LOW where AVS is not supported), AVS has to be enabled to avoid impact on device reliability and lifetime POH (Power-On-Hours).

Table 2-6 describes the standard processors clocks speed characteristics vs vdd_mm (MultiMedia voltage at ball level).

Table 2-6: MultiMedia Clocks AC Performances (1) (2)

		OPP_LOW_MM		OPP_NOM_MM		OPP_OD_MM	
Description	**Source Clock**	**Max Freq. (MHz)**	**Ratio**	**Max Freq. (MHz)**	**Ratio**	**Max Freq. (MHz)**	**Ratio**
DPLL_IVA Locked Frequency	-	2330	-	2330	-	1062.4	-
IVA_GCLK (CLKOUTX2_H12)	DPLL_IVA Locked Frequency	194.1	H12 = 12	388.3	H12 = 6	531.2	H12 = 2
DSP_GCLK (CLKOUTX2_H11)	DPLL_IVA Locked Frequency	233	H11 = 10	466	H11 = 5	531.2	H11 = 2

(1) The DPLL ratios are configurable by software programming. For more information regarding the recommended DPLL ratios, including H11, H12 above, see the DPLL_IVA Preferred Settings section of the OMAP543x TRM.
(2) The DPLL ratios documented in this table are recommended ratios. Other values may apply.

2.2.2 3D Graphic Accelerator (GPU)

Table 2-7 shows the standard graphic accelerator (GPU) clocks speed characteristics vs vdd_mm (MultiMedia voltage at ball level).

Table 2-7: Graphic Accelerator (GPU) Clocks (1) (3)

		OPP_LOW_MM		OPP_NOM_MM		OPP_OD_MM (2)	
Description	**Source Clock**	**Max Freq. (MHz)**	**Ratio**	**Max Freq. (MHz)**	**Ratio**	**Max Freq. (MHz)**	**Ratio**
Configuration 1 - From CORE DPLL – Locked Frequency @2127.36 MHz Maximum							
DPLL_CORE Locked Frequency	-	2127.36	-	2127.36	-	2127.36	-
CORE_GPU_CLK (CLKOUTX2_H14)	DPLL_CORE Locked Frequency	212.7	H14 = 5 (4)	425.47	H14 = 2.5 (4)	531.84	H14 = 2 (4)
GPU_CORE_GCLK	CORE_GPU_GCLK	212.7	1	425.47	1	531.84	1
Configuration 2 - From PER DPLL – Locked Frequency @768 MHz Maximum							
DPLL_PER Locked Frequency	-	768	-	768	-		
PER_GPU_CLK (CLKOUTX2_H14)	DPLL_PER Locked Frequency	192	H14 = 4	384	H14 = 2		
GPU_HYD_GCLK	PER_GPU_CLK	192	1	384	1		

(1) The DPLL ratios are configurable by software programming. For more information regarding the recommended DPLL ratios, including H14 above, see the *DPLL_CORE Preferred Settings* or, *DPLL_PER Preferred Settings* section of the OMAP543x TRM.
(2) The DPLL CORE is in the CORE domain that supports up to OPP_NOM_CORE operating point compared to the 3D GPU graphic accelerator (GPU) which is in the MultiMedia (MM) domain which supports up to the OPP_OD_MM operating point. Hence, based on the CORE_GPU_CLK output clocks of DPLL_CORE, the 3D graphic accelerator clock (GPU_CORE_GCLK) can supports up to OPP_HIGH_MM @600MHz based on the DPLL CORE in OPP_NOM_CORE operating point.
(3) The DPLL ratios documented in this table are recommended ratios. Other values may apply.
(4) For DPLL CORE, an additional division by 2 is performed after the HS divider.

CAUTION

During MM / GPU DVFS sequencing to a higher OPP, please make sure to increase the voltage prior to the clocks frequencies.
During MM / GPU DVFS sequencing to a lower OPP, please make sure to decrease the clocks frequencies prior to the voltage.
Not respecting this MM / GPU DVFS sequencing may lead to internal timing violations.

2.3 CORE

CAUTION

The OPP voltage and frequency values may change following the silicon characterization result.

Table 2-8 shows the recommended vdd_core voltages ranges (Core voltage at ball level) with AVS disabled.

Table 2-8: Core Voltages with AVS disabled (1) (2) (3)

	RETENTION	OPP_BOOT_CORE		
	MIN	MIN	INITIAL SAFE	MAX
Vdd_core (V)	0.81	1.0	1.05	1.1

(1) Initial Safe voltage value documented in this table corresponds to the initial voltage to be applied at power IC level. Whereas, minimum and maximum voltage values correspond to the possible voltage at OMAP ball level.
(2) These vdd_core voltage ranges are defined with AVS feature disabled for Retention and OPP_BOOT_CORE operating points.
(3) Minimum OPP voltage values defined in this table include any voltage transient.

Table 2-9 shows the recommended vdd_core voltages ranges (Core voltage at ball level) during operation.

Table 2-9: Core Voltages during operation (1)

	OPP_NOM_CORE		
	MIN	INITIAL SAFE	MAX
Vdd_core (V)	0.83	1.04	1.09

(1) Initial Safe voltage value documented in this table corresponds to the initial voltage to be applied at power IC level. Whereas, minimum and maximum voltage values correspond to the possible voltage at OMAP ball level.
(2) For all OPPs (except OPP_LOW where AVS is not supported), AVS has to be enabled to avoid impact on device reliability and lifetime POH (Power-On-Hours).

Table 2-10 shows the standard DPLL CORE clocks speed characteristics vs vdd_core (Core voltage at ball level).

Table 2-10: Core Clocks AC Performances – From DPLL CORE (1) (2)

		OPP_NOM_CORE	
Description	**Source Clock**	**Max Freq. (MHz)**	**Ratio**
DPLL_CORE Locked Frequency	-	2127.36	-
CORE_DLL_GCLK (CLKOUTX2_H11)	DPLL_CORE Locked Frequency	265.92	H11 = 8
CORE_X2_CLK (CLKOUTX2_H12)	DPLL_CORE Locked Frequency	531.84	H12 = 4
L3MAIN2_L3_GICLK	CORE_X2_CLK	265.92	2
L3MAIN2_L4_GICLK	L3MAIN2_L3_GICLK	132.96	2
EMIF_PHY_GCLK (CLKOUT_M2)	DPLL_CORE Locked Frequency	531.84	2 * (M2 = 2)
EMIF_FCLK (DDRPHY divider)	EMIF_PHY_GCLK	265.92	2
GPMC_CLK	L3MAIN2_L3_GICLK	265.92	2

(1) The DPLL ratios are configurable by software programming. For more information regarding the recommended DPLL ratios, including M2, H11, H12 above, see the *DPLL_CORE Preferred Settings* section of the OMAP543x TRM.
(2) The DPLL ratios documented in this table are recommended ratios. Other values may apply.

3 OPP DEPENDENCIES

CAUTION

The OPP dependencies apply only when both voltage domains are in ON state. That is:

- Any module in the domain may be powered, clocked and active
- SMPS is in active mode, delivering the voltage corresponding to current OPP

For more information on the Voltage Domain definitions, see the Power, Reset and Clock Management / Voltage Management Functional Description section in the OMAP543x TRM

Table 3-1 shows the acceptable OPP dependencies between MPU, CORE and MultiMedia voltage domains.

Table 3-1. OPP Dependencies between MPU, CORE and MultiMedia

vdd_mpu	vdd_core	vdd_mm
OPP_LOW_MPU	OPP_NOM_CORE	OPP_NOM_MM
OPP_NOM_MPU	OPP_NOM_CORE	OPP_LOW_MM
OPP_NOM_MPU	OPP_NOM_CORE	OPP_NOM_MM
OPP_HIGH_MPU	OPP_NOM_CORE	OPP_NOM_MM
OPP_NOM_MPU	OPP_NOM_CORE	OPP_OD_MM
OPP_HIGH_MPU	OPP_NOM_CORE	OPP_OD_MM
OPP_SPEEDBIN_MPU	OPP_NOM_CORE	OPP_OD_MM
OPP_SPEEDBIN_MPU	OPP_NOM_CORE	OPP_NOM_MM
OPP_LOW_MPU	OPP_NOM_CORE	OPP_LOW_MM
OPP_HIGH_MPU	OPP_NOM_CORE	OPP_LOW_MM
OPP_SPEEDBIN_MPU	OPP_NOM_CORE	OPP_LOW_MM
OPP_LOW_MPU	OPP_NOM_CORE	OPP_OD_MM

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