Sample & Hold Glitch Reduction for Precision Outputs

Reference Design

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TI Designs – Precision: Verified Design

Sample & Hold Glitch Reduction for Precision Outputs

Circuit Description

DAC R-2R architectures display great performance in regards to noise and accuracy, but at a cost of large glitch area. This design focuses on the reduction of major-carry glitches that occur from code specific transitions in DAC R-2R architectures. This design reduces this glitch area, making it suitable for glitch-sensitive applications such as waveform generation.

Design Resources

- TIPD142
- TINA-TI™
- DAC9881
- OPA2192
- TS12A4515

All Design files
SPICE Simulator
Product Folder
Product Folder
Product Folder

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1 Design Summary

The design requirements are as follows:

- Supply Voltage: (DAC9881: 5 V, OPA2192: +/-12 V, TS12A4515: 5 V)
- Input: 0 to +5 V
- Output: 0 to +5 V

The design goals and performance are summarized in Table 1. Figure 1 depicts the measured glitch area of the S&H design and DAC output.

Table 1. Comparison of Design Goals, Simulation, and Measured Performance

<table>
<thead>
<tr>
<th></th>
<th>Goal</th>
<th>Simulated</th>
<th>Measured</th>
</tr>
</thead>
<tbody>
<tr>
<td>TUE Error (%FSR)</td>
<td>0.015%</td>
<td>0.013689%</td>
<td>-0.0025%</td>
</tr>
<tr>
<td>Major-Carry Glitch Area Reduction</td>
<td>90%</td>
<td>----</td>
<td>94.3%</td>
</tr>
<tr>
<td>Settling time 0.003%FS (4000h-3C000h)</td>
<td>&lt;10μs</td>
<td>5.2 μs</td>
<td>8.35 μs</td>
</tr>
</tbody>
</table>

Figure 1: Measured Glitch Impulse Area (1FFFFh-20000h)
Theory of Operation

2.1 DAC Glitch Energy

Glitch Energy is mathematically described as the time integral of glitch power. However, most data sheets inaccurately term ‘glitch energy’ as the time integral of glitch voltage. The misnomer may have initially occurred to avoid the inclusion of load current, as this current value is dependent on the impedance connected to the DAC output. This design refers to the time integral of glitch voltage as ‘glitch impulse area’ or ‘glitch area’. Glitch impulse area is defined as the area associated with the overshoot or undershoot created by a code transition, and is generally quantified in Volt-seconds. There are two different types of glitches, single-lobe and double-lobe, which are mostly dependent on the DAC architecture. The DAC R-2R architecture produces the largest glitch in terms of amplitude and duration. An example waveform of this double-lobe glitch is displayed in Figure 2, which displays a glitch impulse area of 28 nV-s.

![Figure 2: DAC9881 Major Carry Glitch](image)

Different code-to-code transitions produce different levels of glitch impulses. DACs with R-2R architectures produce large glitches during major-carry transitions. For a complete explanation of R-2R architecture and glitch origin the reader is referred to Appendix B.
2.2 **Calculation of Glitch Impulse Area**

To calculate glitch area the waveform is plotted with respect to voltage and time. The area under the curve is then calculated using conventional integration methods. An example waveform with the corresponding glitch area equation is displayed in Figure 3.

![Calculation of Glitch Impulse Area](image)

**Figure 3: Glitch Area Calculation**

2.3 **Basic Sample and Hold Theory**

The glitch reduction technique employed in this design is based on an external Sample and Hold (S&H) circuit following the DAC output. In its simplest form the sample and hold circuit can be constructed from the following components: a capacitive element, output buffer, and switch. A schematic of the simplified S&H is shown in Figure 4.

![Basic Sample and Hold System](image)

**Figure 4: Basic Sample and Hold System**
The Sample/Track and Hold modes of operation correspond to the state of the switch, which connects the DAC output to the hold capacitor \( C_H \). In Sample mode — also referred to as Track mode -- the switch is closed, allowing the capacitor to charge or discharge to the sampled DAC output voltage. The operational amplifier is configured as a buffer, which tracks and passes the voltage seen across \( C_H \) to the output of the circuit.

In Hold mode the switch opens, disconnecting \( C_H \) from the DAC output. The DAC is updated while the circuit is in hold mode, preventing any DAC major carry glitches from propagating to the S&H output. The capacitor retains the previous sampled voltage, and this value is buffered to the output of the circuit. In real circuits, switch leakage and operational amplifier input bias current must be taken into consideration as it will impact circuit performance. The switch is generally controlled by an external discrete or digital driver.

Once the DAC glitch passes the switch closes and re-enters Sample/Track mode.

2.4 DAC Sample and Hold Glitch Reduction Block Diagram

A complete schematic of the DAC Sample and Hold Glitch Reduction circuit is displayed in Figure 5. The primary difference from the schematic and the previous simplified representation is the addition of an input buffer in the path from the DAC output to S&H output.

![Figure 5: DAC S&H Glitch Reduction Circuit](image)

The limitations of buffered DACs are typically drive strength and capability of driving large capacitive loads -- some DACs are only capable of driving a few milliamps of current. To prevent potential stability problems from driving a large capacitive load, an additional buffer stage is included between the DAC output and switch. The additional stage provides a high impedance input to the DAC output and is also capable of driving additional current, which is helpful when charging or discharging \( C_H \).

There are many challenges when designing a S&H system, which are mainly dependent on the different modes of operation. The following provides a theoretical overview of circuit performance during the different modes of operation.

2.4.1 Sample/Track Mode

In track mode, the primary specifications to design around are stability, offset, settling time, slew rate, bandwidth, nonlinearity and gain. Since the amplifier stages in this design are configured as unity gain, nonlinearity and gain are omitted from the theoretical overview. In other S&H circuits with gain stages, the impact of nonlinearity and gain error should be explored, as slight changes in any passive value will impact the overall transfer curve of the system.

As previously mentioned, the value of the hold capacitor, \( C_H \), has the greatest impact in regards to affecting stability and limiting the bandwidth of the overall circuit. To reduce this possibility, a buffer is placed in between the DAC output and \( C_H \). The implemented operational amplifier should be capable of driving large capacitive loads and output large current. Low input bias current and low input offset voltage is also desired in producing an output that tracks well with the input.
In the case where \( C_H \) exceeds the maximum load capacitance of the op amp, an additional resistor can be placed in between the op amp output and capacitor. This isolation resistor, \( R_S \), provides separation between \( C_H \) and the feedback path, ensuring optimal stability. To obtain the value of \( R_S \) the buffer stage is simulated with \( R_S \) and \( C_H \). \( R_S \) changes the magnitude and phase of the open loop gain of the system allowing the circuit to have acceptable phase margin. An additional isolation resistor, \( R_L \), is included in the final output stage. This final RC stage promotes further attenuation of small transients, as well as separating the feedback path from any large capacitances associated with output cable connections. More information regarding capacitive load solutions can be found in [1].

For non-major-carry transitions the switch remains closed passing the sampled DAC voltage to the S&H output. The settling time of the S&H system will rise with any increase in \( R_S \) and \( C_H \). The complete S&H model includes 3 RC stages, shown in Figure 6 -- the first RC filter is included to simulate the settling time of the DAC. Treating each stage independently is one way to generate a quick and simple settling time calculation. The combined calculations of each stage result in a worst case prediction of settling time, shown in Equation (1). In this design settling time is specified as 0.003% of Full-Scale (FS).

\[
t = -R_{DAC} C_{DAC} \ln \left( \frac{0.003\% \text{ FS}}{V_{IN}} \right) - R_S C_H \ln \left( \frac{0.003\% \text{ FS}}{V_{IN}} \right) - R_L C_L \ln \left( \frac{0.003\% \text{ FS}}{V_{IN}} \right) \tag{1}
\]

A more accurate model of settling time can be found by deriving the transfer function of the complete system. The complete model includes the input bias current and offset voltage of the op amps, and is displayed in Figure 6.

The time domain representation of \( V_{OUT}(t) \) is provided in Equation (2).

\[
V_{OUT}(t) = V_{IN} + \frac{X}{R_{DAC} C_{DAC}} e^{R_{DAC} C_{DAC} t} + \frac{Y}{R_S C_H} e^{R_S C_H t} + \frac{Z}{R_L C_L} e^{R_L C_L t} \pm I_{BIAS2} R_S \pm V_{OSA1} \pm V_{OSA2} \tag{2}
\]

Where,

\[
X = \frac{-V_{IN}}{(R_{DAC} C_{DAC})(1 - \frac{R_S C_H}{R_{DAC} C_{DAC}})(1 - \frac{R_L C_L}{R_{DAC} C_{DAC}})}
\]
The derivation of this Equation is provided in Appendix C.

$R_{DAC}$ and $C_{DAC}$ are back calculated using the settling time parameter in the DAC’s datasheet. The RC calculation is derived from the simple first order RC discharge model.

$$R_{DAC}C_{DAC} = -\frac{t}{\ln\left(\frac{0.003\% \text{FS}}{V_{IN}}\right)} \quad (3)$$

Another parameter that may impact settling time is the on-resistance of the solid state switch, $R_{ON}$. An illustration of this additional series resistance is provided in Figure 7. To update the previous formula, the switch on-resistance, $R_{ON}$, is linearly added to $R_S$, creating a new equivalent resistance value $R_S' = (R_S + R_{ON})$.

As an example, let’s assume the operational amplifier used in this TI Design draw 5 pA of input bias current, with an internal offset of 5 µV. Using this information, along with the passive components displayed in Figure 8 will produce the following representation of the S&H output.

$$V_{OUT}(t) = 5 - 12.351889 \cdot e^{-t/4.80108 \times 10^{-7}} + 7.352224 \cdot e^{-t/2.8454 \times 10^{-7}} \ldots$$

$$- 3.35008409327 \times 10^{-4} \cdot e^{-t/3 \times 10^{-9}} = 17.35 \times 10^{-11} \pm 2 \cdot 5 \times 10^{-6}$$

$R_{DAC}$ and $C_{DAC}$ are back calculated using the settling time published in the DAC datasheet. For reference, let’s assume that the DAC takes 5 µs to reach 0.003%FS. The RC calculation is derived from the simple first order RC discharge model.
\[
R_{DAC}C_{DAC} = \frac{-t}{\ln\left(\frac{0.003\% \text{FS}}{V_{IN}}\right)} = -\frac{5\mu s}{\ln\left(\frac{0.00015V}{5V}\right)} = 4.80108 \times 10^{-7} \Omega F
\]  

Equation (4) is graphed, and settling time is extracted as 0.003%FS. Settling time is shown as 5.40 \( \mu s \).

\[\Delta V_{OUT} = \frac{Q}{C}\]  

\[\Delta V_{OUT} \] is the measured offset voltage resulting from charge injection when the switch transitions to the hold state. \(\Delta V_{OUT}\) is related to charge injection through the equation:

**Figure 9: Settling Time of Theoretical Model**

**2.4.2 Sample/Track to Hold Transition**

During the Track to Hold transition a small amount of charge is injected onto the hold capacitor mostly due to the non-ideal switch -- all solid state switches include stray capacitances that create small level changes when transitioning between states. The resulting dc offset is typically referred to as pedestal error. An illustration of this pedestal error is shown in Figure 10.

\[\Delta V_{OUT} \] is the measured offset voltage resulting from charge injection when the switch transitions to the hold state. \(\Delta V_{OUT}\) is related to charge injection through the equation:

**Figure 10: Switch Pedestal error**
As (6) implies, pedestal error can be reduced by increasing the hold capacitor, although this comes at the expense of decreased bandwidth, longer acquisition time, and potential stability problems. In most solid state switch datasheets charge injection is graphed with respect to supply voltage, analog input or temperature. As an example, the switch incorporated in the S&H circuit specifies a typical value of 3 pC for the following conditions: 25°C, 5V supply, and 0V analog input.

For a pedestal error, \( \Delta V_{\text{OUT}} \), of 1mV Equation (6) yields a hold capacitance value of:

\[
C = \frac{3 \times 10^{-12}}{1 \times 10^{-3}} = 3 \text{ nF}
\]  

(7)

Charge injection varies with switch input voltage. As an example, the datasheet lists the charge injection as 3 pC for 0 V switch input. However, this charge injection number may increase as the input voltage is increased. Therefore, the charge injection for a 0 V switch input will be different from a 2.5 V switch input. A brief experiment is required to determine the actual charge injection value for a given input voltage. A known load capacitance is tied to the switch output at a specific switch input voltage. The switch is programmed to enter sample and then hold mode. During the sample-to-hold transition the switch output will produce a pedestal voltage. This pedestal voltage along with capacitor value is used to determine the amount of charge injected onto the capacitor.

### 2.4.3 Hold Mode

Once the switch fully opens the S&H circuit enters hold mode. In this mode the hold capacitor is disconnected from the input buffer, with the previously stored voltage value. Ideally this voltage value would remain constant, but imperfections in the output amplifier, switch, and hold capacitor create current draw that will either slowly charge or discharge the hold capacitor. The resulting droop in voltage is generally expressed in V/\(\mu\)s. The two main contributors to voltage droop are the switch 'off' leakage, \(I_{\text{LEAK}}\), and the input bias current, \(I_{\text{BIAS2}}\), of the operational amplifier. Additionally, the insulation resistance, which is the modeled parallel resistance \(R_p\), of the capacitor also affects droop since it creates a leakage path to ground. A modeled representation of the capacitor during hold mode is provided in Figure 11.

![Figure 11. S&H Model in Hold Mode](image)

The voltage across \(C_H\) can be found by applying Kirchhoff's current law, resulting in Equation (8).

\[
\frac{CdV}{dt} + I_{\text{bias}} + I_{\text{leak}} + \frac{V}{R_p} = 0
\]  

(8)
Solving the differential equation produces Equation (9).

\[ V(t) = \left( V_H + I_{\text{leak}} \cdot R_p + I_{\text{bias}} \cdot R_p \right) e^{-\frac{t}{R_p C}} - \left( I_{\text{leak}} \cdot R_p + I_{\text{bias}} \cdot R_p \right) \tag{9} \]

The droop rate is calculated by taking the time-derivative of \( V(t) \).

\[ \frac{dV}{dt} = -\left( \frac{1}{R_p \cdot C} \right) \left( V_H + I_{\text{leak}} \cdot R_p + I_{\text{bias}} \cdot R_p \right) e^{-\frac{t}{R_p C}} \tag{10} \]

As \( R_p \) approaches \( \infty \) the non-ideal model approaches an ideal representation and simplifies this expression to Equation (11).

\[ \frac{dV}{dt} = -\frac{(I_{\text{bias}} + I_{\text{leak}})}{C} \tag{11} \]

### 2.4.4 Hold to Sample/Track Transition

A worst case calculation of settling time was produced in the Sample/Track section, but only applies to a full-scale transition, which doesn’t include Hold or Hold to Sample transitions. The S&H circuit only enters Hold mode during DAC major carry transitions.

The settling time for this transition is calculated as a 2 stage RC with the switch output acting as a unit step with an amplitude equivalent to 1LSB. The corresponding equation is shown in Equation (12).

\[ V_{\text{OUT}}(t) = V_{\text{IN}} - \frac{V_{\text{IN}} R_S C_H}{(R_S C_H - R_L C_L)} \cdot e^{-\frac{t}{R_S C_H}} - \frac{V_{\text{IN}} R_L C_L}{(R_L C_L - R_S C_H)} \cdot e^{-\frac{t}{R_L C_L}} \ldots \tag{12} \]

\[ \pm I_{\text{BIAS2}} \cdot R_S \pm V_{\text{OSA2}} \]

This transition is also similar to the Track to Hold Transition as a small amount of switching transient is injected onto the hold capacitor before the DAC output voltage drives the voltage across the capacitor to its new value. Therefore the true settling time from this transition will depend on this additional pedestal voltage.
3 Component Selection

3.1 DAC Selection

DAC selection for this design is based on glitch performance, resolution, and end-use in precision instrumentation and automatic test equipment where minimal glitch energies are necessary in maintaining performance.

The DAC9881 is a single-channel device offering 18 bits or resolution, with fast settling time and an on-chip precision output amplifier. The maximum glitch impulse area produced by the device is 37nV-s.

3.2 Amplifier Selection

Two amplifiers must be selected in this design: one to drive the hold capacitor, \( C_H \), and another to buffer the voltage seen across the hold capacitor.

Both amplifiers should provide excellent dc precision, including rail-to-rail input/output, low offset, low offset drift and large bandwidth. Low input bias current is especially important, along with very high slew rate.

The OPA2192 was chosen for this design as it is capable of delivering all of these requirements: rail-to-rail input/output swing, +/-5 µV offset voltage, +/-5 pA bias current, 20 V/µs slew rate and 10 MHz bandwidth. The OPA2192 also conveniently includes two operational amplifiers in an 8-pin SOIC package enabling the reduction of PCB area to keep costs low.

3.3 Switch Selection

The switch in the design should feature low on-state resistance, low OFF-leakage, and handle rail-to-rail analog signals. Very low charge injection is also a primary factor in ensuring high S&H performance.

The TS12A4515 are single pole/single throw (SPST), low-voltage, single-supply CMOS analog switches with a 20 Ω on-state resistance, 3 pC of charge-injection (5 V supply) and an OFF-Leakage current value of 1nA.

3.4 Hold Capacitor Selection

This energy storage device is the foundation of the S&H circuit, since the physics and value of the component significantly affect S&H performance. The capacitor used should have very high insulation resistance – parallel resistance to ground. This resistance is heavily dependent on the dielectric of the capacitor, and can range from tens of megaohms for some electrolytic capacitors to tens of gigaohms for ceramic dielectrics. A low temperature coefficient is also necessary for correct operation across a wide temperature range.

Another parameter typically overlooked is dielectric absorption -- once the capacitor is discharged and left floating it will recover some residual charge and develop a small voltage. This voltage will affect sampled voltages during track and hold operation. Ceramic capacitors typically have a maximum dielectric absorption value of 0.6% and 2.5%, for class 1 (NP0/C0G) and class 2 (X7R) respectively. Electrolytic capacitors have much higher rates falling within 10% for Tantalum, and 15% for Aluminum.

The hold capacitor used in the design is a 8.2nF 5% 25V C0G capacitor. Other capacitors used in collecting data are also C0G capacitors.
4 Simulation

4.1 Pedestal Voltage vs Hold Capacitance

The charge injection of the switch, 3 pC, is used in Equation (6) to produce the Pedestal Error vs Capacitance graph, which is shown in Figure 12:

![Pedestal Error Graph](image)

Figure 12. Pedestal Error

4.2 Droop Voltage vs Hold Capacitance

Assuming an ideal capacitor model, Droop Rate vs Capacitance is calculated from Equation (11). The below input parameters are used to create Figure 13. (1) OPA2192 input bias: 5 pA (2) TS12A4515 OFF-Leakage: 1 nA

![Voltage Droop Error Graph](image)

Figure 13. Voltage Droop Error
To achieve similar results, capacitors with very high insulation resistances should be picked as any decrease in this resistance will affect droop rate. Equation (10) describes this time dependent droop rate for a non-ideal capacitor.

Figure 14 displays Voltage Droop vs Time with an initial $V_{\text{HOLD}}$ value of 7.5 mV across a 1 nF hold capacitor. Different insulation resistances are used in Equation (9) to generate the graph. As shown in the image, smaller insulation resistances result in a faster discharge -- this should intuitively make sense as current draw is inversely proportional to resistance. The slope of the curves become more linear as $R_P$ increases, nearing the ideal model derived in Equation (11). The input parameters are the following:

$C_H = 1$ nF, $I_{\text{LEAK}} = 1$ nA, $I_{\text{BIAS}} = 5$ pA.

\[
\frac{dV}{dt} = 1.005 \text{ [V/s]}
\]

![Figure 14. Voltage Droop vs Time (For Different $R_P$ values and $C_H = 1$nF)](image)

4.3 Rate-of-Closure (ROC) analysis

In this design different $C_H$, and $R_S$ values are evaluated to minimize voltage droop and pedestal error. ROC analysis is used to evaluate a minimum $R_S$ in driving a maximum hold capacitance of 10nF. This type of analysis and topology is discussed in [1]. A phase margin value equal to or greater than 60° is recommended ensuring 8.7% overshoot.

Starting the resistance value at 0 ohms reveals a phase margin of 25.47°, displayed in Figure 15.
Figure 15. OPA2192 ROC Analysis. $C_H = 10\, \text{nF}$, $R_S = 0\, \Omega$, $PM = 25.47^\circ$
Increasing $R_S$ improves the phase margin of the system. A resistance value of 14.7 Ω produces a phase margin of 60.97°. This is shown in Figure 16.

**Figure 16. OPA2192 ROC Analysis.** $C_H = 10nF$, $R_S = 14.7 \Omega$, $PM = 60.97^\circ$
4.4 Settling Time

An ideal model of the S&H circuit is created in TINA-TI™. The model uses ideal sources to model op amp input bias current and offset voltage, along with the RC stages shown in Figure 17. The output response of the circuit is shown in Figure 18.

It is important to note that the final $C_H$ value was obtained from experimental analysis, which is highlighted in Section 6. This final value was chosen as a balance between pedestal error, voltage droop, and settling time.

Substituting OPA2192 in place of the ideal op amp produces Figure 19, with corresponding settling time curve shown in Figure 20.
Figure 19. TINA-TI™ S&H Settling Time OPA2192 model

Figure 20. TINA-TI™ OPA2192 Settling time results

A summary of the settling time results are displayed in Table 2.

<table>
<thead>
<tr>
<th>Code Transition</th>
<th>Slew Rate (10% - 90%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Figure 9. Theoretical</td>
<td>5.40308 µs</td>
</tr>
<tr>
<td>Figure 18. Ideal Model</td>
<td>5.355901 µs</td>
</tr>
<tr>
<td>Figure 20. OPA2192 Model</td>
<td>5.206425 µs</td>
</tr>
</tbody>
</table>

Generally settling time is defined by min-code to max-code transitions. The DAC9881 datasheet indicates a typical settling time value of 5 µs for a 4.375 V step, [4000h to 3C000h] code transition.
The previous equations and schematics accounted for a full-scale (0-5V) transition, but are modifiable in producing a new settling time estimate. This new estimate is shown in Table 3.

### Table 3. Simulated Slew Rate [4.375V input]

<table>
<thead>
<tr>
<th>Code Transition</th>
<th>Slew Rate (10% - 90%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Figure 9. Theoretical Model</td>
<td>5.33896 µs</td>
</tr>
<tr>
<td>Figure 18. Ideal Model</td>
<td>5.29347 µs</td>
</tr>
<tr>
<td>Figure 20. OPA2192 Model</td>
<td>5.14047 µs</td>
</tr>
</tbody>
</table>

#### 4.5 TUE Error Calculation

Total unadjusted error (TUE) is obtained by computing the root square sum (RSS) of all errors generated from the DAC9881 and any passive or active components affecting gain, linearity, and offset.

Using information from the DAC9881 datasheet, integral non-linearity error is shown to have a maximum value of +/-3 LSBs for the DAC9881S device. The INL error is converted to % FSR by using Equation (14).

\[
\text{INL}_{\text{DAC}}(\%\text{FSR}) = \frac{\text{INL}_{\text{LSB}}}{2^{\text{bits}}} \cdot 100
\]  

\[
\text{INL}_{\text{DAC}}(\%\text{FSR}) = \frac{3\text{LSB}}{2^{18}} \cdot 100 = 0.00114\%
\]  

The gain error is also shown in the datasheet, having a maximum value of +/-32 LSBs. Equation (16) is used to convert gain error to %FSR.

\[
\text{GainError}_{\text{DAC}}(\%\text{FSR}) = \frac{\text{GainError}_{\text{LSB}}}{2^{\text{bits}}} \cdot 100
\]  

\[
\text{GainError}_{\text{DAC}}(\%\text{FSR}) = \frac{32\text{LSB}}{2^{18}} \cdot 100 = 0.0122\%
\]  

The DAC9881 includes an offset error which is created from the internal amplifier – the input bias currents of the internal amplifier interact with the R-2R output resulting in an offset voltage. The DAC9881 has a maximum offset value of 16 LSBs for 25°C, and 32 LSBs over a temperature range of -40°C to +105°C.

Using a value of 16 LSBs and Equation (18), the offset error is converted to %FSR.

\[
\text{OffsetError}_{\text{DAC}}(\%\text{FSR}) = \frac{\text{OffsetError}_{\text{LSB}}}{2^{\text{bits}}} \cdot 100
\]  

\[
\text{OffsetError}_{\text{DAC}}(\%\text{FSR}) = \frac{16\text{LSB}}{2^{18}} \cdot 100 = 0.0061\%
\]  

The S&H circuit does not include any passive elements affecting gain, but two operational amplifier stages do add a small offset voltage to the overall characteristic transfer function, which does impact the TUE of the system. The OPA2192 specifies a typical offset voltage of +/-5 µV, and a maximum value of 75 µV over a temperature range of -40°C to +105°C.
Using a value of 5 µV and Equation (20), the offset error generated from the op amp stages is converted to %FSR.

\[
\text{OffsetError}_{\text{OPA}}(\%\text{FSR}) = \frac{2 \cdot V_{\text{OPA OFFSET}}}{\text{FullScaleRange}} \cdot 100
\]

\[
\text{OffsetError}_{\text{OPA}}(\%\text{FSR}) = \frac{2 \cdot 5 \mu V}{5V} \cdot 100 = 0.0002\%
\]

All of the calculations performed above are included in the total unadjusted error, TUE, formula displayed in Equation (21). The equation combines all errors by taking the root square sum (RSS).

\[
\text{TUE} = \sqrt{\text{INL}_{\text{DAC}}^2 + \text{GainError}_{\text{DAC}}^2 + \text{OffsetError}_{\text{DAC}}^2 + \text{OffsetError}_{\text{OPA}}^2}
\]

\[
\text{TUE} = 0.013689032\%
\]
5 PCB Design

The PCB schematic and bill of materials can be found in Appendix A.

5.1 PCB Layout

The PCB layout for the top and bottom layers is shown in Figure 21 and Figure 22, respectively. General PCB layout design should be implemented, including but not limited to adequate bypass arrangement on power supplies and proper placement of analog and digital components.

The MSP430F5529 Platform is used to digitally drive the TS12A4515. The J5 and J7 connectors are responsible for interfacing the DAC9881 Glitch Reduction solution to the MSP430F5529 Launchpad.

![Figure 21. PCB Layout, Top Layer](image1)

![Figure 22. PCB Layout, Bottom Layer](image2)
6 Verification & Measured Performance

6.1 Glitch Impulse Area (DAC Output vs S&H Output)

Figure 23 and Figure 24 display the glitch impulse observed at the S&H output for different major-carry code transitions. For the DAC9881 device, maximum glitch energies are observed from code transitions [1FFFFh-20000h] and [20000h-1FFFFh]. A 1 µs hold signal – labeled One Shot – is generated preventing the DAC glitch from propagating to the S&H output. The 1mV offset is a result of pedestal error generated from switch transient, which is further explained in 6.2. The measured response of the system indicates a 94.3% reduction of glitch area.

![Figure 23: Measured Glitch Area (1FFFFh-20000h); C_H = 8.2nF, R_S = 14.7Ω: (TOP) Digital Signal One-Shot pulse; (MIDDLE) DAC Output Glitch; (BOTTOM) S&H Output Glitch](image)

$Glitch_{DAC} = 32.73nVs$

$Glitch_{SH} = 1.04nVs$
Figure 24. Measured Glitch Area (20000h-1FFFFh); $C_H = 8.2\, \text{nF}$, $R_S = 14.7\, \Omega$:

(TOP) Digital Signal One-Shot pulse; (MIDDLE) DAC Output Glitch; (BOTTOM) S&H Output Glitch
6.2 Pedestal and Voltage Droop Error

Figure 25 illustrates pedestal error with voltage droop for different \( C_H \) and \( R_S \) values. The figure displays that pedestal error decreases with \( C_H \). The figure also reveals that increasing \( R_S \) for a given capacitance will increase the amount of charge retained during switch transitions. This, however, does not impact the characteristic curve of the voltage droop, as the slope does not change for a given capacitance with different \( R_S \) values.

Using Equation (6), along with the pedestal voltage from “0Ω + 1200pF” the injected charge was calculated as 6.36pC. Assuming an ideal capacitor with Equation (11) will also produce an approximation of the cumulative switch plus input bias leakage:

\[
(I_{\text{bias}} + I_{\text{leak}}) = \frac{CdV}{dt} = (1200\text{pF})\left(\frac{0.098V}{s}\right) = 117.6\text{pA}
\]

This leakage value is considerably less than the previously calculated, as the datasheet generally guard bands in creating a maximum specified parameter.

![Pedestal Error + Voltage Droop](image)

**Figure 25. Measured Pedestal Error w/ Voltage Droop (1FFFFh-20000h);**

(TOP) Digital Signal One-Shot pulse; (BOTTOM) S&H Output Voltage
6.3 Slew Rate / Settling Time

Slew Rate was measured for two different code transitions – code transition [4000h-3C000h] and [0h-3FFFFh]. Figure 26 displays the relation between LDAC assertion and the ramping waveforms.

![S&H Slew Rate](chart.png)

Figure 26. DAC9881 S&H Measured Slew Rate; \( C_H = 8.2\text{nF}, R_S = 14.7\Omega \):
(TOP) LDAC Signal; (BOTTOM) S&H Output for different code transitions

<table>
<thead>
<tr>
<th>Code Transition</th>
<th>Slew Rate (10% - 90%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>00000h-3FFFFh</td>
<td>1.56 ( \mu \text{s} )</td>
</tr>
<tr>
<td>4000h-3C000h</td>
<td>1.12 ( \mu \text{s} )</td>
</tr>
</tbody>
</table>
Figure 27 displays 0.003%FS settling time of the DAC9881 and S&H output for a 4.375V transition [4000h-3C000h]. This figure also displays settling in relation to LDAC assertion, and displays the final settled voltage for comparison. Table 5 shows the time to reach 0.003%FS of the settled code 3C000h.

In this design, the DAC9881 settling time value was measured as 7.55 µs. The S&H settling time was measured as 8.35 µs.

![Figure 27. DAC9881 S&H Measured Settling Time; C_H = 8.2nF, R_S = 14.7Ω:](image)

<table>
<thead>
<tr>
<th>Output</th>
<th>Time to Reach 0.003% Full-Scale</th>
</tr>
</thead>
<tbody>
<tr>
<td>DAC9881 Output</td>
<td>7.55 µs</td>
</tr>
<tr>
<td>S&amp;H Output</td>
<td>8.35 µs</td>
</tr>
</tbody>
</table>
6.4 Error Calculation

Figure 32 graphs the measured S&H transfer function from code 0 to code $2^{18}$.

![Figure 28. DAC9881 S&H Measured Transfer Function](image)

Figure 28. DAC9881 S&H Measured Transfer Function

Figure 29 and Figure 30 display the performance of the S&H output voltage near the supply rails for the first and last 1000 codes. Near zero-scale and full-scale the internal amplifier does not have enough headroom resulting in non-linear behavior and preventing full rail-to-rail output swing.

![Figure 29. Voltage output for code 0 to 1000](image)
The INL, DNL, Offset Error, and TUE figures are provided below. For correlation purposes, this data is plotted from the code ranges included in the DAC9881 datasheet – 2048 to 260096. Any error derived from S&H performance is mostly limited to the DAC9881 device, with the exception of op amp offset.

Table 6 displays the maximum error and average obtained on 3 boards. Linearity, offset and gain error are measured using a two-point line of best fit including one data point near zero-scale and another near full-scale. The minimum and maximum codes used in this design are 2048 and 260096, respectively.

**Table 6. Measured Error Values**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Maximum Error</th>
<th>Average Error</th>
</tr>
</thead>
<tbody>
<tr>
<td>Offset Error (%FSR)</td>
<td>-0.000817301587</td>
<td>-0.00060449735</td>
</tr>
<tr>
<td>Gain Error (%FSR)</td>
<td>-0.001645714285</td>
<td>-0.00155767195</td>
</tr>
<tr>
<td>INL Error (%FSR)</td>
<td>-0.000674939958</td>
<td>-0.00059620769</td>
</tr>
<tr>
<td>Measure TUE (%FSR)</td>
<td>-0.002695292968</td>
<td>-0.0024526432</td>
</tr>
</tbody>
</table>

Equations (24), (25), (26) and (27) are used to calculate offset error, gain error, INL and TUE from measured results.

\[
\text{Offset Error } \%\text{FSR} = \frac{V_{\text{OUT}(\text{LOW Code})} - (\text{Low Code}) \cdot \text{LSB}_{\text{Measured}}}{\text{Full Scale Range}} \cdot 100
\]  \hspace{1cm} (24)

\[
\text{Gain Error } \%\text{FSR} = \frac{\text{LSB}_{\text{Measured}} - \text{LSB}_{\text{Ideal}}}{\text{LSB}_{\text{Ideal}}} \cdot 100
\]  \hspace{1cm} (25)
\[ INL(k) = \sum_{j=0}^{k} (DNL(j)) \]  

\[ TUE\,(\%\text{FSR}) = \frac{V_{\text{Code(Measured)}} - V_{\text{Code(Ideal)}}}{\text{Full\_Scale\_Range}} \times 100 \]  

Where,

\[ LSB_{\text{Measured}} = \frac{(V_{\text{OUT(High\_Code)}} - V_{\text{OUT(Low\_Code)}})}{\text{High\_Code-Low\_Code}} \]  

**Figure 31. DAC9881 S&H DNL Error**
Figure 32. DAC9881 S&H INL Error

Figure 33. DAC9881 TUE Error %FSR
7 Modifications

This S&H circuit was designed to address the large glitch impulses of R-2R DACs, but can be easily modified to accommodate any type of analog input. It is important to note the internal amplifier in the DAC9881, as most R-2R architectures may not include this internal op amp stage. Table 7 provides examples of different op amps that can be used when designing with an un-buffered DAC. The operation amplifiers feature excellent input bias current, offset voltage, and bandwidth specifications.

<table>
<thead>
<tr>
<th>OPA</th>
<th>Supply Voltage</th>
<th>Bandwidth</th>
<th>Input Bias Current</th>
<th>Offset Voltage</th>
<th>Slew Rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPA172</td>
<td>+/- 18V</td>
<td>10MHz</td>
<td>15pA</td>
<td>1mV</td>
<td>10V/µs</td>
</tr>
<tr>
<td>OPA2172</td>
<td>+/- 18V</td>
<td>10MHz</td>
<td>15pA</td>
<td>1mV</td>
<td>10V/µs</td>
</tr>
<tr>
<td>OPA140</td>
<td>+/- 18V</td>
<td>11MHz</td>
<td>10pA</td>
<td>0.12mV</td>
<td>20V/µs</td>
</tr>
<tr>
<td>OPA2192</td>
<td>+/- 18V</td>
<td>10MHz</td>
<td>5pA</td>
<td>5µV</td>
<td>20V/µs</td>
</tr>
</tbody>
</table>

Additionally, if a multi-channel solution is desired, the following multi-channel DACs offer high performance in regards to resolution, noise, and linearity.

<table>
<thead>
<tr>
<th>DAC</th>
<th>Resolution</th>
<th>Channel Count</th>
<th>Relative Accuracy (Max)</th>
<th>Output Vrange Min/Max [V]</th>
<th>Noise (nV/sqrt(Hz))</th>
</tr>
</thead>
<tbody>
<tr>
<td>DAC8881</td>
<td>16-bit</td>
<td>1</td>
<td>+/- 1 LSB</td>
<td>0/5.5</td>
<td>30</td>
</tr>
<tr>
<td>DAC8831ICD</td>
<td>16-bit</td>
<td>1</td>
<td>+/- 1 LSB</td>
<td>-5.5/5.5</td>
<td>18</td>
</tr>
<tr>
<td>DAC7632VFB</td>
<td>16-bit</td>
<td>2</td>
<td>+/- 3LSB</td>
<td>-2.5/2.5</td>
<td>60</td>
</tr>
<tr>
<td>DAC7634EB</td>
<td>16-bit</td>
<td>4</td>
<td>+/- 3LSB</td>
<td>-2.5/2.5</td>
<td>60</td>
</tr>
</tbody>
</table>

The switch component of this design is also in a convenient 5-pin SOT 23 package, which is compatible among other switch devices. For additional single and multi-channel switches the reader is referred to Table 9. This table displays switch performance in terms of charge injection, on-resistance, as well as leakage.

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>TS12A4516</td>
<td>1</td>
<td>13pC</td>
<td>25Ω</td>
<td>5nA</td>
</tr>
<tr>
<td>TS5A3166</td>
<td>1</td>
<td>2pC</td>
<td>0.9Ω</td>
<td>80nA</td>
</tr>
<tr>
<td>TS5A21366</td>
<td>2</td>
<td>1.3pC</td>
<td>0.75Ω</td>
<td>10nA</td>
</tr>
</tbody>
</table>
8 About the Author

Matthew Saucedas is an applications engineer in the precision digital to analog converters group at Texas Instruments where he supports telecommunication and catalog products. Matthew received his MSEE from Texas A&M University in 2009.
9 Acknowledgements & References

Online Sources:

Appendix A.

A.1 Electrical Schematic

Figure A-1: Electrical Schematic
## A.2 Bill of Materials

### Figure A-2: Bill of Materials

<table>
<thead>
<tr>
<th>Item</th>
<th>Quantity</th>
<th>Designator</th>
<th>Description</th>
<th>Manufacturer</th>
<th>Manufacturer PN</th>
<th>DigiKey PN</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>12</td>
<td>C1, C2, C3, C4, C5, C14, C15, C16, C17, C18, C19, C20</td>
<td>CAP, CERM, 1uF, 25V, +/-10%, X5R, 0603</td>
<td>MuRata</td>
<td>GRM188R61E105KA12D</td>
<td>490-3897-1-ND</td>
</tr>
<tr>
<td>2</td>
<td>6</td>
<td>C6, C7, C8, C9, C10, C11</td>
<td>CAP, CERM, 510 pF, 50 V, +/-5%, COG/NP0, 0402</td>
<td>MuRata</td>
<td>GRM1555C1H511JA01D</td>
<td>490-3237-1-ND</td>
</tr>
<tr>
<td>3</td>
<td>1</td>
<td>C12</td>
<td>CAP, CERM, 8200 pF, 25 V, +/-5%, COG/NP0, 0603</td>
<td>MuRata</td>
<td>GRM1885C1H301JA01D</td>
<td>490-1438-1-ND</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
<td>C13</td>
<td>Header, 100mil, 2x1, Gold, TH</td>
<td>TDK</td>
<td>C1608CG01E822J</td>
<td>445-2668-1-ND</td>
</tr>
<tr>
<td>5</td>
<td>3</td>
<td>J1, J3, J4</td>
<td>Header, 100mil, 3x1, Gold, TH</td>
<td>Samtec</td>
<td>TSW-102-07-G-S</td>
<td>SAM1029-02-ND</td>
</tr>
<tr>
<td>6</td>
<td>1</td>
<td>J2</td>
<td>Header, 100mil, 3x1, Gold, TH</td>
<td>Samtec</td>
<td>TSW-103-07-G-S</td>
<td>SAM1029-03-ND</td>
</tr>
<tr>
<td>7</td>
<td>2</td>
<td>J5, J7</td>
<td>Connector, Receptacle, 100mil, 10x2, Gold plated, TH</td>
<td>Samtec, Inc.</td>
<td>SSW-110-23-F-D</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>1</td>
<td>J6</td>
<td>Terminal Block, 6A, 3.5mm Pitch, 2-Pos, TH</td>
<td>On-Shore Technology</td>
<td>ED555/2DS</td>
<td>ED1514-ND</td>
</tr>
<tr>
<td>9</td>
<td>4</td>
<td>R1, R2, R3, R4</td>
<td>RES, 10.0 k, 1%, 0.1 W, 0402</td>
<td>Panasonic</td>
<td>ERI-2RF1002X</td>
<td>P10.0KLC-ND</td>
</tr>
<tr>
<td>10</td>
<td>6</td>
<td>R6, R7, R8, R9, R10, R11</td>
<td>RES, 24.3, 1%, 0.063 W, 0402</td>
<td>Vishay-Dale</td>
<td>CRCW040224R3FKED</td>
<td>541-24.3LCT-ND</td>
</tr>
<tr>
<td>11</td>
<td>1</td>
<td>R12</td>
<td>RES, 10.0, 1%, 0.1 W, 0603</td>
<td>Vishay-Dale</td>
<td>CRCW060310R0FKEA</td>
<td>541-10.0HCT-ND</td>
</tr>
<tr>
<td>12</td>
<td>1</td>
<td>R13</td>
<td>RES, 14.7, 1%, 0.1 W, 0603</td>
<td>Vishay-Dale</td>
<td>CRCW060314R7FKEA</td>
<td>541-14.7HCT-ND</td>
</tr>
<tr>
<td>13</td>
<td>1</td>
<td>R14</td>
<td>RES, 0, 5%, 0.1 W, 0603</td>
<td>Vishay-Dale</td>
<td>CRCW0603000020EA</td>
<td>541-0.0GCT-ND</td>
</tr>
<tr>
<td>14</td>
<td>1</td>
<td>TP1</td>
<td>Test Point, Miniature, Orange, TH</td>
<td>Keystone</td>
<td>5003</td>
<td>5003K-ND</td>
</tr>
<tr>
<td>15</td>
<td>1</td>
<td>TP2</td>
<td>Test Point, Miniature, White, TH</td>
<td>Keystone</td>
<td>5002</td>
<td>5002K-ND</td>
</tr>
<tr>
<td>16</td>
<td>2</td>
<td>TP3, TP4</td>
<td>Test Point, Miniature, Black, TH</td>
<td>Keystone</td>
<td>5001</td>
<td>5001K-ND</td>
</tr>
<tr>
<td>17</td>
<td>1</td>
<td>U1</td>
<td>18-Bit, Single-Channel, Low-Noise, Voltage-Output DIGITAL-TO-ANALOG CONVERTER, RGE0024B</td>
<td>Texas Instruments</td>
<td>DAC9881SRGET</td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>1</td>
<td>U2</td>
<td>High Voltage, Rail-to-Rail Input/Output, Precision Operational Amplifiers, e-trim™ Series, D0008A</td>
<td>Texas Instruments</td>
<td>OPA2192IDR</td>
<td></td>
</tr>
<tr>
<td>19</td>
<td>1</td>
<td>U3</td>
<td>SPST CMOS ANALOG SWITCHES, DBV0005A</td>
<td>Texas Instruments</td>
<td>TS12A4515DBVR</td>
<td></td>
</tr>
</tbody>
</table>
Appendix B.

B.1 R-2R Architecture and Glitch origin

A simplified 4-bit representation of a buffered R-2R architecture is shown in Figure 34. Each bit of the data converter corresponds to a switch on the 2R leg of the ladder, which connects to $V_{REFH}$ or GND. The overall concept is based on the principle of voltage division -- the effective output voltage is the additive superposition of each 2R leg connected to $V_{REFH}$. Therefore, the 4-bit representation produces the output voltage listed in Equation (28).

$$V_{OUT} = V_{REFH} - \frac{V_{REFH}}{16} - V_{REFH} \left( \frac{B_3}{2} + \frac{B_2}{4} + \frac{B_1}{8} + \frac{B_0}{16} \right)$$  \hspace{1cm} (28)$$

Figure 34: 4-bit representation of DAC9881

R-2R DAC architectures display large glitch energies at major-carry transitions. A major-carry transition is a single-code transition that causes the most significant bit (MSB) to change because of the transitioning lower bits (LSBs). In the case of the DAC9881, the worst-case major-carry glitches occur at 2000h to 1FFFFh, and 1FFFFh to 20000h.

These glitch impulses are highly dependent on the parasitic capacitances associated with the analog switches. Figure 34 simplified the model of the switches to a single-pole-double-throw, SPDT, model, but a more accurate model is provided in Figure 35.

Figure 35: CMOS Transistor Model of SPDT Switch
The switches are constructed of a parallel NMOS and PMOS transistor. Each transistor exhibits stray capacitances in the form of the gate-to-drain, gate-to-source, and gate-to-channel capacitances (C_{gd}, C_{gs}, and C_{g} respectively). In voltage R-2R architectures, the main parasitic capacitors affecting output performance are the gate-to-drain capacitances, C_{gd} and C_{gd}. To prevent possible shoot-through current from V_{REFH} to V_{REFL}, occurring when both transistors conduct in saturation, a break-before-make switching scheme is generally employed ensuring that one of the transistors is fully off before activating the remaining transistor in parallel. Although this method eliminates shoot-through current, it essentially creates a time delayed switching structure that produces large glitch impulses from charging and discharging C_{gd} and C_{gd}. 
Appendix C.

C.1 DAC Settling time derivation

V_in is treated as a unit step voltage source transitioning from 0 to 5V, with other sources being held constant. Applying the theorem of superposition, the voltage at the output node is equivalent to the algebraic sum of all voltages generated from each acting source.

Therefore,

\[ V_{OUT}(t) = V_{OUT\text{in}}(t) \pm I_{\text{BIAS}2} \cdot R_S \pm V_{OSA1} \pm V_{OSA2} \]  (29)

To find the output voltage produced by the unit step voltage source we can derive the frequency-based s-domain transfer function across the output capacitor, C_L, as \( V_{OUT\text{in}}(s) \) and take the inverse Laplace transform to express the output as a function of time, \( V_{OUT\text{in}}(t) \).

\[ V_{OUT\text{in}}(s) = \frac{V_{IN}}{s(R_{DAC}C_{DAC} + 1)(sR_S + 1)(sR_LC_L + 1)} \]  (30)

Partial fraction expansions and inverse Laplace transform yields the following expression:

\[ V_{OUT\text{in}}(s) = \mathcal{L}^{-1}\{ V_{OUT\text{in}}(s) \} \]

\[ \mathcal{L}^{-1}\{ V_{OUT\text{in}}(s) \} = V_{IN} + \frac{X}{R_{DAC}C_{DAC}} \cdot e^{-tR_{DAC}C_{DAC}} + \frac{Y}{R_SC_H} \cdot e^{-tR_SC_H} + \frac{Z}{R_LC_L} \cdot e^{-tR_LC_L} \]  (31)

Where,

\[ X = \frac{V_{IN}}{R_{DAC}C_{DAC}(1 - \frac{R_S}{R_{DAC}C_{DAC}})(1 - \frac{R_L}{R_{DAC}C_{DAC}})} \]

\[ Y = \frac{V_{IN}}{(R_S + 1)(1 - \frac{R_{DAC}}{R_SC_H})(1 - \frac{R_L}{R_{DAC}C_L})} \]

\[ Z = \frac{V_{IN}}{(R_L + 1)(1 - \frac{R_{DAC}}{R_LC_L})(1 - \frac{R_S}{R_{DAC}C_L})} \]

\[ \therefore V_{OUT}(t) = V_{IN} + \frac{X}{R_{DAC}C_{DAC}} \cdot e^{-tR_{DAC}C_{DAC}} + \frac{Y}{R_SC_H} \cdot e^{-tR_SC_H} + \frac{Z}{R_LC_L} \cdot e^{-tR_LC_L} \pm I_{\text{BIAS}2} \cdot R_S \pm V_{OSA1} \pm V_{OSA2} \]  (32)
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