Microcontroller PWM to 12bit Analog Out

**TI Precision Designs**

TI Precision Designs are analog solutions created by TI’s analog experts. Verified Designs offer the theory, component selection, simulation, complete PCB schematic & layout, bill of materials, and measured performance of useful circuits. Circuit modifications that help to meet alternate design goals are also discussed.

**Circuit Description**

This design note provides a passive RC filter design for PWM to analog conversion, as well as a test circuit for verifying that the filter meets the design goals. Methods for selecting the passive filter’s order, cutoff frequency, and component values for achieving a targeted resolution are described. The design example shows a 12 bit filter but the method could be used for other resolutions. The test circuit is needed to confirm that the output error (ripple) meets the design requirements because this cannot be directly measured using standard test equipment.

**Design Resources**

- **Design Archive**
- **TINA-TI™**
- **OPA2209**
- **MSP430**
- **All Design files**: SPICE Simulator, Product Folder, Product Folder
- **Ask The Analog Experts**
- **WEBENCH® Design Center**
- **TI Designs Precision Library**

**Ripple Measurement Test**

- **Square wave Signal Generator** (PWM 50% duty cycle)
- **4th order passive LPF**
- **Post Amp ac coupled** $G = 1024 \text{ V/V}$
- **Scope To Measure Ripple**

---

**Important Notice**

An IMPORTANT NOTICE at the end of this TI reference design addresses authorized use, intellectual property matters and other important disclaimers and information.

TINA-TI is a trademark of Texas Instruments
WEBENCH is a registered trademark of Texas Instruments

Copyright © 2013, Texas Instruments Incorporated
1 Design Summary

The design requirements for PWM filter are as follows:

- Input: 3.3 Vpp square wave to simulate 50% duty cycle PWM
- Filter output: DC with 12-bit resolution (Maximum ripple: 403uVpp)

The design requirements for Post Amp are as follows:

- Supply Voltage: ±15 V dc (for post amplifier)
- Post amplifier gain: 1024 V/V, ac coupled

The design goals and performance for 12bit, system resolution are summarized in Table 1. Figure 1 depicts the measured ripple for 12bit system resolution with 1024 times gain of the RC low pass filter design.

Table 1: Comparison of Design Goals, Simulated Performance, and Measured Results

<table>
<thead>
<tr>
<th>System Resolution</th>
<th>Goal Max Ripple</th>
<th>Simulated Ideal Components</th>
<th>Measured Results</th>
</tr>
</thead>
<tbody>
<tr>
<td>12bit (filter out)</td>
<td>403uVpp</td>
<td>344.48uVpp</td>
<td>347.66uVpp</td>
</tr>
<tr>
<td>12bit (post amp out)</td>
<td>412mVpp</td>
<td>396mVpp</td>
<td>404mVpp</td>
</tr>
</tbody>
</table>

Figure 1: PWM Output Ripple Verification for 12 bit System (Gain = 1024V/V)
2 Theory of Operation

2.1 Design Overview

Pulse Width Modulation (PWM) is a technique where the width of digital pulses is adjusted to generate different average dc voltages. Most microcontrollers have a built-in timer that can be used to generate a PWM signal. PWM outputs can be converted to a dc voltage by using a series of RC low pass filters to average the pulses. Thus, a filtered PWM circuit is a simple low cost method to convert digital to analog (i.e. create a DAC). The main goal of this design is to convert PWM to analog output and achieve a 12 bit resolution with a ripple signal less than one half LSB. A secondary goal is to develop a circuit that amplifies the output ripple (error) to a level that an oscilloscope can measure. A system block diagram is shown in Figure 2.

![System block diagram](image)

Figure 2: System block diagram
The PWM output from a microcontroller is a square wave that has a programmable pulse width (duty cycle). The output of a simple RC filter connected to the PWM output will charge to the average voltage of the PWM signal. **Figure 3** shows a 10% and 90% duty cycle PWM signal connected to a simple RC filter. Note that the output charges to approximately 90% of the square wave's amplitude for a 90% duty cycle. In general, the ideal average dc output is PWM amplitude multiplied by the duty cycle (i.e. $V_{out} = V_{PWM} \times \text{Duty\_Cycle}$). The charge and discharge of the filter capacitor can also be seen in **Figure 3**. The peak-to-peak amplitude of the variations caused by the charge and discharge of the filter capacitor is called the ripple. The objective is to convert the PWM signal to a dc voltage so ideally the ripple would be zero. The results shown in **Figure 3** are for a single pole RC filter; adding additional filter stages will further minimize the ripple. The ripple can be thought of as an error that limits the resolution of the signal. As a rule of thumb the ripple should be kept to half the voltage resolution. To achieve our resolution objective (12 bits) we will have to determine the number of filter stages and the cutoff frequency required to reduce the ripple to half of the voltage resolution.

**Figure 3: PWM Signal and dc Output for 10% and 90% Duty Cycle**
Another factor that controls the resolution is the degree by which the width of the PWM signal can be adjusted. A common method for generating PWM signals is to use a binary counter. Figure 4 shows the generation of two different PWM signals with an 8 bit counter. The counter output remains high until the desired duty cycle is met and then it is reset. The MSP430 microcontroller uses this principle with a 16 bit counter. The number of bits in the counter corresponds to the bits of resolution in the analog output if the signal is properly filtered. For this design our goal is 12 bit resolution, so a 12 bit counter is needed to achieve 12 bits of resolution. Later in this document we will discuss the trade-offs associated with higher resolution systems.

![Figure 4: PWM for an 8 Bit Counter](image-url)

1/8 \(=0.125\)  
12.5% duty cycle

2/8 \(=0.25\)  
25% duty cycle

Copyright © 2013, Texas Instruments Incorporated
**Figure 5** illustrates the PWM (counter) output on the MSP430. In this figure the full 16 bit (i.e. 65,536) counter is being used. In **Figure 5** the PWM output is configured for the minimum duty cycle (i.e. 1 count in 65,536 or 0.00153% duty cycle). The period of one count is 62.5ns for the MSP430 at a master clock frequency of 16MHz. The period of the entire 16 bit clock cycle is 4.096ms (62.5 ns x 65536). The PWM frequency is 244Hz ($f_{PWM\_Cycle} = 4.096$ms).

![Figure 5: PWM for a 16 bit Counter (Frequency, Period, and Duty Cycle shown)](image)

In the case of this design our resolution objective is 12 bits, so we only need 12 bits of the 16 bit counter in the MSP430. **Figure 6** shows the PWM signal where the counter is reset after 12 bits. The resolution is now 1/4096 or a 0.0244% duty cycle. Limiting the counter to 12 bits also affects the period and frequency of the PWM signal. The frequency of the 12 bit PWM signal is 3.91kHz which is substantially higher than the 16 bit PWM frequency (244Hz). The PWM frequency is the frequency by which analog output can be adjusted. The PWM frequency also determines the cutoff frequency of the filter.

![Figure 6: PWM for a 12 bit Counter (Frequency, Period, and Duty Cycle shown)](image)
2.2 PWM Filter Design

The PWM signal is a square wave with a different duty cycle depending on the dc output voltage target. The filter will convert the square wave to an average dc voltage. Remember that a square wave is composed of a series of sinusoidal waveforms at odd harmonic intervals. The objective of the filter is to attenuate all of the harmonics in the square wave and leave the dc average. Figure 7 below shows the PWM waveform with a 50% duty cycle in the time domain and in the frequency domain. In this design we will use a series of simple RC low pass filters to attenuate the fundamental and the harmonics.

![PWM Signal Fourier Series (Odd Harmonics)](image_url)
Figure 8 below illustrates how a fourth order low pass filter can be used to filter the harmonics in the PWM waveform. Note that the higher frequency harmonics are attenuated to a greater degree. The filter design is covered later in this section.

Figure 8: Attenuation of the harmonics in the PWM with a low pass filter
As a rule of thumb, the cutoff frequency needs to be at least 1 decade lower than the PWM frequency to achieve good attenuation of the fundamental. Using this rule of thumb the fundamental will be attenuated by 20dB for a first order, and 40dB for a second order. We need to determine the filter order required to minimize the ripple to one half of a least significant bit (LSB). Equations (1) to (6) work towards the derivation of a general formula that finds the required filter order to achieve a given resolution. These equations assume that the filter cutoff frequency is set one decade below the PWM frequency.

Resolution = \frac{V_{PWM}}{2^n} \quad (1)

Where:
- **Resolution** is the minimum incremental change in the analog output voltage with a change in PWM duty cycle.
- \( V_{PWM} \) is the amplitude of the PWM signal
- \( n \) is the resolution in bits for the analog signal (12 in this case)

Minimum_Ripple = \frac{\text{Resolution}}{2} = \frac{1}{2} \left( \frac{V_{PWM}}{2^n} \right) \quad (2)

Minimum_Ripple = \frac{1}{2} \left( \frac{V_{PWM}}{2^n} \right) = \frac{1}{2} \left( \frac{3.3V}{2^{12}} \right) = 403μVpp \quad (3)

Where:
- **Minimum_Ripple** is the minimum peak-to-peak amplitude left from the PWM waveform after filtering. Ideally the ripple is zero.

Ripple = \frac{V_{PWM}}{10^{\text{order}}} \quad (4)

Where:
- **Ripple** is the ripple out of the filter assuming the cutoff frequency is one decade lower than the PWM frequency (i.e. \( f_{\text{cutoff}} = \frac{f_{PWM}}{10} \))
- **order** is the filter order (e.g. first order 1/10 or -20dB, second order 1/100 or -40dB)
Substituting (3) into (4), we get Equation (5). Rearranging Equation (5), we get Equation (6). Equation (5) can be used to calculate the required filter order given the PWM resolution. In Equation (7) we determine the order needed for our design (i.e. 4th order filter is needed for a 12 bit PWM).

\[
\frac{V_{PWM}}{10^{\text{order}}} = \frac{1}{2} \left( \frac{V_{PWM}}{2^n} \right)
\]

\[
\text{order} = (n + 1) \log(2)
\]

\[
\text{order} = (n + 1) \log(2) = (12 + 1) \log(2) = 3.91
\]

order = 4 round up to next highest integer to achieve performance better than the goal.

From Equation (7) we determined that a fourth order filter is required for 12 bit PWM. Now we need to select the component values for this filter. A simple first order low pass RC filter is shown in Figure 9. The equation that sets the cutoff frequency is given in Equation (8).

\[
\frac{1}{2\pi f_{\text{cut}}} C_1 = \frac{1}{2\pi(3.91kHz)(470pF)} = 866\Omega
\]

Where:
- \( f_{\text{cut}} = f_{\text{PWM}}/10 = (3.91kHz) / 10 = 391Hz \)
- R1 and C1 = first stage low pass RC filter
- C1 is selected arbitrarily as a standard value. Choose near 1uF as the capacitance in each subsequent stage is divided by 10.
The RC filter will load the microcontroller. The load current is at a maximum when the PWM signal makes a logic level transition (i.e. low to high or high to low). The transient current can be estimated by Equation (9). Using the initial filter values calculated in Equation (9) the transient current is 3.8mA. This is a reasonable load for the MSP430.

\[
I_{\text{transient}} = \frac{V_{\text{cc}}}{R_1} = \frac{3.3V}{866\Omega} = 3.8mA
\]  

(9)

To obtain a higher order filter we can cascade additional stages of the filter. However, it is important to ensure that subsequent stages do not load the initial stage. A simple approach to prevent the loading is to increase the impedance of each subsequent stage by a factor of ten. Equation (10) and (11) show the calculation of the second stage. Subsequent stages follow the same procedure. The final filter is shown in Figure 10.

\[
R_2 = R_1 \times 10 = (866\Omega)(10) = 8.66k\Omega
\]  

(10)

\[
C_2 = \frac{1}{2\pi f_{\text{cut}} R_1} = \frac{1}{2\pi (391\text{Hz})(8.66k\Omega)} = 47nF
\]  

(11)

Figure 10: Cascading four RC Filters for 4<sup>th</sup> Order LPF
Finally, consider the noise contribution of the resistors in the filter. The noise density plot shown in Figure 11 can be used to determine the noise for the filter resistors. The expected noise is 16\textmu Vpp, from Equation (12) and (13), which is significantly less than the required minimum ripple 403\textmu Vpp, so noise is not an issue for this design. However, in other designs (e.g. higher order filter) the noise may be significant.

Figure 11: Noise Spectral Density vs. Resistance

\[ E_{\text{pp}} = 6(e_n)\sqrt{K_n f_{\text{3db}}} \]  
\[ E_{\text{pp}} = 6(100 \text{nV/\sqrt{Hz}})\sqrt{1.57(491\text{Hz})} = 16\text{\mu Vpp} \]
2.3 Filter Post Amplifier Design

The purpose of this design is to filter the PWM signal to a dc voltage that has a ripple that is less than one half the LSB of the required analog output resolution. Equation (14) calculates the minimum ripple to be 403μVpp for this design. Most oscilloscopes have a minimum resolution of 1mV/div and cannot directly measure the filter output ripple. The post amplifier amplifies the ripple to a level where the oscilloscope can measure the ripple to allow confirmation of filter performance.

\[
\text{Minimum_Ripple} = \frac{1}{2} \left( \frac{V_{\text{PWM}}}{2^n} \right) = \frac{1}{2} \left( \frac{3.3V}{2^{12}} \right) = 403\mu\text{Vpp}
\]  

(Equation 14)

**Figure 12** shows the filter post amplifier used to amplify the ripple to a level where it can be easily read by an oscilloscope. The first stage (U1a) has a dc gain of 1 if you consider the capacitor (C5) acts as an open to dc. C5 was selected as a large capacitance (100μF) so that it would act as a short (negligible reactance) at very low frequencies. The cutoff frequency for C5 and R5 is 0.159Hz. So for frequencies above 0.159Hz you can consider C5 a short. For frequencies above 0.159Hz the gain of U1a is 32 (R6/R5 +1). At high frequencies R6 and C6 will attenuate the gain (for f > 513kHz). In summary, U1a amplifies the ac ripple from the filter by a factor of 32 but only amplifies the dc by a factor of 1. This topology was used because the high input impedance of the non-inverting amplifier does not affect the filter.

The filter, C7 and R7, between U1a and U1b is used to ac couple the two stages (i.e. eliminate the dc output of U1a). U1b is a non-inverting amplifier with a gain of 32 (Gain = R9/R8 +1). Thus, the total ac gain of the cascaded amplifier (U1a and U1b) is 1024. In this example we should expect to see less than 412mVpp of ripple on the oscilloscope (403μVpp x 1024 = 412mVpp).

**Figure 12: Post Filter Amplifier for Ripple Verification**

![Post Filter Amplifier for Ripple Verification](image-url)
3 Component Selection

3.1 Passive Component Selection

Standard 1% 100ppm/C resistors and are sufficient for the accuracy required. The capacitors used should be 5% COG or NP0 type for best accuracy and lowest distortion.

3.2 Amplifier Selection

Use a low noise op amp for the post filter amplifier (U1a and U1b) to insure that the noise contributed by the amplifier should be minimal compared to the ripple signal. The OPA2209 (dual OPA209) was used for this design.

4 Simulation

Figure 13 shows the forth order filter used to filter the PWM signal. Figure 14 shows the response of each stage in the filter. The fourth stage has the expected attenuation of 80dB at the PWM frequency.

![Filter Circuit](image)

Figure 13: 12 bit PWM filter design ($f_{\text{cutoff}} = 391\text{Hz}$, 4$^{\text{th}}$ order)

![Frequency Response Graph](image)

Figure 14: Frequency Response for PWM filter (80dB attenuation for 3.91kHz)
Figure 16 shows the ac frequency sweep for the circuit shown in Figure 15. In Figure 16 the Monte Carlo analysis option was also used to show that the gain is reasonably accurate at 3.91kHz (i.e. gain variation is 1020.9 to 1025.6V/V, Ideal Gain = 1024 V/V).
Figure 16: Monte Carlo Analysis for Post Amplifier Frequency Response
Figure 17 shows the total noise for the post amplifier (7.18mVrms). The peak-to-peak noise, at Vout_scope, can be estimated as six times the rms (6 x 7.18mVrms = 43mVpp). The expected ripple amplitude can be calculated from Equation (3) and the post filter amplifier gain to be 412mVpp (403μVpp x 1024 = 412mVpp). Since the output signal is 412mVpp, the 43mVpp of noise should not be a significant error source.

![Figure 17: Total noise (Vrms) at the output of the Post Amplifier](image-url)
Figure 18 shows the TINA-TI™ SPICE circuit used to simulate the entire circuit. Figure 19 shows the expected result out of the filter (386uVpp) and out of the post amplifier (396mV). The post amplifier properly amplifies the ripple with minimal error (see Equation (15)).

Figure 18: TINA-TI™ – Schematic for 12bit system
Figure 19: TINA-TI™ – Schematic for 12bit System Simulation

\[ V_{OUT_SCOPE} = V_{4R} \times G_{POSTAMP} = (386 \mu V_{pp})(1024) = 395.3mV_{pp} \] (15)
4.1 Simulated Results Summary

The simulation results are shown in Table 2 as below.

Table 2: Comparison of Design Goals, Simulation Performance, and Measured Results

<table>
<thead>
<tr>
<th>System Resolution</th>
<th>Goal Max Ripple</th>
<th>Simulated Ideal Components</th>
<th>Measured Results</th>
</tr>
</thead>
<tbody>
<tr>
<td>12bit (filter out)</td>
<td>403uVpp</td>
<td>344.48uVpp</td>
<td>347.66uVpp</td>
</tr>
<tr>
<td>12bit (post amp out)</td>
<td>412mVpp</td>
<td>396mVpp</td>
<td>404mVpp</td>
</tr>
</tbody>
</table>
5 PCB Design

The PCB schematic and Bill of Materials can be found in Appendix A.

5.1 PCB Layout

The general guidelines for precision PCB layout were used on this design. For example, trace lengths are kept to minimum length especially input signals.

Figure 20: PCB Layout
6 Verification & Measured Performance

6.1 Low Pass Filter Ripple Measurement

The ripple of the low pass filter output is in level of uV which cannot be read directly with an oscilloscope. Therefore, the post amplifier is used to amplify the signal to a milivolt level. The test results are shown in Figure 21 as below.

Figure 21: 12bit system resolution with 1024 times gain output ripple
6.2  Post amplifier Filter Frequency Response

Figure 22 illustrates the frequency responses of the post amplifier.

![Graph](image)

Figure 22: Post Amplifier Bandwidth Measurement

6.3  Measured Result Summary

The measurement results are shown in Table 3 as below. Note that the output ripple and cutoff frequencies are close to the goal. The accuracy of the cutoff frequencies is not critical. The main goal is to ensure that the PWM frequency (3.91kHz) is in the passband.

<table>
<thead>
<tr>
<th>System Requirement</th>
<th>Goal</th>
<th>Measurement</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Ripple</td>
<td>412mVpp</td>
<td>404mVpp</td>
</tr>
<tr>
<td>Lower Cutoff Freq (-6dB)</td>
<td>0.125Hz</td>
<td>0.2Hz</td>
</tr>
<tr>
<td>Upper Cutoff Freq (-6dB)</td>
<td>513kHz</td>
<td>400kHz</td>
</tr>
</tbody>
</table>
7 Modifications

This design is for a 12 bit PWM system. The same design methods can be used for higher resolution system; however, you will be confronted with several limitations.

- The higher resolution PWM requires a lower peak-to-peak ripple. This will require an additional filter stage. If you use the same passive filter design, the additional filter stage will have an 8.6MΩ resistor in it. The 8.6M resistor adds excessive intrinsic noise and increases extrinsic noise pick-up. An active filter approach may be a better choice for higher order filters.

- Assuming you are using the same clock for both the high and low resolution PWM signal, the higher resolution PWM signal has a lower PWM frequency than the lower resolution PWM signal. In this example the 12 bit PWM signal had a frequency of 3.91kHz. A 13 bit PWM signal would have a PWM frequency of 1.955kHz (3.91kHz / 2), and a 16 bit PWM frequency would be 244Hz (3.91kHz / (2^4)).

- In this example, we set the cutoff frequency of the PWM filter one decade below the PWM frequency. Additional filter attenuation could be achieved by moving the filter cutoff frequency even lower. If we move the filter two decades below from the PWM frequency the attenuation in decibels will double compared to the current filter. For a fourth order filter the attenuation will change from 80db to 160dB. This is a huge improvement but it makes the PWM update rate very slow (2.4Hz for a 16 bit system).
8 About the Authors

Arthur Kay is an applications engineering manager at TI where he specializes in the support of amplifiers, references, and mixed signal devices. Arthur focuses a good deal on industrial applications such as bridge sensor signal conditioning. Arthur has published a book and an article series on amplifier noise. Before working in applications engineering, he was a semiconductor test engineer for Burr-Brown and Northrop Grumman Corp. Arthur received his MSEE from Georgia Institute of Technology (1993), and BSEE from Cleveland State University (1992).

Andrew Wu (Andrew-wu@ti.com) is a Signal Chain FAA from South China who rotation in the Precision Analog Linear group at Texas Instruments. Prior to joining Texas Instruments, Andrew received his Master and Bachelor from Guilin University of Electronic Technology, major in Communication and Information System.

9 Acknowledgements & References


2. Special thanks to John Caldwell, Collin Wells, and Tim Green for their insight and consultation on PWM operation.
Appendix A.

A.1 Electrical Schematic

Figure A-1: Electrical Schematic
## A.2 Bill of Materials

<table>
<thead>
<tr>
<th>Item #</th>
<th>Quantity</th>
<th>Value</th>
<th>Designator</th>
<th>Footprint</th>
<th>LibRef</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>6</td>
<td>5000</td>
<td>+15V, -15V, S1_IN, S1_OUT, S2_IN, S2_OUT</td>
<td>Keystone5000</td>
<td>5000</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>470n</td>
<td>C1</td>
<td>1210</td>
<td>Capacitor</td>
</tr>
<tr>
<td>3</td>
<td>1</td>
<td>47n</td>
<td>C2</td>
<td>1210</td>
<td>Capacitor</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
<td>4.7n</td>
<td>C3</td>
<td>1210</td>
<td>Capacitor</td>
</tr>
<tr>
<td>5</td>
<td>1</td>
<td>470p</td>
<td>C4</td>
<td>1210</td>
<td>Capacitor</td>
</tr>
<tr>
<td>6</td>
<td>2</td>
<td>NU</td>
<td>C5, C6</td>
<td>1210</td>
<td>Capacitor</td>
</tr>
<tr>
<td>7</td>
<td>2</td>
<td>0.1u</td>
<td>C7, C9</td>
<td>0603</td>
<td>Capacitor</td>
</tr>
<tr>
<td>8</td>
<td>2</td>
<td>10u</td>
<td>C8, C10</td>
<td>1210</td>
<td>Capacitor</td>
</tr>
<tr>
<td>9</td>
<td>2</td>
<td>100u</td>
<td>C11, C13</td>
<td>1210</td>
<td>Capacitor</td>
</tr>
<tr>
<td>10</td>
<td>1</td>
<td>1p</td>
<td>C12</td>
<td>0603</td>
<td>Capacitor</td>
</tr>
<tr>
<td>11</td>
<td>1</td>
<td>10p</td>
<td>C14</td>
<td>0603</td>
<td>Capacitor</td>
</tr>
<tr>
<td>12</td>
<td>6</td>
<td>5001</td>
<td>GND0, GND3, GND4, GND5, GND6, GND7</td>
<td>Keystone5001</td>
<td>5001</td>
</tr>
<tr>
<td>13</td>
<td>4</td>
<td>108-0740-001</td>
<td>GND1, GND2, V+, V-</td>
<td>Johnson_108-0740-001</td>
<td>108-0740-001</td>
</tr>
<tr>
<td>14</td>
<td>4</td>
<td>NY PMS 440 0025 PH</td>
<td>H1, H2, H3, H4</td>
<td>NY PMS 440 0025 PH</td>
<td>NY PMS 440 0025 PH</td>
</tr>
<tr>
<td>15</td>
<td>2</td>
<td>901-143</td>
<td>Input, Output</td>
<td>Amphenol_901-143</td>
<td>901-143</td>
</tr>
<tr>
<td>16</td>
<td>1</td>
<td>TSW-106-07-G-D</td>
<td>J1</td>
<td>TSW-106-07-G-D</td>
<td>TSW-106-07-G-D</td>
</tr>
<tr>
<td>17</td>
<td>1</td>
<td>50</td>
<td>R1</td>
<td>0603</td>
<td>Resistor</td>
</tr>
<tr>
<td>18</td>
<td>1</td>
<td>866</td>
<td>R2</td>
<td>0603</td>
<td>Resistor</td>
</tr>
<tr>
<td>19</td>
<td>1</td>
<td>8.66k</td>
<td>R3</td>
<td>0603</td>
<td>Resistor</td>
</tr>
<tr>
<td>20</td>
<td>1</td>
<td>86.6k</td>
<td>R4</td>
<td>0603</td>
<td>Resistor</td>
</tr>
<tr>
<td>21</td>
<td>1</td>
<td>866k</td>
<td>R5</td>
<td>0603</td>
<td>Resistor</td>
</tr>
<tr>
<td>22</td>
<td>2</td>
<td>NU</td>
<td>R6, R7</td>
<td>0603</td>
<td>Resistor</td>
</tr>
<tr>
<td>23</td>
<td>1</td>
<td>310k</td>
<td>R8</td>
<td>0603</td>
<td>Resistor</td>
</tr>
<tr>
<td>24</td>
<td>2</td>
<td>10k</td>
<td>R9, R10</td>
<td>0603</td>
<td>Resistor</td>
</tr>
<tr>
<td>25</td>
<td>1</td>
<td>1k</td>
<td>R11</td>
<td>0603</td>
<td>Resistor</td>
</tr>
<tr>
<td>26</td>
<td>1</td>
<td>31k</td>
<td>R12</td>
<td>0603</td>
<td>Resistor</td>
</tr>
<tr>
<td>27</td>
<td>1</td>
<td>OPA2209</td>
<td>U1</td>
<td>D0008A_M</td>
<td>OPA2209</td>
</tr>
</tbody>
</table>
Appendix B.

B.1 Adjustable PWM Signal Source

To test our final design we will create an easy to adjust and use PWM signal generator shown in Figure B-1. This generator has adjustable frequency, duty cycle, Voh (output high voltage level), and Vol (output high voltage level). This will allow us to easily test all corner conditions of our specification for our final circuit implementation compliance. Figure B-2 shows the subcircuits used inside of the PWM Macromodel. VCO is a SPICE standard voltage-controlled-oscillator out of which we will use the triangle wave output scaled for 0V to 1V. Frequency is scaled for 1V=1Hz. External to the macromodel, duty cycle is scaled 0V to 100V for 0% to 100% respectively. Internally we scale this from 0 to 1V by VCVS2. An ideal comparator, VCVS1, compares the triangle waveform (0V to 1V) to the duty cycle setting (0V to 1V). The output high and low limits, Voh and Vol, are set externally and become the limit values of U2, a voltage-controlled-voltage source with clamp limits.

Figure B-1: Transient Analysis PWM Source
Figure B-2: PWM Macromodel Details
IMPORTANT NOTICE FOR TI REFERENCE DESIGNS

Texas Instruments Incorporated ("TI") reference designs are solely intended to assist designers ("Buyers") who are developing systems that incorporate TI semiconductor products (also referred to herein as "components"). Buyer understands and agrees that Buyer remains responsible for using its independent analysis, evaluation and judgment in designing Buyer’s systems and products.

TI reference designs have been created using standard laboratory conditions and engineering practices. TI has not conducted any testing other than that specifically described in the published documentation for a particular reference design. TI may make corrections, enhancements, improvements and other changes to its reference designs.

Buyers are authorized to use TI reference designs with the TI component(s) identified in each particular reference design and to modify the reference design in the development of their end products. HOWEVER, NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY THIRD PARTY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT, IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used.

Information published by TI regarding third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI REFERENCE DESIGNS ARE PROVIDED "AS IS". TI MAKES NO WARRANTIES OR REPRESENTATIONS WITH REGARD TO THE REFERENCE DESIGNS OR USE OF THE REFERENCE DESIGNS, EXPRESS, IMPLIED OR STATUTORY, INCLUDING ACCURACY OR COMPLETENESS. TI DISCLAIMS ANY WARRANTY OF TITLE AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, QUIET ENJOYMENT, QUIET POSSESSION, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS WITH REGARD TO TI REFERENCE DESIGNS OR USE THEREOF. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY BUYERS AGAINST ANY THIRD PARTY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON A COMBINATION OF COMPONENTS PROVIDED IN A TI REFERENCE DESIGN. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, SPECIAL, INCIDENTAL, CONSEQUENTIAL OR INDIRECT DAMAGES, HOWEVER CAUSED, ON ANY THEORY OF LIABILITY AND WHETHER OR NOT TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES, ARISING IN ANY WAY OUT OF TI REFERENCE DESIGNS OR BUYER’S USE OF TI REFERENCE DESIGNS.

TI reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques for TI components are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products, Buyers should provide adequate design and operating safeguards.

Reproduction of significant portions of TI information in TI data books, data sheets or reference designs is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards that anticipate dangerous failures, monitor failures and their consequences, lessen the likelihood of dangerous failures and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in Buyer’s safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed an agreement specifically governing such use.

Only those TI components that TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components that have not been so designated is solely at Buyer’s risk, and Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2013, Texas Instruments Incorporated