TI Designs – Precision: Verified Design
Capacitive Load Drive Solution using an Isolation Resistor

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Circuit Description
This design can be used to drive capacitive loads such as cable shields, reference buffers, MOSFET gates, and diodes. The circuit uses an isolation resistor (R_{iso}) to stabilize the output of an op amp. R_{iso} modifies the open loop gain of the system to ensure the circuit has sufficient phase margin. The OPA192 is highlighted because it can drive large capacitive loads using a small isolation resistor.

Design Resources

Design Archive
- All Design files
- SPICE Simulator
- Product Folder
- OPA192
- OPA140
- OPA170
- OPA171
- OPA172
- OPA180
- OPA209
- OPA320
- OPA340
- OPA350
- OPA365

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1 Capacitive Load Drive Solution using an Isolation Resistor

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1 Design Summary

The design requirements are as follows:

- Supply Voltage: 30 V (+/-15 V)
- Capacitive Loads: 100 pF, 1000 pF, 0.01 µF, 0.1 µF, 1 µF

The design goals and performance are summarized in Table 1. Figure 1 depicts the transient response of the OPA192 driving a 0.1 µF load capacitance (C\text{load}) using an isolation resistor (R\text{iso}) of 6.2 Ω to obtain a percent overshoot (PO) of 23.1% and corresponding phase margin (PM) of 45.2°.

<table>
<thead>
<tr>
<th>OPA192</th>
<th>Capacitive Load</th>
<th>100 pF</th>
<th>1000 pF</th>
<th>0.01 µF</th>
<th>0.1 µF</th>
<th>1 µF</th>
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<tr>
<td></td>
<td>Phase Margin</td>
<td>Goal</td>
<td>45°</td>
<td>60°</td>
<td>45°</td>
<td>60°</td>
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<tr>
<td></td>
<td>R\text{iso} (Ω)</td>
<td>47.0</td>
<td>360.0</td>
<td>24.0</td>
<td>100.0</td>
<td>20.0</td>
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<td></td>
<td>Measured Overshoot (%)</td>
<td>23.2</td>
<td>10.4</td>
<td>22.5</td>
<td>9.0</td>
<td>22.1</td>
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<tr>
<td></td>
<td>Calculated PM</td>
<td>45.1°</td>
<td>58.1°</td>
<td>45.8°</td>
<td>59.7°</td>
<td>46.1°</td>
</tr>
</tbody>
</table>

Figure 1: OPA192 Transient Response, C\text{load}=0.1 µF, R\text{iso}=6.2 Ω, PM=45.2°
2 Theory of Operation

Figure 2 depicts a unity-gain buffer driving a capacitive load. Equation (1) shows the transfer function for the circuit in Figure 2. Not depicted in Figure 2 is the open-loop output impedance of the op amp, $R_o$.

\[
T(s) = \frac{1 + C_{load} \times R_{iso} \times s}{1 + (R_o + R_{iso}) \times C_{load} \times s}
\]

The transfer function in Equation (1) has a pole and a zero. The frequency of the pole ($f_p$) is determined by $(R_o + R_{iso})$ and $C_{load}$. $R_{iso}$ and $C_{load}$ determine the frequency of the zero ($f_z$). A stable system is obtained by selecting $R_{iso}$ such that the rate of closure (ROC) between the open loop gain ($A_{ol}$) and $1/\beta$ is 20 dB/decade. [1] Figure 3 depicts the concept. For further information, please consult References [1]-[3]. Note that the $1/\beta$ curve for a unity-gain buffer is 0 dB.

ROC stability analysis is typically simulated. The validity of the analysis depends on multiple factors, especially the accurate modeling of the open-loop output impedance of the amplifier ($R_o$).
In addition to simulating the ROC, a robust stability analysis includes a measurement of the circuit’s percent overshoot and ac gain peaking using a function generator, oscilloscope, and gain/phase analyzer. Phase margin is then calculated from these measurements. Table 2 shows the percent overshoot and ac gain peaking that correspond to phase margins of 45° and 60°. The theory behind these values is in Appendix B and the corresponding software simulation is located in the design file.

### Table 2: Phase Margin vs. Overshoot and AC Gain Peaking

<table>
<thead>
<tr>
<th>Phase Margin</th>
<th>Overshoot (%)</th>
<th>AC Gain Peaking (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>45°</td>
<td>23.3</td>
<td>2.35</td>
</tr>
<tr>
<td>60°</td>
<td>8.8</td>
<td>0.28</td>
</tr>
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### 3 Component Selection

This Precision Design intends to provide $R_{iso}$ values for a variety of op amps and capacitive loads. Table 3 lists the op amps and some of their characteristics. The OPA192 is featured because of its ability to drive large capacitive loads using a small isolation resistor.

### Table 3: Selected Op Amps

<table>
<thead>
<tr>
<th>Op Amp</th>
<th>$V_{supply}$ Range (V)</th>
<th>$I_0$ @ 25°C (max, mA)</th>
<th>$V_{os}$ @ 25°C (max, µV)</th>
<th>$V_{os}$ Drift @ 25°C (max, µV/C)</th>
<th>$V_n$ @ 25°C (max, nV/√Hz)</th>
<th>BW (typ, MHz)</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPA192</td>
<td>4.5 – 36</td>
<td>1.2</td>
<td>25</td>
<td>0.5</td>
<td>5.5</td>
<td>10</td>
<td>RRI/O, Low Noise</td>
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<tr>
<td>OPA140</td>
<td>4.5 – 36</td>
<td>2</td>
<td>120</td>
<td>1</td>
<td>5.1</td>
<td>11</td>
<td>RRI/O, JFET input, Low Noise</td>
</tr>
<tr>
<td>OPA170</td>
<td>2.7 – 36</td>
<td>0.145</td>
<td>1800</td>
<td>2</td>
<td>19</td>
<td>1.2</td>
<td>RRO, Value Line</td>
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<tr>
<td>OPA171</td>
<td>2.7 – 36</td>
<td>0.595</td>
<td>1800</td>
<td>2</td>
<td>14</td>
<td>3.0</td>
<td>RRO, Value Line</td>
</tr>
<tr>
<td>OPA172</td>
<td>4.5 – 36</td>
<td>1.8</td>
<td>1000</td>
<td>1.5</td>
<td>7</td>
<td>10</td>
<td>RRO, Low Power</td>
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<td>OPA180</td>
<td>4.0 – 36</td>
<td>0.525</td>
<td>75</td>
<td>0.35</td>
<td>10</td>
<td>2</td>
<td>RRO, Low Noise, Zero-Drift</td>
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<tr>
<td>OPA209</td>
<td>4.5 – 36</td>
<td>2.5</td>
<td>150</td>
<td>3</td>
<td>2.2</td>
<td>18</td>
<td>RRO, Low Noise</td>
</tr>
<tr>
<td>OPA320</td>
<td>1.8 – 5.5</td>
<td>1.6</td>
<td>150</td>
<td>5</td>
<td>8.5</td>
<td>20</td>
<td>RRI/O, Low Noise</td>
</tr>
<tr>
<td>OPA340</td>
<td>2.7 – 5.5</td>
<td>0.95</td>
<td>500</td>
<td>2.5 (typ)</td>
<td>25</td>
<td>5.5</td>
<td>RRI/O, SR=6V/µs</td>
</tr>
<tr>
<td>OPA350</td>
<td>2.7 – 5.5</td>
<td>7.5</td>
<td>500</td>
<td>4 (typ)</td>
<td>15</td>
<td>38</td>
<td>RRI/O, SR=22V/µs</td>
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<tr>
<td>OPA365</td>
<td>2.2 – 5.5</td>
<td>5</td>
<td>200</td>
<td>1 (typ)</td>
<td>13</td>
<td>50</td>
<td>RRI/O, SR=25V/µs</td>
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</tbody>
</table>
4 Simulation

ROC analysis (or ac analysis) is used to determine an approximate value of $R_{iso}$. Figure 4 depicts the TINA-TI™ schematic topology used in ROC analysis. This topology is thoroughly discussed in [2].

Figure 4: TINA-TI™ Circuit used for ROC Stability Analysis

Figure 5 shows the corresponding ROC analysis of $V_{oa}$ in Figure 4 with SW1 closed. Note that the ROC is ~40 dB/decade and the phase margin is only 8.4°. While a phase margin of 8.4° is technically stable, it is not a robust design. Variation in process and environmental conditions may reduce the phase margin such that the system becomes unstable. Therefore, a phase margin of at least 45° is recommended.

Figure 5: OPA192, $C_{load}=0.1 \mu F$, $R_{iso}=0.0 \Omega$, $PM=8.4^\circ$
Placing a zero at the frequency where $A_{ol}=20$ dB, as shown in Figure 6, adds ~90° of phase margin. [3] Further analysis will refine the location of the zero to reduce the value of $R_{iso}$ while maintaining a stable system.

$$r_{z}=67.04\text{kHz}$$

**Figure 6: Frequency of Zero for Increased Phase Margin**

$R_{iso}$ is calculated as shown in Equation (2).

$$R_{iso} = \frac{1}{2 \times \pi \times f_z \times C_{load}} = \frac{1}{2 \times \pi \times 67.04\text{kHz} \times 0.1\mu\text{F}} = 23.74\Omega$$

(2)

Setting $R_{iso}$ in Figure 4 to 23.7 Ω (nearest 1% standard value) and opening SW1 yields the ROC analysis shown in Figure 7. Notice the ROC and phase margin indicate a stable system.
One drawback to stabilizing capacitive loads using an isolation resistor is dc accuracy. [2] If the op amp is required to supply significant current, a voltage drop will develop across $R_{iso}$. Therefore it is recommended to minimize $R_{iso}$ to increase dc accuracy.

However, reducing $R_{iso}$ will also reduce phase margin. 45° and 60° of phase margin are commonly used in practical designs. [1]

The values of $R_{iso}$ that correspond to phase margins of ~45° and ~60° were determined empirically and are depicted in Figure 8 and Figure 9, respectively.

**Figure 7: OPA192, $C_{load}=0.1 \mu F$, $R_{iso}=23.7 \Omega$, PM=105.5°**
Figure 8: OPA192, $C_{\text{load}}=0.1 \, \mu\text{F}$, $R_{\text{iso}}=4.87 \, \Omega$, PM=44.7°

Figure 9: OPA192, $C_{\text{load}}=0.1 \, \mu\text{F}$, $R_{\text{iso}}=7.15 \, \Omega$, PM=59.5°
Component tolerance also affects the phase margin of the system. The simulation in Figure 10 shows a reduction in phase margin of 1.3° given $R_{iso}$ and $C_{load}$ tolerances of 1% and 5%, respectively. Appendix D contains additional simulations of component tolerance on phase margin.

Figure 10: OPA192, $C_{load}=100$ nF-5%, $R_{iso}=4.87$ Ω-1%, $PM=43.7^\circ$
5 PCB Design

The PCB schematic and bill of materials can be found in Appendix A.

5.1 PCB Layout

The PCB shown in Figure 11 is composed of two layers with signals and power routed on the top layer. The remainder of the top layer was poured with ground copper and stitched to a solid ground plane on the bottom layer. The bottom layer is a solid ground plane to ensure a low impedance path for return currents. General guidelines for PCB layout were followed. For example, input signal trace lengths were kept to a minimum and decoupling capacitors were placed close to the power pins of the device.

![Figure 11: PCB Layout](image-url)
6 Verification & Measured Performance

6.1 Transient Response

Figure 12 shows the transient response to a 10 mVpp step input where \( C_{\text{load}} = 0.1 \ \mu\text{F} \) and \( R_{\text{iso}} = 4.87 \ \Omega \). The overshoot measured at \( V_{\text{opa}} \) is 29.62\%, which corresponds to a phase margin of 39.4\(^\circ\). The equations in Appendix B were used to calculate phase margin given percent overshoot.

\[
\text{Figure 12: OPA192, } C_{\text{load}} = 0.1 \ \mu\text{F}, \ R_{\text{iso}} = 4.87 \ \Omega, \ PM = 39.4^\circ
\]

Many factors can cause this discrepancy, including passive element tolerances, \( A_{\text{ol}} \) and \( R_{\text{o}} \) variation due to process shifts, and measurement/PCB non-idealities.

To achieve a phase margin of \(~45^\circ\), \( R_{\text{iso}} \) was increased to 6.2 \( \Omega \). The resulting transient response is shown in Figure 13.

\[
\text{Figure 13: OPA192, } C_{\text{load}} = 0.1 \ \mu\text{F}, \ R_{\text{iso}} = 6.2 \ \Omega, \ PM = 45.2^\circ
\]
For some scenarios (e.g. large capacitive loads), the magnitude of the input stimulus was reduced until the output response had a waveform similar to Figure 13. For more information, please refer to [4].

6.2 AC Response

Figure 14 depicts the ac response of the OPA192 when $C_{load}=0.1 \ \mu F$ and $R_{iso}=6.2 \ \Omega$. The ac gain peaking is 2.5 dB, which corresponds to a phase margin of 44.2°. These results correlate with the phase margin reported in Figure 8.

![AC Response Graph](image)

Figure 14: OPA192, $C_{load}=0.1 \ \mu F$, $R_{iso}=6.2 \ \Omega$, PM=44.2°
6.3 $R_{\text{iso}}$ vs. $C_{\text{load}}$

Using the described methodology, the values of $R_{\text{iso}}$ that yield phase margins of 45° and 60° for various capacitive loads were determined. The results are shown in Figure 15.

![OPA192 Riso vs. Cload](image)

**Figure 15: OPA192, $R_{\text{iso}}$ vs. $C_{\text{load}}$**

Additional $R_{\text{iso}}$ vs. $C_{\text{load}}$ graphs for various op amps can be found in Appendix C.

It is sometimes desirable to know the phase margin for a capacitive load without $R_{\text{iso}}$ compensation. Figure 16 depicts the phase margin for a variety of capacitive loads where $R_{\text{iso}}=0 \ \Omega$. Note that the OPA192 can deliver reasonable PM for larger capacitive loads than most op amps.

![OPA192 P.M. vs. Cload, Riso=0Ω](image)

**Figure 16: OPA192, PM vs. $C_{\text{load}}$, $R_{\text{iso}}=0 \ \Omega$**
7 Modifications

As mentioned earlier, one drawback to $R_{iso}$ compensation is dc accuracy. One alternative is ‘$R_{iso}$ with dual feedback’ compensation, as shown in Figure 17. This technique has an additional feedback path that corrects for the voltage drop across $R_{iso}$. The design of this compensation technique is discussed in references [1]-[3].

![Figure 17: $R_{iso}$ with Dual Feedback](image)

8 About the Authors

Pete Semig is an Analog Applications Engineer in the Precision Linear group at Texas Instruments. He supports Texas Instruments’ difference amplifiers & instrumentation amplifiers. Prior to joining Texas Instruments in 2007, he earned his B.S.E.E. and M.S.E.E. from Michigan State University in 1998 & 2001, respectively. From 2001-2007 he was a faculty member in Michigan State University’s Department of Electrical & Computer Engineering where he taught a variety of courses and laboratories.

Timothy Claycomb was an intern for the Precision Linear group at Texas Instruments. He currently is an undergraduate student pursuing a B.S. in Electrical Engineering at Michigan State University and will graduate in December of 2013.
9 Acknowledgements & References

The authors would like to acknowledge Collin Wells and Mike Mock for their technical contributions to this design.


A.1 Electrical Schematic

Figure A-1: Electrical Schematic
# A.2 Bill of Materials

<table>
<thead>
<tr>
<th>QTY</th>
<th>Designator</th>
<th>Value</th>
<th>Description</th>
<th>Manufacturer</th>
<th>Manufacturer PN</th>
<th>DigiKey PN</th>
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<td>1</td>
<td>U1</td>
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<td>Texas Instruments</td>
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<td></td>
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<td>2</td>
<td>Riso</td>
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<td>RES, 0.25W, 1206</td>
<td>Various</td>
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<td>3</td>
<td>Cloud</td>
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<td>CAP, CERM, 1206</td>
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<td>5006</td>
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<td>9</td>
<td>R2</td>
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<td>R1</td>
<td>40.2</td>
<td>RES, 40.2 ohm, 1%, 0.25W, 1206</td>
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<td>2205K-ND</td>
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</table>

Figure A-2: Bill of Materials
Appendix B.

B.1 Percent Overshoot and AC Gain Peaking vs. Phase Margin

Percent overshoot and ac gain peaking are related to phase margin ($\phi_m$) via damping ratio ($\zeta$). Equation (3) and Figure 18 depict the relationship between $\zeta$ and phase margin.

$$\phi_m(\zeta) := \frac{180}{\pi} \arctan \left( 2 \cdot \zeta \left( \frac{1}{\sqrt{4 \cdot \zeta^4 + 1 - 2 \cdot \zeta^2}} \right) \right)$$

(3)

where

$$\zeta := 0.0, 0.001..0.707$$

(4)

![Figure 18: Damping Ratio vs. Phase Margin](image)
Percent overshoot and ac gain peaking relate to phase margin as shown by Equation(5), Equation (6), and Figure 19.

\[
PO(\zeta) := 100 \cdot \exp \left( \frac{-1\pi \cdot \zeta}{\sqrt{1 - \zeta^2}} \right) 
\]

\[
GP(\zeta) := 20 \cdot \log \left( 2 \cdot \frac{Q(\zeta)^2}{\sqrt{4 \cdot Q(\zeta)^2 - 1}} \right)
\]

where

\[
Q(\zeta) := \frac{1}{2 \zeta}
\]

Figure 19: PO and GP vs. Phase Margin

Calculate percent overshoot and ac gain peaking (in dB) for 45° of phase margin as follows:

Given \( \zeta := 0 \)

\[
\frac{180}{\pi} \cdot \text{atan} \left[ 2 \cdot \zeta \left( \frac{1}{\sqrt{4 \cdot \zeta^4 + 1 - 2 \zeta^2}} \right) \right] = 45
\]

\[
\zeta_{45} := \text{Find} \zeta \quad \zeta_{45} = 0.42
\]

\[
PO_{45} := 100 \cdot \exp \left( \frac{-\pi \cdot \zeta_{45}}{\sqrt{1 - \zeta_{45}^2}} \right) = 23.321
\]

\[
GP_{45} := 20 \cdot \log \left( 2 \cdot \frac{Q(\zeta_{45})^2}{\sqrt{4 \cdot Q(\zeta_{45})^2 - 1}} \right) = 2.35
\]

Repeat the calculations to determine percent overshoot and ac gain peaking for 60° of phase margin.
B.2 Phase Margin vs. Percent Overshoot

After measuring the percent overshoot of a transient analysis, Equations 13 to 15 can be used to calculate the corresponding phase margin.

\[
PO := 23.321
\]

\[
\zeta := \frac{-\ln \left( \frac{PO}{100} \right)}{\sqrt{\frac{2}{\pi} + \left( \ln \left( \frac{PO}{100} \right) \right)^2}} = 0.42
\]

\[
\phi_{\text{PM}} := \frac{180}{\pi} \text{atan} \left( \frac{2\zeta}{\sqrt{4\zeta^4 + 1 - 2\zeta^2}} \right) = 45
\]
Appendix C.

All measured data values can be found in the design file archive. If no data points exist for 100pF scenario, the amplifier does not require an isolation resistor for stable operation. If no data points exist for 1µF scenario, the isolation resistor required for stable operation is less than 1 Ω.

C.1 OPA140

![OPA140 Riso vs. Cload](image1)

Figure 20: OPA140, $R_{iso}$ vs. $C_{load}$

C.2 OPA170

![OPA170 Riso vs. Cload](image2)

Figure 21: OPA170, $R_{iso}$ vs. $C_{load}$
C.3  OPA171

Figure 22: OPA171, $R_{iso}$ vs. $C_{load}$

C.4  OPA172

Figure 23: OPA172, $R_{iso}$ vs. $C_{load}$
C.5 OPA180

Figure 24: OPA180, $R_{iso}$ vs. $C_{load}$

C.6 OPA209

Figure 25: OPA209, $R_{iso}$ vs. $C_{load}$
C.7 OPA320

![OPA320 Riso vs. Cload](image1)

**Figure 26**: OPA320, $R_{iso}$ vs. $C_{load}$

C.8 OPA340

![OPA340 Riso vs. Cload](image2)

**Figure 27**: OPA340, $R_{iso}$ vs. $C_{load}$
C.9 OPA350

**Figure 28: OPA350, $R_{iso}$ vs. $C_{load}$**

C.10 OPA365

**Figure 29: OPA365, $R_{iso}$ vs. $C_{load}$**
Appendix D. Passive Tolerance Simulations

Figure 30: OPA192, \( C_{\text{load}} = 100 \text{ nF} + 5\% \), \( R_{\text{iso}} = 4.87 \, \Omega - 1\% \), \( \text{PM} = 44.94^\circ \)

Figure 31: OPA192, \( C_{\text{load}} = 100 \text{ nF} - 5\% \), \( R_{\text{iso}} = 4.87 \, \Omega + 1\% \), \( \text{PM} = 44.36^\circ \)
Figure 32: OPA192, $C_{load}=100 \text{ nF} \pm 5\%$, $R_{iso}=4.87 \pm 1\%$, $PM=45.63^\circ$
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