This user's guide describes the features and operation of the bq24650EVM Evaluation Module (EVM). The EVM assists users in evaluating the bq24650 synchronous battery charger. The EVM is also called the HPA639 A. The manual includes the bq24650EVM bill of materials, board layout, and schematic.
1 Introduction

1.1 Features

- Synchronous switch-mode battery charge controller for solar power
- Resistor-programmable up to 26-V battery voltage
- Input operating range: 5 V–28 V
- LED indication for charge status
- Test points for key signals available for testing purposes; easy probe hook-up.
- Jumpers available; easy-to-change setting

1.2 General Description

The bq24650 is a highly integrated switch-mode battery charge controller. It provides input voltage regulation, which reduces charge current when input voltage falls below a programmed level. When the input is powered by a solar panel, the input regulation loop maintains the panel at maximum power output.

The bq24650 offers a constant-frequency, synchronous PWM controller with high-accuracy current and voltage regulation, charge preconditioning, charge termination, and charge status monitoring.

The bq24650 changes the battery in three phases: preconditioning, constant current, and constant voltage. Charge is terminated when the current reaches one-tenth of the fast charge rate. A programmable fast-charge timer provides a safety backup. The precharge timer is fixed at 30 minutes. The bq24650 automatically restarts the charge cycle if the battery voltage falls below an internal threshold and enters a low, quiescent-current sleep mode when the input voltage falls below the battery voltage.

The bq24650 supports the battery from 2.1 V to 26 V with VFB set to a 2.1-V feedback reference. The charge current is programmed by selecting an appropriate sense resistor. The bq24650 is available in a 16-pin, 3.5x3.5 mm², thin QFN package.

For details, see the bq24650 data sheet (SLUSA75).

1.3 I/O Description

Table 1. I/O Description

<table>
<thead>
<tr>
<th>Jack</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>J1–VIN</td>
<td>Positive input</td>
</tr>
<tr>
<td>J1–PGND</td>
<td>Negative input</td>
</tr>
<tr>
<td>J2–VSYS</td>
<td>Connected to system</td>
</tr>
<tr>
<td>J2–VOUT</td>
<td>Connected to charger output</td>
</tr>
<tr>
<td>J2–PGND</td>
<td>Ground</td>
</tr>
<tr>
<td>J2–TS</td>
<td>Temperature qualification voltage input</td>
</tr>
</tbody>
</table>
1.4 Control and Key Parameters Settings

Table 2. Control and Key Parameters Settings

<table>
<thead>
<tr>
<th>Jack</th>
<th>Description</th>
<th>Factory Setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>JP1</td>
<td>Select external TS input or internal valid TS setting</td>
<td>Jumper ON 1-2 (external TS)</td>
</tr>
<tr>
<td></td>
<td>1-2 : External TS input</td>
<td></td>
</tr>
<tr>
<td></td>
<td>2-3 : Internal valid TS setting</td>
<td></td>
</tr>
<tr>
<td>JP2</td>
<td>The pullup power source supplies the LEDs when JP2 ON. LED has no power</td>
<td>Jumper ON (LED power available)</td>
</tr>
<tr>
<td></td>
<td>source when JP2 is OFF.</td>
<td></td>
</tr>
<tr>
<td>JP3</td>
<td>TERM_EN setting</td>
<td>Jumper ON 2-3 (enable termination)</td>
</tr>
<tr>
<td></td>
<td>2-3 : Connect TERM_EN to VREF to enable termination</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1-2 : Connect TERM_EN to GND to disable termination</td>
<td></td>
</tr>
<tr>
<td>JP4</td>
<td>Charger enable/disable setting. MPPSET is pulled to GND and the charger</td>
<td>Jumper OFF (disable charger)</td>
</tr>
<tr>
<td></td>
<td>is disabled when JP4 OFF; charger is enabled when JP4 is ON.</td>
<td></td>
</tr>
</tbody>
</table>

1.5 Recommended Operating Conditions

Table 3. Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage, $V_{IN}$</td>
<td>Input voltage</td>
<td>5</td>
<td>20</td>
<td>28</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Battery voltage, $V_{OUT}$</td>
<td>Voltage applied at VOUT terminal of J2</td>
<td>2.1</td>
<td>12.6</td>
<td>26</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Supply current</td>
<td>Maximum input current</td>
<td>0</td>
<td>8</td>
<td></td>
<td>A</td>
<td></td>
</tr>
<tr>
<td>Charge current, $I_{CHG}$</td>
<td>Battery charge current</td>
<td>0</td>
<td>2</td>
<td>8</td>
<td>A</td>
<td>For charge current above 2 A, replace R6 and L1 with high-current rating components</td>
</tr>
<tr>
<td>Operating junction temperature range, $T_J$</td>
<td></td>
<td>0</td>
<td>125</td>
<td></td>
<td>°C</td>
<td></td>
</tr>
</tbody>
</table>

The bq24650EVM board requires a regulated supply approximately 1 V minimum above the regulated voltage of the battery pack to a maximum input voltage of 28 Vdc. The charge voltage is programmed via a resistor divider from the battery to ground, with the midpoint tied to the VFB pin.

R13 and R15 can be changed to regulate output between approximately 2.1 V to 26 V.

\[
V_{OUT} = 2.1 \times \left(1 + \frac{R_{13}}{R_{15}}\right)
\]

(1)

It is set at 12.6 Vdc from the factory.

A solar panel has a unique point on the V-I or V-P curve, called the maximum power point (MPP), at which the entire photovoltaic (PV) system operates with maximum efficiency and produces its maximum output power. The constant voltage algorithm is the simplest maximum power point tracking (MPPT) method. The bq24650 automatically reduces charge current, so the maximum power point is maintained for maximum efficiency.

If the solar panel or other input source cannot provide the total power of the system and bq24650 charger, the input voltage drops. Once the voltage sensed on the MPPSET pin drops below 1.2 V, the charger maintains the input voltage by reducing the charge current.

\[
V_{MPPSET} = 1.2 \times \left(1 + \frac{R_{17}}{R_{19}}\right)
\]

(2)

It is set at 17.8 Vdc from the factory.
Battery current is sensed by resistor RSR connected between SRP and SRN. The full-scale differential voltage between SRP and SRN is fixed at 40 mV.

\[ I_{\text{CHARGE}} = \frac{40 \text{ mV}}{R_6} \]  

(3)

It is set at 2 Adc from the factory.
2 Test Summary

2.1 Definitions

This procedure details how to configure the HPA639 A evaluation board. The following naming conventions are followed on the test procedure.

VXXX : External voltage supply name (VADP, VBT, VSBT)
LOADW: External load name (LOADR, LOADI)
V(TPyyy): Voltage at internal test point TPyyy. For example, V(TP1) means the voltage at TP1.
V(jxx): Voltage at jack terminal Jxx.
V(TP(XXX)): Voltage at test point XXX. For example, V(MPPSET) means the voltage at the test point which is marked as MPPSET.
V(XXX, YYY): Voltage across point XXX and YYY.
I(JXX(YYY)): Current going out from the YYY terminal of jack XX.
Jxx(BBB): Terminal or pin BBB of jack xx
Jxx ON : Internal jumper Jxx terminals are shorted
Jxx OFF: Internal jumper Jxx terminals are open
Jxx (-YY-) ON: Internal jumper Jxx adjacent terminals marked as YY are shorted
Measure: → A,B Check specified parameters A, B. If measured values are not within specified limits the unit under test has failed.
Observe: → A,B Observe if A, B occur. If they do not occur, the unit under test has failed.

Assembly drawings have location for jumpers, test points and individual components.

2.2 Safety

1. Safety Glasses are to be worn.
2. This test must be performed by qualified personnel who are trained in electronics theory and understand the risks and hazards of the assembly to be tested.
3. ESD precautions must be followed while handling electronic assemblies and performing this test.
4. Precautions must be observed to avoid touching areas of the assembly that may get hot or present a shock hazard during testing.

2.3 Quality

1. Test data can be made available on request from Texas Instruments.

2.4 Apparel

1. Electrostatic smock
2. Electrostatic gloves or finger cots
3. Safety glasses
4. Ground ESD wrist strap.

2.5 Equipment

2.5.1 Power Supplies

Power Supply #1 (PS#1): a power supply capable of supplying 30 V at 3 A is required.
2.5.2  Loads

LOAD#1 A 30-V (or greater), 5-A (or greater) electronic load that can operate at constant current and constant voltage mode.

LOAD#2: An HP 6060B 3-V to 60-V/0A to 60-A, 300-W system dc electronic load or equivalent.

2.5.3  Meters

Seven Fluke 75 multimeters (equivalent or better) or four equivalent voltage meters and three equivalent current meters.

The current meters must be capable of measuring 5-A+ current.

2.6  Equipment Setup

1. Set the power supply #1 (PS#1) for 21-V ±500-mVdc, 2.5-A ±0.1-A current limit, and then turn off supply.
2. Connect the output of PS#1 in series with a current meter (multimeter) to J1 (VIN, PGND).
3. Connect a voltage meter across J1 (VIN, PGND).
4. Connect Load#1 in series with a current meter to J2 (VOUT, PGND). Turn off Load#1.
5. Connect Load#2 in series with a current meter to J2 (VSYS, PGND). Turn off Load#2.
6. Connect a voltage meter across J2 (VOUT, PGND).
7. Connect a voltage meter across J2 (VSYS, PGND).
8. Check all jumper shunts. JP1: connect 1-2 (External TS); JP2: ON; JP3: connect 2-3 (Enable TERM_EN); JP4: OFF.

Figure 1. Original Test Setup for HPA639 A Evaluation Board
2.7 Procedure

2.7.1 Power Supply and VREF

Ensure that Section 2.6 steps are followed.

Disconnect LOAD#1#2. Turn on PS#1.

Measure → V(J2(VSYS)) = 21 V ± 500 mV
Measure → V(J2(VOUT)) = 0 V ± 500 mV
Measure → V(TP(VREF)) = 3.3 V ± 200 mV
Measure → V(TP(REGN)) = 0 V ± 200 mV

2.7.2 Charger Enable and Battery Detection

Connect 2-3 of JP1 (Internal TS); Short JP4 (Charger Enable)

Measure → V(TP(VREF)) = 3.3 V ± 200 mV
Measure → V(TP(REGN)) = 6 V ± 200 mV
Observe → V(J2(VOUT))=12.6 V ±500 mV
Observe → D4 (/STAT1) OFF, D5 (/STAT2) OFF

2.7.3 Charge Current/Voltage Regulation and Battery Temperature Qualification

Reconnect LOAD#2, and turn on. Use the constant voltage mode. Set the output voltage to 8 V.

Measure → I(J2(VOUT)) = 0.2 A ±100 mA
Observe → D4 (/STAT1) ON, D5 (/STAT2) OFF

Increase the voltage of LOAD#2 to be 10.5 V.

Measure → I(J2(VOUT)) = 2 A ±200 mA
Observe → D4 (/STAT1) ON, D5 (/STAT2) OFF

Open 2-3 of JP1

Measure → I(J2(VOUT)) = 0 A ±100 mA
Observe → D4 (/STAT1) OFF, D5 (/STAT2) OFF

Connect 2-3 of JP1 (Internal TS)

Measure → I(J2(VOUT)) = 2 A ±200 mA
Observe → D4 (/STAT1) ON, D5 (/STAT2) OFF

2.7.4 Charger Termination

Increase the voltage of LOAD#2 slowly to approximately 12.6 V.

Observe → I(J2(VOUT)) decreases from 2 A while V(J2(VOUT)) becomes constant.
Observe → I(J2(VOUT)) drops to zero when it is less than 0.2 A.

2.7.5 Maximum Power Point, Input Voltage Regulation

Connect the output of the Load#1 in series with a current meter (multimeter) to J2 (SYS, PGND). Ensure that a voltage meter is connected across J2 (SYS, PGND). Resume other status as in Section 2.7.3. (Short JP1, JP4, set LOAD#2 to 10.5 V.)
2.7.6 Final Step

Turn on the power of Load#1. Set the load current to 1 A. Increase the load current slowly and observe the following.

\[ V(J1(VIN)) = 17.8 \text{ V} \pm 500 \text{ mV.} \]

Keep increasing \( I(J2(VSYS)) \).

\[ I(J2(VOUT)) \] decreases from 2 A toward 0 A while \( V(J1(VIN)) \) become constant 17.8 V \( \pm 500 \text{ mV.} \) Ensure that \( I(J2(VOUT)) = 0 \text{ A} \pm 100 \text{ mA} \) and \( (J2(VSYS)) = 2.4 \text{ A} \pm 200 \text{ mA.} \)

2.7.7 Test Complete

Turn off the power supply, and remove all connections from the unit under test.
3 PCB Layout Guideline

1. It is critical that the exposed thermal pad on the backside of the bq24650 package be soldered to the PCB ground. Ensure that sufficient thermal vias are right underneath the IC, connecting to the ground plane on the other layers.

2. The control stage and the power stage must be routed separately. At each layer, the signal ground and the power ground are connected only at the thermal pad.

3. Charge current sense resistor must be connected to SRP, SRN with a Kelvin contact. The area of this loop must be minimized. The decoupling capacitors for these pins must be placed as close to the IC as possible.

4. Decoupling capacitors for VREF, VCC, REGN must make the interconnections to the IC as short as possible.

5. Decoupling capacitors for BAT must be placed close to the corresponding IC pins, and make the interconnections to the IC as short as possible.

6. Decoupling capacitor(s) for the charger input must be placed close to the Q1A drain and Q1B source.

7. Take the EVM layout for design reference.
# Bill of Materials, Board Layout, and Schematic

## 4 Bill of Materials, Board Layout, and Schematic

### 4.1 Bill of Materials

<table>
<thead>
<tr>
<th>RefDes</th>
<th>Value</th>
<th>Description</th>
<th>SIZE</th>
<th>PART NUMBER</th>
<th>MFR</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1, C2, C7</td>
<td>10 µF</td>
<td>Capacitor, Ceramic, 35V, X7R, 10%</td>
<td>1210</td>
<td>STD</td>
<td>STD</td>
</tr>
<tr>
<td>C3, C5, C8</td>
<td>1.0 µF</td>
<td>Capacitor, Ceramic, 35V, X7R, 10%</td>
<td>805</td>
<td>STD</td>
<td>STD</td>
</tr>
<tr>
<td>C4</td>
<td>2.2 µF</td>
<td>Capacitor, Ceramic, 35V, X7R, 20%</td>
<td>1210</td>
<td>STD</td>
<td>STD</td>
</tr>
<tr>
<td>C6, C11, C12</td>
<td>0.1 µF</td>
<td>Capacitor, Ceramic, 50V, X7R, 10%</td>
<td>603</td>
<td>STD</td>
<td>STD</td>
</tr>
<tr>
<td>C9, C13</td>
<td>Open</td>
<td>Capacitor, Ceramic, 50V, X7R, 10%</td>
<td>603</td>
<td>STD</td>
<td>STD</td>
</tr>
<tr>
<td>C10, C16</td>
<td>1.0 µF</td>
<td>Capacitor, Ceramic, 16V, X7R, 10%</td>
<td>805</td>
<td>STD</td>
<td>STD</td>
</tr>
<tr>
<td>C14</td>
<td>0.1 µF</td>
<td>Capacitor, Ceramic, 16V, X7R, 10%</td>
<td>603</td>
<td>STD</td>
<td>STD</td>
</tr>
<tr>
<td>C15, C17</td>
<td>22 pF</td>
<td>Capacitor, Ceramic, 50V, X7R, 10%</td>
<td>603</td>
<td>STD</td>
<td>STD</td>
</tr>
<tr>
<td>D1, D3</td>
<td>PowerDi 5</td>
<td>Diode, 10A 40V Schottky Barrier Rectifier</td>
<td>PDS1040-13</td>
<td>Diodes</td>
<td></td>
</tr>
<tr>
<td>D2</td>
<td>ZLSS350-7</td>
<td>Diode, Schottky, 1.16A, 40-V</td>
<td>SOD-523</td>
<td>Zetex</td>
<td></td>
</tr>
<tr>
<td>D4, D5</td>
<td>LTST-C190GKT</td>
<td>Diode, LED, Green, 2.1V, 20mA, 6mcd</td>
<td>603</td>
<td>Lite On</td>
<td></td>
</tr>
<tr>
<td>J1</td>
<td>ED120/2DS</td>
<td>Terminal Block, 2 pin, 15A, 5.1mm</td>
<td>0.40 x 0.35 inch</td>
<td>Sullins</td>
<td></td>
</tr>
<tr>
<td>J2</td>
<td>ED120/4DS</td>
<td>Terminal Block, 4 pin, 15A, 5.1mm</td>
<td>0.80 x 0.35 inch</td>
<td>OST</td>
<td></td>
</tr>
<tr>
<td>JP2, JP4</td>
<td>PEC02SAAN</td>
<td>Header, 2 pin, 100mil spacing</td>
<td>0.100 inch x 2</td>
<td>Sullins</td>
<td></td>
</tr>
<tr>
<td>JP1, JP3</td>
<td>PEC03SAAN</td>
<td>Header, 3 pin, 100mil spacing</td>
<td>0.100 inch x 3</td>
<td>Sullins</td>
<td></td>
</tr>
<tr>
<td>L1</td>
<td>IHLPS25SCZER100M01</td>
<td>Inductor, SMT, 102m, 7.0A, 20%</td>
<td>0.255 x 0.270 inch</td>
<td>Vishay</td>
<td></td>
</tr>
<tr>
<td>Q1</td>
<td>N57288-T1</td>
<td>FET, Dual N Chan, 40V, 20A, 19 mΩ</td>
<td>SOT8-PowerPak</td>
<td>Siliconix</td>
<td></td>
</tr>
<tr>
<td>Q2</td>
<td>N7002-7-F</td>
<td>MOSFET, N-ch, 60V, 115mA, 1.2Ω</td>
<td>2N7002-7-F</td>
<td>Diodes</td>
<td></td>
</tr>
<tr>
<td>R1, R2</td>
<td>1206</td>
<td>Resistor, Chip, 1/4W, 5%</td>
<td>STD</td>
<td>STD</td>
<td></td>
</tr>
<tr>
<td>R3</td>
<td>805</td>
<td>Resistor, Chip, 1/8W, 5%</td>
<td>STD</td>
<td>STD</td>
<td></td>
</tr>
<tr>
<td>R4, R8</td>
<td>805</td>
<td>Resistor, Chip, 1/8W, 5%</td>
<td>STD</td>
<td>STD</td>
<td></td>
</tr>
<tr>
<td>R5</td>
<td>603</td>
<td>Resistor, Chip, 1/10W, 5%</td>
<td>STD</td>
<td>STD</td>
<td></td>
</tr>
<tr>
<td>R6</td>
<td>1206</td>
<td>Resistor, Metal Film, 1/4 watt, 0.1%, Axial</td>
<td>WSLP1206R0200FEA</td>
<td>Vishay</td>
<td></td>
</tr>
<tr>
<td>R7, R10</td>
<td>603</td>
<td>Resistor, Chip, 1/10W, 5%</td>
<td>STD</td>
<td>STD</td>
<td></td>
</tr>
<tr>
<td>R9</td>
<td>603</td>
<td>Resistor, Chip, 1/10W, 1%</td>
<td>STD</td>
<td>STD</td>
<td></td>
</tr>
<tr>
<td>R11</td>
<td>603</td>
<td>Resistor, Chip, 1/10W, 5%</td>
<td>STD</td>
<td>STD</td>
<td></td>
</tr>
<tr>
<td>R12</td>
<td>603</td>
<td>Resistor, Chip, 1/10W, 1%</td>
<td>STD</td>
<td>STD</td>
<td></td>
</tr>
<tr>
<td>R13, R17</td>
<td>603</td>
<td>Resistor, Chip, 1/10W, 1%</td>
<td>STD</td>
<td>STD</td>
<td></td>
</tr>
<tr>
<td>R14</td>
<td>603</td>
<td>Resistor, Chip, 1/10W, 5%</td>
<td>STD</td>
<td>STD</td>
<td></td>
</tr>
<tr>
<td>R15, R18</td>
<td>603</td>
<td>Resistor, Chip, 1/10W, 1%</td>
<td>STD</td>
<td>STD</td>
<td></td>
</tr>
<tr>
<td>R16</td>
<td>603</td>
<td>Resistor, Chip, 1/10W, 5%</td>
<td>STD</td>
<td>STD</td>
<td></td>
</tr>
<tr>
<td>R20, R21</td>
<td>603</td>
<td>Resistor, Chip, 1/10W, 1%</td>
<td>STD</td>
<td>STD</td>
<td></td>
</tr>
<tr>
<td>R19</td>
<td>603</td>
<td>Resistor, Chip, 1/10W, 5%</td>
<td>STD</td>
<td>STD</td>
<td></td>
</tr>
<tr>
<td>TP1, TP3–TP7</td>
<td>0.020”</td>
<td>Test Point, 0.020 Hole</td>
<td>STD</td>
<td>STD</td>
<td></td>
</tr>
<tr>
<td>TP2</td>
<td>0.200 inch</td>
<td>Test Point, White, Thru Hole Color Keyed</td>
<td>131-5031-00</td>
<td>Tektronix</td>
<td></td>
</tr>
<tr>
<td>U1</td>
<td>BQ24650RVA</td>
<td>IC, High Efficiency Synchronous Switch-Mode Fast Charge Controller for Solar Power</td>
<td>QFN16[RVA]</td>
<td>TI</td>
<td></td>
</tr>
<tr>
<td>CE, GND, MPPSET, REGN, STAT1, STAT2, TS, TERM, EN, VCC, VREF</td>
<td>TP-5002</td>
<td>Test Point, White, Thru Hole Color Keyed</td>
<td>0.100 x 0.100 inch</td>
<td>5002</td>
<td>Keystone</td>
</tr>
<tr>
<td>–</td>
<td>HPA639</td>
<td>PCB, 3 ln x 3 ln x 0.062 ln</td>
<td>Any</td>
<td>3M</td>
<td></td>
</tr>
<tr>
<td>–</td>
<td>SJ-5303</td>
<td>Bumper foot (install after final wash)</td>
<td>0.440 x 0.2</td>
<td>3M</td>
<td></td>
</tr>
<tr>
<td>–</td>
<td>929950-00</td>
<td>Shunt, 100-mil, Black</td>
<td>0.100</td>
<td>3M</td>
<td></td>
</tr>
</tbody>
</table>
4.2 Board Layout

Figure 2. Top Layer
Figure 3. Second Layer
Figure 4. Third Layer
Figure 5. Bottom Layer
Figure 7. Bottom Assembly
Figure 8. bq24650EVM Schematic
**Evaluation Board/Kit Important Notice**

Texas Instruments (TI) provides the enclosed product(s) under the following conditions:

This evaluation board/kit is intended for use for ENGINEERING DEVELOPMENT, DEMONSTRATION, OR EVALUATION PURPOSES ONLY and is not considered by TI to be a finished end-product fit for general consumer use. Persons handling the product(s) must have electronics training and observe good engineering practice standards. As such, the goods being provided are not intended to be complete in terms of required design-, marketing-, and/or manufacturing-related protective considerations, including product safety and environmental measures typically found in end products that incorporate such semiconductor components or circuit boards. This evaluation board/kit does not fall within the scope of the European Union directives regarding electromagnetic compatibility, restricted substances (RoHS), recycling (WEEE), FCC, CE or UL, and therefore may not meet the technical requirements of these directives or other related directives.

Should this evaluation board/kit not meet the specifications indicated in the User’s Guide, the board/kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE.

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies TI from all claims arising from the handling or use of the goods. Due to the open construction of the product, it is the user’s responsibility to take any and all appropriate precautions with regard to electrostatic discharge.

EXCEPT TO THE EXTENT OF THE INDEMNITY SET FORTH ABOVE, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

TI currently deals with a variety of customers for products, and therefore our arrangement with the user is not exclusive.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein.

Please read the User’s Guide and, specifically, the Warnings and Restrictions notice in the User’s Guide prior to handling the product. This notice contains important safety information about temperatures and voltages. For additional information on TI’s environmental and/or safety programs, please contact the TI application engineer or visit www.ti.com/esh.

No license is granted under any patent right or other intellectual property right of TI covering or relating to any machine, process, or combination in which such TI products or services might be or are used.

**FCC Warning**

This evaluation board/kit is intended for use for ENGINEERING DEVELOPMENT, DEMONSTRATION, OR EVALUATION PURPOSES ONLY and is not considered by TI to be a finished end-product fit for general consumer use. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

**EVM Warnings and Restrictions**

It is important to operate this EVM within the input voltage range of 18 V to 22 V and the output voltage range of 0 V to 18 V. Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60°C. The EVM is designed to operate properly with certain components above 125°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2010, Texas Instruments Incorporated
IMPORTANT NOTICE FOR TI REFERENCE DESIGNS

Texas Instruments Incorporated (“TI”) reference designs are solely intended to assist designers (“Buyers”) who are developing systems that incorporate TI semiconductor products (also referred to herein as “components”). Buyer understands and agrees that Buyer remains responsible for using its independent analysis, evaluation and judgment in designing Buyer’s systems and products.

TI reference designs have been created using standard laboratory conditions and engineering practices. TI has not conducted any testing other than that specifically described in the published documentation for a particular reference design. TI may make corrections, enhancements, improvements and other changes to its reference designs.

Buyers are authorized to use TI reference designs with the TI component(s) identified in each particular reference design and to modify the reference design in the development of their end products. HOWEVER, NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY THIRD PARTY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT, IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used.

Information published by TI regarding third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI REFERENCE DESIGNS ARE PROVIDED “AS IS”. TI MAKES NO WARRANTIES OR REPRESENTATIONS WITH REGARD TO THE REFERENCE DESIGNS OR USE OF THE REFERENCE DESIGNS, EXPRESS, IMPLIED OR STATUTORY, INCLUDING ACCURACY OR COMPLETENESS. TI DISCLAIMS ANY WARRANTY OF TITLE AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, QUIET ENJOYMENT, QUIET POSSESSION, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS WITH REGARD TO TI REFERENCE DESIGNS OR USE THEREOF. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY BUYERS AGAINST ANY THIRD PARTY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON A COMBINATION OF COMPONENTS PROVIDED IN A TI REFERENCE DESIGN, IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, SPECIAL, INCIDENTAL, CONSEQUENTIAL OR INDIRECT DAMAGES, HOWEVER CAUSED, ON ANY THEORY OF LIABILITY AND WHETHER OR NOT TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES, ARISING IN ANY WAY OUT OF TI REFERENCE DESIGNS OR BUYER’S USE OF TI REFERENCE DESIGNS.

TI reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques for TI components are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

Reproduction of significant portions of TI information in TI data books, data sheets or reference designs is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards that anticipate dangerous failures, monitor failures and their consequences, lessen the likelihood of dangerous failures and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in Buyer’s safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed an agreement specifically governing such use.

Only those TI components that TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components that have not been so designated is solely at Buyer’s risk, and Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2013, Texas Instruments Incorporated