Chapter 1
TIDU168—October 2013

System Description

The DC (24 V, nominal) Power-Line Communication (PLC) reference design is intended as an evaluation module for users to develop end-products for industrial applications leveraging the capability to deliver both power and communications over the same DC-power line. The reference design provides a complete design guide for the hardware and firmware design of a master (PLC) node, slave (PLC) node in an extremely small (approximately 1-inch diameter) industrial form factor. The design files include schematics, BOMs, layer plots, Altium files, Gerber Files, a complete software package with the application layer, and an easy-to-use Graphical User Interface (GUI).

The application layer handles the addressing of the slave (PLC) nodes as well as the communication from the host processor (PC or Sitara™ ARM® MPU from Texas Instruments). The host processor communicates only to the mater (PLC) node through a USB-UART interface. The master node then communicates to the slave nodes through PLC. The easy-to-use GUI is also included in the EVM that runs on the host processor and provides address management as well as slave-node status monitoring and control by the user.

The reference design has been optimized from each slave (PLC)-node source-impedance perspective that multiple slaves can be connected to the master (see Section 2.1). Protection circuitry has also been added to the analog front-end (AFE) so that it can be reliably AC coupled to the 24-V line (see Section 2.4). Also note that this reference design layout has been optimized to meet the PLC-power requirements. See for the AFE031 layout requirements for high-current traces.

At the heart of this reference design are the AFE from TI, AFE031, to interface with power lines and the TMS320F28035 Piccolo™ Microcontroller that runs the PLC-Lite protocol from TI.

1.1 AFE031

The AFE031 device is a low-cost, integrated, power-line communication (PLC) AFE device that is capable of capacitive-coupled or transformer-coupled connections to the power line while under the control of a DSP or microcontroller. The AFE031 device is also ideal for driving low-impedance lines that require up to 1.5 A into reactive loads. The integrated receiver is able to detect signals down to 20 µVRMS and is capable of a wide range of gain options to adapt to varying input signal conditions. This monolithic integrated circuit provides high reliability in demanding power-line communications applications. The AFE031 transmit power-amplifier operates from a single supply in the range of 7 V to 24 V. At a maximum output current, a wide output swing provides a 12-VPP (IOUT = 1.5 A) capability with a nominal 15-V supply.

The analog and digital signal-processing circuitry operates from a single 3.3-V power supply. The AFE031 device is internally protected against overtemperature and short-circuit conditions. The AFE031 device also provides an adjustable current limit. An interrupt output is provided that indicates both current limit and thermal limit. There is also a shutdown pin that can be used to quickly put the device into its lowest power state. Through the four-wire serial-peripheral interface, or SPI™, each functional block can be enabled or disabled to optimize power dissipation. The AFE031 device is housed in a thermally-enhanced, surface-mount PowerPAD™ package (QFN-48). Operation is specified over the extended industrial junction temperature range of −40°C to +125°C.
1.2 C2000

The F2803x Piccolo family of microcontrollers (C2000™) provides the power of the C28x core and control-law accelerator (CLA) coupled with highly integrated control peripherals in low pin-count devices. This family is code-compatible with previous C28x-based code, as well as providing a high level of analog integration. An internal voltage regulator allows for single-rail operation. Enhancements have been made to the HRPWM module to allow for dual-edge control (frequency modulation). Analog comparators with internal 10-bit references have been added and can be routed directly to control the PWM outputs. The ADC converts from 0 to 3.3-V fixed full scale range and supports ratiometric VREFHI and VREFLO references. The ADC interface has been optimized for low overhead and latency.

Based on TI's powerful C2000-microcontroller architecture and the AFE031 device, developers can select the correct blend of processing capacity and peripherals to either add power-line communication to an existing design or implement a complete application with PLC communications.
Chapter 2
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Test Data

NOTE: The test data for the DC-PLC Reference Design is also included in the reference design document TIDU160.

2.1 Multiple Slave Nodes Support

The reference design is optimized from an impedance perspective to support multiple slave nodes. Refer to the SAT0021 schematic (see Figure A-1), as more and more nodes are added, the C11 capacitor is added in parallel and therefore the total capacitance as seen by a slave node increases. To support multiple slave nodes, the source impedance must be very small as compared to the load impedance (see Figure 2-1).

C11 (100 pF) creates a low-pass filter and, as multiple nodes are added, the effective capacitance increases. Note that a PLC network is a star topology where each node drives the effective combination load of every other node. Thus C11 is chosen to be 100 pF such that even when up to 10 nodes are added the effective capacitance would be 100 pF x 10 = 1 nF. Therefore the impedance at the PLC-modulation band is calculated with Equation 1

\[ \text{Impedance} = \frac{1}{2\pi fC} = \text{approximately 1.8 k}\Omega \]

where

- \( f = 90 \text{ kHz} \)
- \( C = 1 \text{ nF} = 100 \text{ pF} \times 10 \)

\[ (1) \]

![Figure 2-1. Power-Line Communication AC-Coupling Protection Circuitry](image)

NOTE: Equation 2 is a key requirement to drive multiple slave nodes.

\[ \text{Source Impedance} \ll \text{Load Impedance} \]

(2)

For the following calculation assume that the PLC-Lite modulation frequency is approximately 40 KHz. The source impedance of a PLC node is then calculated as shown in Equation 3.

\[ \text{Source Impedance} = \frac{1}{2\pi fC} = \frac{1}{2\pi(40000)(0.000022)} = 0.18 \Omega \]

where

- \( C = C6 = 22 \mu\text{F} \) (see )

(3)
Assume that the load impedance of a given slave node as seen by the driver PLC-node is approximately 30 Ω. As multiple slaves are added, this load impedance is reduced as the loads are seen as a parallel combination of load impedances. For example, if there are nine slaves on the system, then the total load impedance as seen by one driver PLC-node is calculated as shown in Equation 4.

\[ \text{9 (slaves) + 1 (Master) = 10 PLC nodes, Load Impedance = } \frac{30}{10} = 3 \Omega \]  
\[ \text{4 (slaves) + 1 (Master) = 5 PLC nodes, Load Impedance = } \frac{30}{5} = 6 \Omega \]  

Based on the system requirements, optimizing the capacitance C6, 22 µF, and C11, 100 pF, is important in order to meet the requirement of Equation 2.

2.2 Multiple Slave transmissions and System Latency

As seen in Figure 2-2 and Figure 2-3, there is an insignificant change in amplitude of the modulation signal as more slaves are added. In the previous setup, the 24-V DC line is probed (AC coupled) to the oscilloscope. The oscilloscope is triggered when the button on the PLC node is pressed as it generates a PLC communication packet.

24_IN

SW

Overhead = ~17 ms

Button processing & back-off

TOTAL = ~80 – 200+ ms

Figure 2-4. System Latency
PLC-Lite contains a simple CSMA/CA, MAC which means that if multiple slaves try to access the 24-V DC line, the MC layer in PLC-Lite senses that the line is busy and backs off for a random duration. The total latency for a typical transaction is thus a function of this random back-off for both the initial message and response, as well as the fixed time required to transmit the messages on the line. As shown in Figure 2-4, the system-level latency with one button press event was captured at approximately 80 to 200 ms. This measurement is typical for the default MAC and PHY layer settings used by the demonstration firmware. Modifying MAC or PHY layer parameters can change the system latency.
2.3 15-V Power-Supply Performance for AFE Power Amplifier

For this reference design, note that the 24-V DC supply generates a 15-V and 3.3-V supply as well as it is modulated by the AFE031 for PLC communication. The key point to note is that the switching-regulator operation that generates the 15 V and 3.3 V can interfere with PLC modulation if proper power supply filtering is not included in the design.

To ensure the above requirement, refer to the schematic as shown in : the first circuit seen by the 24-V DC line is a low-pass filter (see Section 2.3.1) which is a very important element of the design. Without this low-pass filter circuit, PLC communication will not work.

![Figure 2-5. Power Section of the Schematic Showing the Low-Pass Filter](image)

![Figure 2-6. 15-V Section of the Power Schematic](image)

In the DC-PLC reference design, another key requirements is to ensure that in an application when a PLC node transmits or receives data, the power amplifier for the AFE031 device is provided with the necessary power (500-mA power budget for the maximum TX swing) to drive the line and to drive the line with a fast response time. The LM34910 step-down switching regulator is used in this reference design (see Figure 2-6) to generate the 15 V for the power amplifier of the AFE031 device. The LM34910 device features all of the functions required to implement a low-cost efficient buck-bias regulator capable of supplying up to 1.25 A to the load. This buck regulator contains a 40-V N-Channel buck switch, and is available in the thermally enhanced WSON-10 package.

**NOTE:** The LM34910 device features a hysteretic-regulation scheme that requires no loop compensation, results in fast load-transient response, and simplifies circuit implementation.

The operating frequency remains constant with line and load variations because of the inverse relationship between the input voltage and the on-time.
As shown in Figure 2-7, the LM34910 device as implemented in this reference design, provides the necessary power for the AFE031 to meet the PLC functionality.

**NOTE:** As seen in Section 2.5, the TX level of 2 Vpp is enough to drive up to a 40-m (length) cable without any BER.

### 2.3.1 T-Type Low-Pass Filter Design

As shown in and , a low-pass filter separates the PLC modulation signal from the switching regulator. The Fc of the low-pass filter is calculated based on the band occupied by the PLC modulation. As shown in , the PLC Lite occupies 42 to 90 kHz. Therefore, the Fc as per the low pass filter in comprises of L = 360 µH (180 µH + 180 µH) and C of 1 µF.

\[
F_c = \frac{1}{\pi \sqrt{LC}} = \text{approximately 17 kHz}
\]  

**NOTE:** Because of the space constraint on this reference design, the previous values of LC were selected. However in applications where board space is available, a lower cutoff Fc (lower than 10 KHz) is desirable.
2.4 PLC-Coupling Circuit Protection

To ensure the reliability of the overall system, the 24-V line is not directly AC coupled to the AFE031 device. The line goes through a two-step AC coupling (see Figure 2-8 and Figure 2-9). In the first stage, the 24-V line is AC coupled to an intermediary stage that has a TVS protection and therefore arrests voltage surges to 9.2 V for a peak surge current of 43.5 A. In this stage the common mode is biased to the GND. In the second-stage AC coupling, the data is AC coupled to the AFE031 device with a DC bias of 7.5 V. To ensure reliability, a simple test of powering off the node completely and then powering up the node was performed on five nodes approximately 250 times. This stress tests ensures that the surges on the power supply can be applied to the node under test.

### Table 2-1. Reliability Data

<table>
<thead>
<tr>
<th>PLC NODE</th>
<th>COMPLETE POWER-ON AND POWER-OFF SEQUENCE</th>
<th>STATUS</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>250 times</td>
<td>Pass, no reliability failure, no change in current drawn observed pre-stress and post-stress</td>
</tr>
<tr>
<td>2</td>
<td>250 times</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>250 times</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>250 times</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>250 times</td>
<td></td>
</tr>
</tbody>
</table>
2.4.1 PLC TX and RX Impedance-Path Testing

The impedance path of the TX and RX is optimized to avoid any signal losses to the PLC-modulation signal.

![Figure 2-10. Power-Line Communication AC-Coupling Protection Circuitry](image)

Figure 2-10 shows that R1 at 0 Ω provides optimized load impedance to the modulation signal. If R1 in Figure 2-10 is even changed to 15 µH (for example), the modulation signal is severely impeded as shown in Figure 2-11 and Figure 2-12.

![Figure 2-11. RX Signal Impeded With 15-µH Inductance](image)

![Figure 2-12. RX Signal Optimized With 0-Ω Resistor (R1)](image)
2.5 PLC-Cable Performance Data

For performance characterization, a 40-m cable was used. To characterize the cable, use the following steps:

1. Generate a chirp signal.
2. Capture the response of the chirp after the cable as shown in Figure 2-13.
3. Post-process (correlation) the signal using Matlab® to generate the impulse response.
4. Leverage the impulse response of the given 40-m cable to generate approximately 320-m cable impulse response.

The channel loss of the 320-m cable is not significantly more than the 40-m cable even up to 100 KHz as shown in Figure 2-14 and Figure 2-15.

The 40-m cable was then used with the DC-PLC hardware to collect the BER measurements across different AFE031 TX-amplitudes as shown in Figure 2-16. The software and firmware used to conduct BER testing is part of the PLC-Lite SDK and are not included in the demonstration software provided with this design.
Figure 2-16. BER Measurement Using the 24-V DC PLC Hardware and the 40-m Cable

Figure 2-17. BER Data: No Packet Errors With Levels 5 and 6 (15 dB and 18 dB Below 15-V pp)
Table 2-2. BER Measurement Results

<table>
<thead>
<tr>
<th>TX AFE031 LEVEL</th>
<th>DECIBELS BELOW MAXIMUM AMPLITUDE</th>
<th>BER DATA</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>15 dB</td>
<td>0 packet error out of 10000 packets transmitted</td>
</tr>
<tr>
<td>6</td>
<td>18 dB</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>21 dB</td>
<td></td>
</tr>
</tbody>
</table>

The data listed in Table 2-2 confirms that the TI PLC-Lite solution with an OFDM solution can support cable length up to 320 m with a very-low TX amplitude of the AFE031 resulting in a large margin to support even longer cables.

2.5.1 Thermal Performance of the Design

To confirm the thermal performance of the design a simple test was performed. To perform the test, the power amplifier was programmed to send a PLC-modulation signal every 1 second. Thermal-imaging camera hot spots were analyzed at time (t0) and then 30 minutes after launching the application (t1). The purpose of this test is to confirm that the design can effectively dissipate heat without localized heating.

As shown in Figure 2-19 and Figure 2-20, there is no localized heating observed in the system after time, t1, compared to t0. For layout guidelines of the AFE031 device and high-current trace routing, see Section D.1.

NOTE: For the thermal-performance application testing, the TX setting for the AFE031 device was set to Level 3.
2.6 IEC Electrostatic-Discharge Testing

The UART and JTAG interface pins on the SAT0022 processor section have IEC ESD-protection up to ±30-kV air, as well as ±30-kV contact which is provided by the TPD1E10B06 device from TI (see the product folder for more information, http://www.ti.com/product/tpd1e10b06). lists the device level-IEC ESD testing data.

Table 2-3. Device-Level IEC ESD Testing

<table>
<thead>
<tr>
<th>LEVEL</th>
<th>IEC-CONTACT SPEC = ± 30 kV</th>
<th>IEC-AIR SPEC = ± 30 kV</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>UNIT1</td>
<td>UNIT2</td>
</tr>
<tr>
<td>±2 kV</td>
<td>PASS</td>
<td>PASS</td>
</tr>
<tr>
<td>±4 kV</td>
<td>PASS</td>
<td>PASS</td>
</tr>
<tr>
<td>±6 kV</td>
<td>PASS</td>
<td>PASS</td>
</tr>
<tr>
<td>±8 kV</td>
<td>PASS</td>
<td>PASS</td>
</tr>
<tr>
<td>±15 kV</td>
<td>PASS</td>
<td>PASS</td>
</tr>
<tr>
<td>±20 kV</td>
<td>PASS</td>
<td>PASS</td>
</tr>
<tr>
<td>±25 kV</td>
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<td>PASS</td>
</tr>
<tr>
<td>±30 kV</td>
<td>PASS</td>
<td>PASS</td>
</tr>
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The schematics are presented in the following order:

1. PLC Node
   • Power Section — SAT0021 (see Figure A-1)
   • C2000 and AFE031 — SAT0022 (see Figure A-2, and Figure A-3)
   • Application Board — SAT0023 (see Figure A-4)
2. USB to UART Board — SAT0045 (see Figure A-5)
3. Master Base Board — SAT0029 (see Figure A-6)
4. Slave Base Board — SAT0030 (see Figure A-7)
5. JTAG Programming Board — SAT0024 (see Figure A-8)
Figure A-1. SAT0021 — Power Section of the PLC Node
Figure A-2. SAT0022 — Processor Section of the PLC Node
AC Coupling Stage for Power Line Communication

Figure A-3. SAT0022 — AFE Section of the PLC Node
Application Board for the PLC Node

Figure A-4. SAT0023 — Application Section of the PLC Node
Figure A-5. SAT0045 — USB to UART Interface Board for Host-to-Master PLC-Node Communication
Base Board For the Master PLC Node

Figure A-6. SAT0029 — Base Board to Mount the Master PLC

Base Board For the Slave PLC Nodes

Figure A-7. SAT0030 — Base Board to Mount the Slave PLC Nodes

Interface Board that connects to the 8 pin connector (C2000 - processor) for JTAG programming

This board connects to the 8-pin connector (C2000 processor) for JTAG.

Figure A-8. SAT0024 — JTAG Interface Board for Programming C2000
<table>
<thead>
<tr>
<th>Part Number</th>
<th>Description</th>
<th>Value</th>
<th>Designators</th>
<th>Package/Case</th>
<th>Tolerance</th>
<th>Volts</th>
<th>Comment</th>
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Figure B-1. SAT0022 — BOM
Appendix C
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Layer Plots

To download the layer plots for each board, see the design files at www.ti.com/tool/24VDCPLCEVM. Figure C-2, Figure C-2, and Figure C-3 show the layer plots for the SAT0021, SAT0022, and SAT0023 respectively.

Figure C-1. SAT0021 — Layer Plot

Figure C-2. SAT0022 — Layer Plot

Figure C-3. SAT0023 — Layer Plot
Appendix D
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Altium Project

To download the Altium project files for each board, see the design files at www.ti.com/tool/24VDCPLCEVM. Figure D-1, Figure D-2, and Figure D-3 show the layout for the SAT0021, SAT0022, and SAT0023 respectively.

Figure D-1. SAT0021 — Layout

Figure D-2. SAT0022 — Layout

Figure D-3. SAT0023 — Layout
D.1 AFE031 High-Current Trace Layout

In a typical power-line communications application, the AFE031 device dissipates 2 W of power when transmitting into the low impedance of the AC line. This amount of power dissipation can increase the junction temperature. An increase in junction temperature can lead to a thermal overload that results in signal transmission interruptions if the proper thermal design of the PCB has not been performed. Proper management of heat flow from the AFE031 device as well as good PCB design and construction are required to ensure proper device temperature, maximize performance, and extend device operating life.

For a layout example of high-current traces see Figure D-4. To achieve lower thermal resistance, 2-oz copper was used in the design as shown in Figure D-5.

NOTE: The AFE031 device has a power amplifier that requires high-current trace layout.

See Section 2.5.1 for thermal performance data of the design when the application software is running.
Appendix E
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Gerber Files

To download the Gerber files for each board, see the design files at www.ti.com/tool/24VDCPLCEVM
Appendix F
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Software Files

To download the software files for the reference design, see the design files at www.ti.com/tool/24VDCPLCEVM
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