TI Designs

16-Bit Analog Output Module Reference Design for Programmable Logic Controllers (PLCs)

Design Features

- Designed to comply with IEC61000-4 standards for ESD, EFT and Surge
- 4 Channel, 16 bit DAC based configurable Analog Outputs
- Selectable Voltage Outputs:
  - ± 10V, 0 - 10V, ± 5V, 0 - 5V
  - Voltage Output Accuracy: ±0.2% FSR
- Selectable Current Outputs:
  - 0 - 20 mA, 4 - 20 mA, 0 - 24mA
  - Current Output Accuracy: ±0.2% FSR
- Output filtering, protection circuitry and integrated 15kV ESD protection
- High-speed, galvanic isolated SPI interface capable of speeds up to 20MHz
- Integrated over-temperature, open-line and short circuit protection features
- On-board isolated Flybuck power supply with inrush current protection
- SPI for I/O control interface with digital isolation
- Slim form factor 95 x 50x 10mm (LxWxH)
- Pluggable to IO Controller for easy evaluation (TIDA-00123)

Featured Applications

- PLC current and voltage output modules
- Field Sensors and Process Transmitters

Design Resources

- TIDA-00119: Input Module Design Files
- TIDA-00123: IO Controller Design Files
- DAC8760: Product Folder
- OPA188: Product Folder
- LM5069: Product Folder
- LM5017: Product Folder
- TPS7A4700: Product Folder
- TPS7A1650: Product Folder
- TPS7A3001: Product Folder
- TPS71533: Product Folder
- ISO7141CC: Product Folder
- ISO7221: Product Folder

Block Diagram
# Table of Contents

1. System Description .......................................................................................................................... 3
2. Design Specifications ....................................................................................................................... 3
3. Block Diagram .................................................................................................................................. 4
4. Circuit design and Component Selection .......................................................................................... 5
   4.1 Digital to Analog Convertor ........................................................................................................... 5
   4.2 Power Supply ................................................................................................................................... 8
   4.3 Isolation ............................................................................................................................................. 8
   4.4 Interface ............................................................................................................................................ 9
5. Software Description ........................................................................................................................... 9
6. Test Setup .......................................................................................................................................... 10
   6.1 Hardware Test Setup ..................................................................................................................... 10
   6.2 Software Test setup ...................................................................................................................... 10
7. Test Results ........................................................................................................................................ 11
   7.1 Accuracy Testing ........................................................................................................................... 11
   7.2 Pre compliance Testing ............................................................................................................... 13
8. References ......................................................................................................................................... 20
9. Design files ....................................................................................................................................... 21
   9.1 Schematics ...................................................................................................................................... 21
   9.2 Bill of Materials ............................................................................................................................. 32
   9.3 PCB Layout ..................................................................................................................................... 36
   9.4 Altium Project .............................................................................................................................. 47
   9.5 Gerber files .................................................................................................................................... 47
1 System Description

Standard industrial analog output (AO) circuits are dedicated to either voltage or current outputs. This reference design using the DAC8760 can output both the standard industrial voltage and current outputs on a single terminal, thus reducing the number of terminals needed from three to two. A combined output succeeds in reducing the wiring cost, connector count, and increasing the versatility of the AO design.

The Smart Analog Output module reference design is intended as an evaluation module for users to develop end-equipment like PLC, field sensors and process transmitters. This design is an Isolated Analog Output Module with Digital isolators for SPI interface and FlyBuck transformer for power supply isolation. On-board EEPROM has been provided to store calibration data and module configuration. Screw type terminals for individual output channels have been provided for easy wiring. LEDs are provided for Power Supply indication.

The reference design provides a complete guide for the design of an Analog Output Module that can be configured for Voltage or Current output, for different output ranges in a slim form factor. This Module has been designed to be pluggable to the IO Controller for quick testing and evaluation. This Module has been designed to comply with EMC standards for Industrial environment. The design files include schematics, BOM, layer plots, Altium files, Gerber Files and an easy-to-use Graphical User Interface (GUI).

The Smart Analog Output Module has been tested for the following:
- Isolated SPI Interface with DACs configures in daisy chain.
- Voltage and Current output functionality and accuracy including over range.
- Surge, EFT & ESD: Pre-compliance testing as per IEC61000-4 standards.

2 Design Specifications

4 Programmable 16 Bit resolution Voltage / Current Analog Outputs with software configurable ranges:

<table>
<thead>
<tr>
<th>Voltage Outputs*</th>
<th>Current Outputs*</th>
</tr>
</thead>
<tbody>
<tr>
<td>• -10V - 10V</td>
<td>• 0- 20mA.</td>
</tr>
<tr>
<td>• -5V - 5V</td>
<td>• 0- 25mA.</td>
</tr>
<tr>
<td>• 0 - 5V</td>
<td>• 4- 20mA.</td>
</tr>
<tr>
<td>• 0 - 10V</td>
<td></td>
</tr>
</tbody>
</table>

*Can be programmed for 10% over-range.

Accuracy:
- Voltage Range <0.1% Error
- Current Range <0.2% Error.

Isolation:
- Power Supply : 1500 VAC
- Signal : 2500 VAC

EMC:

<table>
<thead>
<tr>
<th>Test</th>
<th>Levels</th>
</tr>
</thead>
<tbody>
<tr>
<td>IEC61000-4-2: Electro Static Discharge.</td>
<td>+/- 8kV Air Discharge, +/- 4kV Contact Discharge</td>
</tr>
<tr>
<td>IEC61000-4-4 : Electrical Fast Transients</td>
<td>+/- 2kV, 5kHz/100kHz.</td>
</tr>
<tr>
<td>IEC61000-4-5 : Surge</td>
<td>+/-1kV Common Mode</td>
</tr>
</tbody>
</table>
3 Block Diagram

The Analog output Module has the following Blocks:
1. Digital to Analog Convertor (DAC)
2. Power Supply
3. Isolation
4. Interface

Digital to Analog Convertor (DAC)
This Module utilizes TI’s 16 Bit resolution DAC DAC8760. DAC8760 was chosen for this design for its high level of integration. The DAC8760 features a max 0.1% full-scale range (FSR) total-unadjusted-error (TUE) specification, which includes offset error, gain error, and integral non-linearity (INL) errors at 25°C. The 0.1% FSR TUE is valid for all of the voltage and current output stages providing a baseline for the final system accuracy. The max differential non-linearity (DNL) specification of +/-1 least significant bit (LSB) provides fully monotonic operation for both VOUT and IOUT.
DAC8760 features software-selectable voltage and current ranges, with calibration register for Gain error and Zero error correction. The output slew rate can also be programmed. Four single outputs DAC have been used in this module. The Analog Output module has an EEPROM that stores the calibration data and configuration.

Power Supply
The required voltage rails for non-isolated and isolated section are generated onboard using Flybuck converter topology. The voltage rails are derived from +24V from the IO Controller. The DAC and Op Amps need +/-15V power supply. The DAC additionally needs 5V as reference. The power supply section has linear voltage regulator to reduce the ripple.

Isolation
Most AO modules require isolation from the backplane and other AO modules. This is typically accomplished by isolating the digital signals between the host processor/controller and the DAC in the AO circuit. There are many topologies available to achieve the isolation but galvanic (capacitive) isolation has many advantages over other topologies and has been selected for this design. The Power supply isolation is achieved by the use of Flybuck configured transformer.
Interface
The DAC card has one 50-pin connector for interface with IO Controller. Four outputs and the system earth connection, five -2 pin connectors have been provided.

4 Circuit design and Component Selection

4.1 Digital to Analog Convertor

DAC8760 is designed for industrial and process control applications. DAC8760 can provide 4 to 20 mA, 0 to 20mA or 0 to 24 mA current outputs or 0-5 V, 0-10 V, ±5 V or ±10 voltage outputs with a 10% over range (0-5.5 V, 0-11 V, ±5.5 V, or ±11 V) capability. DAC8760 internal Block Diagram is shown in Figure 2.

![Figure 2 DAC Block Diagram](image)

Notes:
- After Power is applied, by default both the output stages are disabled.
- DAC8760 is capable of providing both current and voltage outputs simultaneously enabled while being controlled by a single data register. This feature cannot be used as the board is configured to provide either current or voltage input only.

4.1.1 Voltage Output

When DAC8760 is configured for voltage output, The max load allowed is 1KΩ Minimum @ 10mA. For voltage output, the module uses +15V and -15V at Power Supply rails thus providing a 5V of headroom for 10mA/1KΩ.

The equation for DAC8760 to generate 16-bit code required Voltage Output is:
4.1.2 Current Output

DAC8760 current output stage consists of a pre-conditioner and a current source. This stage provides current output according to the DAC code. The output range can be programmed as 0-20 mA, 0-24 mA or 4-20 mA. Optionally an external boost transistor can be used to reduce the power dissipation of the device. The maximum compliance voltage on pin IOUT equals (AVDD – 2.5 V). In single power-supply mode, the maximum AVDD is 36 V, and the maximum compliance voltage is 33.5 V. After power-on, the IOUT pin is in a Hi-Z state, with no output. In the present design an external 15 kΩ 0.1% resistor is connected to the ISET-R pin.

The equation for DAC 16-bit code to Current Output is:

For a 0-mA to 20-mA output range:
\[ \text{IOUT} = 20\text{mA} \times \frac{\text{CODE}}{2^N} \]

For a 0-mA to 24-mA output range:
\[ \text{IOUT} = 24\text{mA} \times \frac{\text{CODE}}{2^N} \]

For a 4-mA to 20-mA output range:
\[ \text{IOUT} = 16\text{mA} \times \frac{\text{CODE}}{2^N} + 4\text{mA} \]

where
- CODE is the decimal equivalent of the code loaded to the DAC.
- N is the bits of resolution; 16 for DAC8760 and 12 for DAC7760.
- VREF is the reference voltage for internal reference. VREF = ±5.0 V.
- GAIN is automatically selected for a desired voltage output range as shown in Table 1.

4.1.3 Voltage Sense

+Vsense and – Vsense enable sensing of load. Ideally it is connected to Vout at the terminals. As the Vout and Iout are tied together, when used as current output there will be gain error due to leakage current of the +Vsense pin. This leakage current will be introducing Gain error of -0.36%. This error can be minimized by using high input impedance, low input bias current Op-Amp. In the present design the +Vsense is connected to Vout through buffer OPA188 which has a typical input bias current of 160 pA. This reduces the Gain error reducing error to <0.008%.

4.1.4 HART Option

The DAC8760 is also provisioned to provide HART output. In this design HART Pins are made available to the user by Test Points. For details on HART utilization refer the DAC8760 datasheet.

4.1.5 SPI and Daisy chained DACs
DAC8760 is controlled over a versatile four-wire serial interface (SDI, SDO, SCLK, and LATCH) that can operate at clock rates of up to 31 MHz and is compatible with SPI, QSPI™, Microwire™, and digital signal processing (DSP) standards. The SPI communication command consists of a write address byte and a data word for a total of 24 bits. If there are multiple SPI slave devices, DACs can be connected in Daisy chain. Here the four DACs are arranged as shown below.

This reference design can be configured for Two or Four DACs, achievable by a quick configuration of Jumpers on the PCBA. But care must be taken to place only one Jumper at a time.

The SDO Pin is used to daisy chain the four devices together. As in a SPI, the rising edge of SCLK that clocks in the MSB of the input frame marks the beginning of WRITE cycle. When the serial transfer to all the devices is complete, LATCH is made HIGH. This action transfers the data from SPI shift registers to the device internal registers of the respective DAC. The number of clocks in each frame depends on the number of devices. Each frame is of Nx24 clocks.

1. 2 DAC Frame size = 48 CLK: First 24clock for DACB and Next 24Clock for DACA.
2. 4 DAC Frame size = 96CLK First 24clock for DACD, Next 24Clock for DACC, Next 24clock for DACB, and Last 24 clock for DACA.

Total Write time estimation for a Four DAC Design:
\[ T = (24 \times 4 / F_s) + t_{DD} + t_{DC} + t_{DB} + t_{DA} + t_{LE} + t_s \]
Where:
\( F_s \) = SPI Clock Rate in Hz.
\( t_{DX} \) = Software overhead from host side to load the Next SPI Data for the next DAC.
\( t_{LE} \) = Software overhead from host to change the LATCH line status (as an I/O port Pin).
\( T_s \) = Analog Output Settling time (Refer Datasheet of DAC8760)

4.1.6 Filter and Protection for Surge, EFT and ESD

The output stage is designed to withstand 8kV ESD, 1kV EFT and 1kV Surge. Every channel is protected by TVS SMBJ18CA. This circuit clamps Over-voltage inputs ~25V. The ESD protection diodes also protect against overvoltage inputs. Layout guidelines have to be followed to ensure compliance to EMC standards. The protection devices are selected to dissipate the required energy.

4.2 Power Supply

The analog output module uses 24V DC input from the IO Controller.

The LM5069 inrush current controller provides intelligent control of the power supply current during insertion and removal of Pluggable Module from a powered IO Controller. The LM5069 provides inrush current limiting during turn-on, and monitoring of the load current for faults during normal operation. Additional functions include Under-Voltage Lock-Out (UVLO) and Over-Voltage Lock-Out (OVLO) to ensure voltage is supplied to the load only when the system input voltage is within a range. The inrush current limit is set to 2.75A.

DAC and Op Amps are supplied by +/-15V, which is derived from Flybuck DC-DC converter (LM5017) followed by a low noise LDO. The Flybuck DC-DC converter is designed to give +/-15V and 3.3V with a ripple of <50mV peak. A soft-start feature is implemented on LM5017 to limit the inrush current. For a detailed Flybuck Design, refer AN-2292.

4.3 Isolation

4.3.1 Power Supply Isolation

The LM5017 based Flybuck Isolated Power supply provides the Galvanic Isolation to the IO Controller. This Isolation is required to keep the IO Controller protected from any unexpected overvoltage on the Analog Outputs field connections. The level of isolation depends on the Coupled Inductor’s specification. This design utilizes a coupled Inductor of 1500VAC, Isolation.

4.3.2 Digital Isolation

In order to maintain isolation from the host controller, these signals are isolated through a digital isolator. The SPI Signals isolated are: SCLK, MISO, MOSI, CSO (Latch), CLR, SDRDY. The IO Controller is connected to the DAC by the High Speed Digital Isolator ISO7141CC and ISO7221. With this digital isolator the Host Processor on IO Controller maintains 2.5kVrms of galvanic isolation. Ten ohms termination resistance is placed near to the Isolators to maintain good Signal Integrity.
4.4 Interface

The Analog Output module has with following connectors:
1. J1 - J4: 2 Pin Screw Terminal type 2.54mm Pitch connectors for interfacing external Loads.
2. J5: 2 Pin Screw Terminal type 2.54mm Pitch connectors for connecting Earth Reference.
3. J6: 50 Pin High Speed Connector for SPI/Power Supply interface to the IO Controller.

5 Software Description

The DAC8760 has a number of 16 bit Registers. These need to be Configured / Read/ Written to achieve the desired functionality. A brief overview is as described here. For details refer the datasheet of DAC8760.

<table>
<thead>
<tr>
<th>REGISTER / COMMAND</th>
<th>READ/WRITE ACCESS</th>
<th>DATA BITS (DB15:DB0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Control</td>
<td>RW</td>
<td>CRSEL, OVR, NEXT, OUTEN, SIGCLK, STSTEP, GREN, DCEN, RANGE</td>
</tr>
<tr>
<td>Configuration</td>
<td>RW</td>
<td>X, IOUT, RANGE, DUALOUT, APD, RESER5, CALEN, HARTE, CRCEN, WDEN, WOPD</td>
</tr>
<tr>
<td>DAC Data</td>
<td>RW</td>
<td>D15:00</td>
</tr>
<tr>
<td>No operation(2)</td>
<td>—</td>
<td>X</td>
</tr>
<tr>
<td>Read Operation(2)</td>
<td>—</td>
<td>READ ADDRESS</td>
</tr>
<tr>
<td>Reset</td>
<td>W</td>
<td></td>
</tr>
<tr>
<td>Status</td>
<td>R</td>
<td>Reserved, CRC, FLT, FD-C, FD-F, I-F, SR, ON, T-F, FLT</td>
</tr>
<tr>
<td>DAC Gain Calibration</td>
<td>RW</td>
<td>0:15:00, unsigned</td>
</tr>
<tr>
<td>DAC Zero Calibration</td>
<td>RW</td>
<td>0:15:20, signed</td>
</tr>
<tr>
<td>WATCHDOG Timer(2)</td>
<td>—</td>
<td>X</td>
</tr>
</tbody>
</table>

1. Control and Configuration registers gives users option to select - Output Type, Range (over range), and Slew rate. It also allows user to set the following: Output, Watchdog, HART, Dual Output.
2. DAC Data Register allow user to write the digital equivalent of the desired Analog Output.
3. Read, Status and Watchdog Timer Commands allow the user to monitor the DAC function.
4. Calibration Registers: Allows the user to write the calibration values for Zero Error and Gain Error correction.
5. At power up each of the DAC needs to be initialized using CONTROL and CONFIGURATION Registers.
6. Next the DAC DATA register has to be loaded with relevant values to generate the desired Analog Output.
DAC configuration Examples
Example 1: DAC configured as Voltage Output of 0 to 10V.
To set the Voltage output Range of 0 to 10V, SSI as daisy chained, set Slew rate and Output Enable
No Overrange the CONTROL register needs to be set as shown
Also the CONFIGURATION registers must be written for NO Dual Output, No HART,10ms
Watchdog enabled, No APD , No Calibration.

<table>
<thead>
<tr>
<th>Register</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Control</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Configuration</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

Example 2: DAC configured as Voltage Output of 0mA to 24mA
To set the Current output of 0 to 24mA, SSI as daisy chained, set Slew rate and Output Enable,
No Overrange the CONTROL register needs to be set as shown below.
Also the CONFIGURATION registers must be written for NO Dual Output, No HART,51ms
Watchdog enabled, No APD , No Calibration.

<table>
<thead>
<tr>
<th>Register</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Control</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Configuration</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td></td>
</tr>
</tbody>
</table>

6 Test Setup

6.1 Hardware Test Setup

6.2 Software Test setup

The design verification setup uses a GUI based Test Setup. The GUI on the PC connects to the IO
Controller through USB communication. The IO Controller then controls the Analog Output Card via
SPI interface, to generate Analog Output levels as selected on the GUI. The Analog Output generated
is measured by the 8 ½ DMM. The GUI does the computation of results.

The GUI is a LabView based software. It can set the below functionalities:
1. Analog Output Channel: There are four channels in each card.
2. Analog output Type: Each Analog Output can be selected as voltage or current type .
3. ZERO Error Correction register:
4. Gain correction Register.
5. Result Options: DNL or INL or TUE. This can be before or after the offset / gain corrections. In
the results herewith the errors are not compensated for.
7 Test Results

7.1 Accuracy Testing

The overall accuracy depends on the performance of the different subsystems. The result below is for the integrated Analog Output Module consisting of the DAC, Power Supply, Filters, and Protections.

Voltage Output – Performance Graphs:

Current Output - Performance Graphs:
7.1.1 Results Summary at 25°C

The Results indicate that the overall TUE is within the target range of 0.2% FSR (Section 2). The maximum DNL is within 1 LSB and the INL is within 0.2% FSR at 25°C.

Table 1 Measurement Results Summary- Voltage Ranges.

<table>
<thead>
<tr>
<th>Sr. No.</th>
<th>Parameter</th>
<th>+/-10V</th>
<th>0 to10V</th>
<th>+/-5V</th>
<th>0 to 5V</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>TUE (%FSR)Max</td>
<td>+0.038</td>
<td>0.035%</td>
<td>0.017%</td>
<td>0.019%</td>
</tr>
<tr>
<td>2</td>
<td>TUE (%FSR)Min</td>
<td>-0.0083</td>
<td>-0.0019</td>
<td>-0.0064</td>
<td>-0.005</td>
</tr>
<tr>
<td>3</td>
<td>INL(%FSR)Max</td>
<td>-0.00045</td>
<td>0.00851</td>
<td>0.00039</td>
<td>0.0047</td>
</tr>
<tr>
<td>4</td>
<td>INL(%FSR)Min</td>
<td>-0.04845</td>
<td>-0.0249</td>
<td>-0.024</td>
<td>-0.0055</td>
</tr>
<tr>
<td>5</td>
<td>DNL Max</td>
<td>0.381</td>
<td>0.594</td>
<td>0.415</td>
<td>0.511</td>
</tr>
<tr>
<td>6</td>
<td>DNL Min</td>
<td>-0.555</td>
<td>-0.587</td>
<td>-0.473</td>
<td>-0.357</td>
</tr>
</tbody>
</table>

Table 2 Measurement Results Summary- Current Ranges.

<table>
<thead>
<tr>
<th>Sr. No.</th>
<th>Parameter</th>
<th>4 to 20mA</th>
<th>0 to 20mA</th>
<th>0 to 24mA</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>TUE (%FSR)Max</td>
<td>0.327</td>
<td>0.291</td>
<td>0.257</td>
</tr>
<tr>
<td>2</td>
<td>TUE (%FSR)Min</td>
<td>-0.532</td>
<td>-0.309</td>
<td>-0.361</td>
</tr>
<tr>
<td>3</td>
<td>INL(%FSR)Max</td>
<td>0</td>
<td>0.0007</td>
<td>0.0009</td>
</tr>
<tr>
<td>4</td>
<td>INL(%FSR)Min</td>
<td>-0.106</td>
<td>-0.106</td>
<td>-0.101</td>
</tr>
<tr>
<td>5</td>
<td>DNL Max</td>
<td>0.120</td>
<td>0.080</td>
<td>0.078</td>
</tr>
<tr>
<td>6</td>
<td>DNL Min</td>
<td>0.024</td>
<td>-0.024</td>
<td>-0.024</td>
</tr>
</tbody>
</table>

By definition, INL for a particular code is the summation of DNL array till that code. DNL is specified in LSB and INL is specified as %FSR.
### 7.2 Pre compliance Testing

The Analog Output Module has been designed to meet standard EMC requirements for Industrial PLC application.

The following EMC tests have been performed:

<table>
<thead>
<tr>
<th>Tests</th>
<th>Standards</th>
</tr>
</thead>
<tbody>
<tr>
<td>Electro Static Discharge</td>
<td>IEC61000-4-2</td>
</tr>
<tr>
<td>Electrical Fast Transients</td>
<td>IEC61000-4-4</td>
</tr>
<tr>
<td>Surge</td>
<td>IEC61000-4-5</td>
</tr>
</tbody>
</table>

Criteria and performance as per IEC61131-2

<table>
<thead>
<tr>
<th>Criteria</th>
<th>Performance (Pass) Criteria</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>The Analog Output Module shall continue to operate as intended. No loss of function or performance even during the test.</td>
</tr>
<tr>
<td>B</td>
<td>Temporary degradation of performance is accepted. After the test Analog Output Module shall continue to operate as intended without manual intervention.</td>
</tr>
<tr>
<td>C</td>
<td>During the test loss of functions accepted, but no destruction of hardware or software. After the test Analog Output Module shall continue to operate as intended automatically, after manual restart or power off/power on.</td>
</tr>
</tbody>
</table>
7.2.1 Test Set-Up

Capacitive Coupler

I/O Cable

EFT/Surge/ESD Generator – UCS500N (EMI Test)

Unit Under Test

24V I/P
7.2.2 Electro Static Discharge (ESD): IEC61000-4-2

The ESD level at I/O connectors and the performance criteria expected are as follows:

<table>
<thead>
<tr>
<th>Generic Test Standard</th>
<th>Test Level</th>
<th>Performance (Pass Criteria)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ESD-IEC 61000-4-2</td>
<td>4 kV contact discharges – Level 2</td>
<td>Criteria B (Monitored before and after the test)</td>
</tr>
<tr>
<td></td>
<td>8 kV air discharges – Level 3</td>
<td></td>
</tr>
</tbody>
</table>

**Setup Description**

The ESD is injected to the EUT as **Contact discharge or Air discharge**.

The EUT is placed on a horizontal coupling plane (HCP) of 160 x 80cm dimensions on top of a wooden table 80cm high and located above ground reference plane. The EUT and its attached cables were isolated from the HCP by a thin insulating support of 0.5mm thickness. Electrostatic discharges were applied using an ESD gun directly (via contact or air discharges) or indirectly (via horizontal coupling plane). EUT operation was monitored after the test. The EUT is tested in active mode using unshielded 3m cables on IO ports.

- Connect the EUT as shown in the Test Setup. The shield pin is connected to Local Earth same as the Test Generator.
- Power on the EUT
  - The test s/w is configured to generate an output of 2.5V and 7.5 V alternately for 2 seconds each.
  - The respective channel is checked before and after the test.
- The ESD test is performed as per below test levels mentioned in below table
- After the test is performed, to check the degradation conduct a performance test.
## Results

<table>
<thead>
<tr>
<th>Test No</th>
<th>Test Mode</th>
<th>Observation</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Air +2kV</td>
<td>PASS</td>
</tr>
<tr>
<td>2</td>
<td>Air -2kV</td>
<td>PASS</td>
</tr>
<tr>
<td>3</td>
<td>Air +4kV</td>
<td>PASS</td>
</tr>
<tr>
<td>4</td>
<td>Air -4kV</td>
<td>PASS</td>
</tr>
<tr>
<td>5</td>
<td>Air +6kV</td>
<td>PASS</td>
</tr>
<tr>
<td>6</td>
<td>Air -6kV</td>
<td>PASS</td>
</tr>
<tr>
<td>7</td>
<td>Air +8kV</td>
<td>PASS</td>
</tr>
<tr>
<td>8</td>
<td>Air -8kV</td>
<td>PASS</td>
</tr>
<tr>
<td>9</td>
<td>Contact +1kV</td>
<td>PASS</td>
</tr>
<tr>
<td>10</td>
<td>Contact -1kV</td>
<td>PASS</td>
</tr>
<tr>
<td>11</td>
<td>Contact +2kV</td>
<td>PASS</td>
</tr>
<tr>
<td>12</td>
<td>Contact -2kV</td>
<td>PASS</td>
</tr>
<tr>
<td>13</td>
<td>Contact +4kV</td>
<td>PASS</td>
</tr>
<tr>
<td>14</td>
<td>Contact -4kV</td>
<td>PASS</td>
</tr>
<tr>
<td>15</td>
<td>HCP +2kV</td>
<td>PASS</td>
</tr>
<tr>
<td>16</td>
<td>HCP -2kV</td>
<td>PASS</td>
</tr>
<tr>
<td>17</td>
<td>HCP +4kV</td>
<td>PASS</td>
</tr>
<tr>
<td>18</td>
<td>HCP -4kV</td>
<td>PASS</td>
</tr>
<tr>
<td>19</td>
<td>VCP +2kV</td>
<td>PASS</td>
</tr>
<tr>
<td>20</td>
<td>VCP -2kV</td>
<td>PASS</td>
</tr>
<tr>
<td>21</td>
<td>VCP +4kV</td>
<td>PASS</td>
</tr>
<tr>
<td>22</td>
<td>HCP -4kV</td>
<td>PASS</td>
</tr>
</tbody>
</table>

*Functionality checked before and after the test.*
7.2.3 Electric Fast Transients test: EFT – IEC61000 – 4-4

Test Level & Expected Performance

The EFT burst at I/O connectors and the performance criteria expected are as follows:

<table>
<thead>
<tr>
<th>Generic Test Standard</th>
<th>Test Level</th>
<th>Performance (Pass Criteria)</th>
</tr>
</thead>
<tbody>
<tr>
<td>EFT - IEC 61000-4-4</td>
<td>±2 KV at 5 KHz, 100 KHz on signal ports</td>
<td>Criteria B</td>
</tr>
</tbody>
</table>

Criteria B (Monitored before and after the test)

Description

Setup:
The EFT is injected on all cables together using a Capacitive Coupling Clamp. EUT is connected to auxiliary sources by unshielded cables. The lengths of the cables are set to 3m and cables are placed 10cm above the reference plane. The test is carried out with the EUT placed 10cm above the reference plane on insulating material, and with the EUT placed on the reference plane.

Monitoring:
- Connect the EUT as shown in the Test Setup. The shield Pin is connected to Local Earth same as the Test Generator.
- Power on the EUT
  - The test s/w is configured to generate an output of 2.5V and 7.5 V alternately for 2 seconds each.
  - The respective channel is checked before and after the test.
- The ESD test is performed as per below test levels mentioned in below table
- After the test is performed, to check the degradation conduct a performance test.
### Results

Result summary to be updated with observations.

<table>
<thead>
<tr>
<th>Test No</th>
<th>Test Mode</th>
<th>Observation</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>+ 0.5 kV, 5kHz</td>
<td>PASS</td>
</tr>
<tr>
<td>2</td>
<td>- 0.5 kV, 5kHz</td>
<td>PASS</td>
</tr>
<tr>
<td>3</td>
<td>+ 1 kV, 5kHz</td>
<td>PASS</td>
</tr>
<tr>
<td>4</td>
<td>- 1 kV, 5kHz</td>
<td>PASS</td>
</tr>
<tr>
<td>5</td>
<td>+ 1.5 kV, 5kHz</td>
<td>PASS</td>
</tr>
<tr>
<td>6</td>
<td>- 1.5 kV, 5kHz</td>
<td>PASS</td>
</tr>
<tr>
<td>7</td>
<td>+ 2 kV, 5kHz</td>
<td>PASS</td>
</tr>
<tr>
<td>8</td>
<td>- 2 kV, 5kHz</td>
<td>PASS</td>
</tr>
<tr>
<td>9</td>
<td>+ 0.5 kV, 100kHz</td>
<td>PASS</td>
</tr>
<tr>
<td>10</td>
<td>- 0.5 kV, 100kHz</td>
<td>PASS</td>
</tr>
<tr>
<td>11</td>
<td>+ 1 kV, 100kHz</td>
<td>PASS</td>
</tr>
<tr>
<td>12</td>
<td>- 1 kV, 100kHz</td>
<td>PASS</td>
</tr>
<tr>
<td>13</td>
<td>+ 1.5 kV, 100kHz</td>
<td>PASS</td>
</tr>
<tr>
<td>14</td>
<td>- 1.5 kV, 100kHz</td>
<td>PASS</td>
</tr>
<tr>
<td>15</td>
<td>+ 2 kV, 100kHz</td>
<td>PASS</td>
</tr>
<tr>
<td>16</td>
<td>- 2 kV, 100kHz</td>
<td>PASS</td>
</tr>
</tbody>
</table>

*Functionality checked before and after the test.

#### 7.2.4 SURGE- IEC61000-4-5

**Test Level & Expected Performance**

The Common-Mode Surge at I/O connectors and the performance criteria expected are as follows:

<table>
<thead>
<tr>
<th>Generic Test Standard</th>
<th>Test Level</th>
<th>Performance (Pass Criteria)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Surge IEC 61000-4-5</td>
<td>±1kV CM on signal ports</td>
<td>Criteria B(Monitored before and after the test)</td>
</tr>
</tbody>
</table>
Description

Setup:
The EUT and analog output cable were placed on non-conductive support 10cm above a reference ground plane. Surge was injected into analog output cable (I/O cable) for testing via Coupling Decoupling Network. The EUT operation was monitored before and after the test.

![Diagram of EUT setup]

EUT operation monitored after the test. All the eight channels were monitored after the test by the Microcontroller (on IO Controller) and compared with a Set Value (equivalent of the external constant voltage or current source). The Error should be within accuracy as mentioned in Section 6.3.1.

Method of monitoring:

- Connect the EUT as shown in the Test Setup. The shield Pin is connected to Local Earth same as the Test Generator.
- Power on the EUT
  - The test s/w is configured to generate an output of 2.5V and 7.5 V alternately for 2 seconds each.
  - The respective channel is checked before and after the test.
- The ESD test is performed as per below test levels mentioned in below table
- After the test is performed, to check the degradation - conduct a performance test.

Results

Result summary to be updated with observations.

<table>
<thead>
<tr>
<th>Test No</th>
<th>Test Mode</th>
<th>Observation*</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>+ 0.5 kV</td>
<td>PASS</td>
</tr>
<tr>
<td>2</td>
<td>- 0.5 kV</td>
<td>PASS</td>
</tr>
<tr>
<td>3</td>
<td>+ 1 kV</td>
<td>PASS</td>
</tr>
<tr>
<td>4</td>
<td>- 1 kV</td>
<td>PASS</td>
</tr>
</tbody>
</table>

*Functionality checked before and after the test.
8 References

2. Op Amp Noise Theory and Applications Literature Number SLOA082

8.1.1 Terminology

**Total Unadjusted Error (TUE)**
TUE is measurement error without any gain or offset error compensations. TUE gives an exact measure of the system level inaccuracies. With the right choice of components and proper PCB layout the need for Factory calibration may be avoided. This shall save a lot of time and cost during Mass Production.

\[
TUE = \sqrt{\text{sq(Offset Error)} + \text{sq(Gain Error)} + \text{sq(DNL)} + \text{sq(INL)}}.
\]

**Differential Non Linearity (DNL) and Integral Non Linearity (INL)**
DNL is the deviation between two analog values corresponding to adjacent digital values. Ideally, any two adjacent digital codes correspond to output analog voltages that are exactly one LSB apart. Any deviation from the ideal step width (LSB) is the Differential Non-Linearity.
9 Design files

9.1 Schematics
## 9.2 Bill of Materials

<table>
<thead>
<tr>
<th>Fitted</th>
<th>Description</th>
<th>Designator</th>
<th>Manufacturer</th>
<th>PartNumber</th>
<th>Quantity</th>
<th>RoHS</th>
<th>Package Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fitted</td>
<td>Printed Circuit Board</td>
<td>IPCB</td>
<td>Any</td>
<td>ISE-PLC-AOM-200</td>
<td>1</td>
<td>O</td>
<td></td>
</tr>
<tr>
<td>Fitted</td>
<td>CAP, TA, 4.7uF, 35V, +/-10%, 1.9 ohm, SMD</td>
<td>C1, C2, C7, C45</td>
<td>Vishay-Sprague</td>
<td>293D475X9035C2TE3</td>
<td>4</td>
<td>Y</td>
<td>6032-28</td>
</tr>
<tr>
<td>Fitted</td>
<td>CAP, CERM, 1uF, 25V, +/-10%, X7R, 0603</td>
<td>C3, C40, C56, C65</td>
<td>TDK</td>
<td>C1608X7R1E105K080AB</td>
<td>4</td>
<td>Y</td>
<td>0603</td>
</tr>
<tr>
<td>Fitted</td>
<td>CAP, CERM, 0.47uF, 100V, +/-10%, X7R, 1206</td>
<td>C4</td>
<td></td>
<td>C3216X7R2A474K</td>
<td>1</td>
<td>Y</td>
<td>1206</td>
</tr>
<tr>
<td>Fitted</td>
<td>CAP, CERM, 4.7uF, 50V, +/-10%, X5R, 0805</td>
<td>C5, C10, C18, C19, C22, C24, C32, C33, C51, C52, C57, C63</td>
<td>TDK</td>
<td>C2012X5R1H475K125AB</td>
<td>12</td>
<td>Y</td>
<td>0805</td>
</tr>
<tr>
<td>Fitted</td>
<td>CAP, CERM, 0.01uF, 100V, +/-5%, X7R, 0603</td>
<td>C6, C71, C76, C82</td>
<td>AVX</td>
<td>06031C103JAT2A</td>
<td>4</td>
<td>Y</td>
<td>0603</td>
</tr>
<tr>
<td>Fitted</td>
<td>CAP, CERM, 1000pF, 2KV 10% X7R 1206</td>
<td>C8, C26, C31, C37, C43, C46, C62</td>
<td>Johanson Dielectrics Inc</td>
<td>202R18W102KV4E</td>
<td>6</td>
<td>Y</td>
<td>1206</td>
</tr>
<tr>
<td>Fitted</td>
<td>CAP, CERM, 0.1uF, 50V, +/-10%, X7R, 0805</td>
<td>C9, C17, C29, C34, C39, C42, C44, C46, C47, C49, C50, C58, C59, C61, C64, C66, C67, C68, C70, C72, C73, C74, C75, C77, C78, C79, C80, C81, C83, C84, C85, C86, C87, C89, C90, C91, C92, C93, C94, C95, C96</td>
<td>AVX</td>
<td>06035C104KAT2A</td>
<td>41</td>
<td>Y</td>
<td>0603</td>
</tr>
<tr>
<td>Fitted</td>
<td>CAP, CERM, 3900pF, 50V, +/-10%, X7R, 0805</td>
<td>C11, C25, C35, C55</td>
<td>AVX</td>
<td>08055C392KAT2A</td>
<td>4</td>
<td>Y</td>
<td>0805</td>
</tr>
<tr>
<td>Fitted</td>
<td>CAP, CERM, 2.2uF, 25V, +/-10%, X5R, 0805</td>
<td>C12, C36, C41</td>
<td>MuRata</td>
<td>GRM219R61E225KA12D</td>
<td>3</td>
<td>Y</td>
<td>0805</td>
</tr>
<tr>
<td>Fitted</td>
<td>CAP, TA, 22uF, 35V, +/-10%, 0.6 ohm, SMD</td>
<td>C13</td>
<td>Vishay-Sprague</td>
<td>293D226X9035D2TE3</td>
<td>1</td>
<td>Y</td>
<td>7343-31</td>
</tr>
<tr>
<td>Fitted</td>
<td>CAP, CERM, 2.2uF, 100V, +/-10%, X7R, 1210</td>
<td>C14, C23</td>
<td>MuRata</td>
<td>GRM32ER72A225KA35L</td>
<td>2</td>
<td>Y</td>
<td>1210</td>
</tr>
<tr>
<td>Fitted</td>
<td>CAP, CERM, 10uF, 16V, +/-20%, X5R, 0805</td>
<td>C16</td>
<td>AVX</td>
<td>0805YD106MAT2A</td>
<td>1</td>
<td>Y</td>
<td>0805</td>
</tr>
<tr>
<td>Fitted</td>
<td>CAP, AL, 22uF, 50V, +/-20%, 0.88 ohm, SMD</td>
<td>C20</td>
<td>Panasonic</td>
<td>EEE-FK1H220P</td>
<td>1</td>
<td>Y</td>
<td>SMT Radial  D</td>
</tr>
<tr>
<td>Fitted</td>
<td>CAP, TA, 10uF, 35V, +/-10%, 1.6 ohm, SMD</td>
<td>C21, C28, C48, C60</td>
<td>Vishay-Sprague</td>
<td>293D106X9035C2TE3</td>
<td>4</td>
<td>Y</td>
<td>6032-28</td>
</tr>
<tr>
<td>Fitted</td>
<td>CAP, CERM, 1000pF, 100V, +/-5%, X7R, 0603</td>
<td>C30, C69, C88</td>
<td>AVX</td>
<td>06031C102JAT2A</td>
<td>3</td>
<td>Y</td>
<td>0603</td>
</tr>
<tr>
<td>Fitted</td>
<td>CAP, CERM, 0.47uF, 50V, 10%, X5R, 0603</td>
<td>C53</td>
<td>Taiyo Yuden</td>
<td>UMK107ABJ474KA-T</td>
<td>1</td>
<td>Y</td>
<td>0603</td>
</tr>
<tr>
<td>Fitted</td>
<td>Diode, Zener, 18V, 1W, SOD-123</td>
<td>D1, D6</td>
<td>Panasonic</td>
<td>DZ2W18000L</td>
<td>2</td>
<td>Y</td>
<td>SOD-123</td>
</tr>
<tr>
<td>Fitted</td>
<td>LED SmartLED Green 570NM</td>
<td>D3, D8, D25</td>
<td>OSRAM</td>
<td>LG L29K-G2J1-24-Z</td>
<td>3</td>
<td>Y</td>
<td>0603</td>
</tr>
<tr>
<td>Fitted</td>
<td>Diode, Schottky, 200V, 1A, PowerDI123</td>
<td>D4, D17</td>
<td>Diodes Inc.</td>
<td>DFLS1200-7</td>
<td>2</td>
<td>Y</td>
<td>PowerDI123</td>
</tr>
<tr>
<td>Fitted</td>
<td>TVS 18 VOLT 600 WATT Bi-DIR SMB</td>
<td>D5, D10, D13, D18</td>
<td>Littelfuse Inc</td>
<td>SMBJ18CA</td>
<td>4</td>
<td>Y</td>
<td>SMB</td>
</tr>
<tr>
<td>Fitted</td>
<td>Diode, P-N, 70V, 0.2A, SOT-323</td>
<td>D9, D12, D16, D21</td>
<td>Diodes Inc.</td>
<td>DESD1P0RFW-7</td>
<td>4</td>
<td>Y</td>
<td>SOT-323</td>
</tr>
<tr>
<td>Fitted</td>
<td>Diode, Schottky, 60V, 1A, SOD-123F</td>
<td>D20</td>
<td>NXP Semiconductor</td>
<td>PMEG6010CEH,115</td>
<td>1</td>
<td>Y</td>
<td>SOD-123F</td>
</tr>
<tr>
<td>Fitted</td>
<td>Diode, Schottky, 45V, 0.1A, SOD-523</td>
<td>D26</td>
<td>Diodes Inc.</td>
<td>SDM10U45-7-F</td>
<td>1</td>
<td>Y</td>
<td>SOD-523</td>
</tr>
<tr>
<td>Fitted</td>
<td>FERRITE CHIP 1000 OHM 300MA 0603</td>
<td>FB1, FB2, FB3, FB4</td>
<td>TDK Corporation</td>
<td>MMZ1608Y102B</td>
<td>4</td>
<td>Y</td>
<td>0603</td>
</tr>
<tr>
<td>Fitted</td>
<td>Description</td>
<td>Designator</td>
<td>Manufacturer</td>
<td>PartNumber</td>
<td>Quantity</td>
<td>RoHS</td>
<td>Package Reference</td>
</tr>
<tr>
<td>--------</td>
<td>-------------</td>
<td>------------</td>
<td>--------------</td>
<td>------------</td>
<td>----------</td>
<td>------</td>
<td>------------------</td>
</tr>
<tr>
<td>Fitted</td>
<td>Terminal Block, 4x1, 2.54mm, TH</td>
<td>J1, J2, J3, J4, J5</td>
<td>On Shore Technology Inc</td>
<td>OSTVN02A150</td>
<td>5</td>
<td>Y</td>
<td>TERM_BLK, 2pos, 2.54mm</td>
</tr>
<tr>
<td>Fitted</td>
<td>Receptacle, 0.8mm, 25x2, SMT</td>
<td>J6</td>
<td>Samtec</td>
<td>ERF8-025-05.0-L-DV-K-TR</td>
<td>1</td>
<td>Y</td>
<td>25x2 Socket Strip</td>
</tr>
<tr>
<td>Fitted</td>
<td>FERRITE CHIP 1000 OHM 300MA 0603</td>
<td>L1, L2, L4</td>
<td>TDK Corporation</td>
<td>MMZ1608B102C</td>
<td>3</td>
<td>Y</td>
<td>0603</td>
</tr>
<tr>
<td>Fitted</td>
<td>Inductor, Chip, ±10%</td>
<td>L3</td>
<td>Panasonic</td>
<td>E LI-EA3R3MF</td>
<td>1</td>
<td>1210</td>
<td></td>
</tr>
<tr>
<td>Fitted</td>
<td>Thermal Transfer Printable Labels, 0.650&quot; W x 0.200&quot; H - 10,000 per roll</td>
<td>LBL1</td>
<td>Brady</td>
<td>THT-14-423-10</td>
<td>1</td>
<td>Y</td>
<td>PCB Label 0.650&quot;H x 0.200&quot;W</td>
</tr>
<tr>
<td>Fitted</td>
<td>MOSFET, N-CH, 60V, 50A, SON 5x6mm</td>
<td>Q1</td>
<td>Texas Instruments</td>
<td>CSD18537NQ5A</td>
<td>1</td>
<td>Y</td>
<td>SON 5x6mm</td>
</tr>
<tr>
<td>Fitted</td>
<td>RES, 0 ohm, 5%, 0.25W, 1206</td>
<td>R1</td>
<td>Vishay-Dale</td>
<td>CRCW12060000Z0EA</td>
<td>1</td>
<td>Y</td>
<td>1206</td>
</tr>
<tr>
<td>Fitted</td>
<td>RES, 10 ohm, 5%, 0.25W, 1206</td>
<td>R2, R11, R20, R31</td>
<td>Vishay-Dale</td>
<td>CRCW120610R0JNEA</td>
<td>4</td>
<td>Y</td>
<td>1206</td>
</tr>
<tr>
<td>Fitted</td>
<td>RES, 340k ohm, 1%, 0.1W, 0603</td>
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<tr>
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<td>RG1608P-563-B-T5</td>
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<td>Manufacturer</td>
<td>PartNumber</td>
<td>Quantity</td>
<td>RoHS</td>
<td>Package Reference</td>
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<td>R54</td>
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<td>Transformer, 50uH, SMT</td>
<td>T1</td>
<td>Wurth Elektronik eiSos</td>
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<td>17.75x12.7x1 3.46mm</td>
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<td>100V, 600mA Constant On-Time Synchronous Buck Regulator, DDA0008B</td>
<td>U1</td>
<td>Texas Instruments</td>
<td>LM5017MRE/NOPB</td>
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<td>1-Channel, 16-Bit, Programmable Current/Voltage Output DAC for 4-20mA Current Loop Applications</td>
<td>U2, U5, U8, U14</td>
<td>Texas Instruments</td>
<td>DAC8760IWP</td>
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<td>HTSSOP (PWP) 24</td>
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<td>36-V, 1-/A, 4.17-/VRMS, RF LDO Voltage Regulator, RGW0020A</td>
<td>U3</td>
<td>Texas Instruments</td>
<td>TPS7A4700RGW</td>
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<td>Y</td>
<td>RGW0020A</td>
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<td>Precision, Low Noise, Rail-to-Rail Output, 36V Zero-Drift Operational Amplifier</td>
<td>U4, U7, U10, U15</td>
<td>Texas Instruments</td>
<td>OPA188AIDBVT</td>
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<td>SOT-23 (DBV) 5</td>
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<td>-36V, -200mA, Ultralow-Noise, Negative Linear Regulator</td>
<td>U6</td>
<td>Texas Instruments</td>
<td>TPS7A3001DGNR</td>
<td>1</td>
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<td>MSOP-PowerPAD (DGN)</td>
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<td>Fitted</td>
<td>Positive High Voltage Hot Swap / Inrush Current Controller with Power Limiting, 10-pin MSOP, Pb-Free</td>
<td>U9</td>
<td>National Semiconductor</td>
<td>LMS069MM-2/NOPB</td>
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<td>MUB10A</td>
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<td>U11</td>
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<td>TPS7153DCK</td>
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<td>4242-VPK Small-Footprint and Low-Power Quad Channels Digital Isolators, DBQ0016A</td>
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<td>Texas Instruments</td>
<td>IS07141CCDBQ</td>
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<td>TPS7A1650DGNR</td>
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<td>Littelfuse Inc</td>
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9.3 PCB Layout

The Analog Output module is implemented in 4 layers PCB. For optimal performance of this design follow standard PCB layout guidelines, including proper decoupling close to all integrated circuits and adequate power and ground connections with large copper pours. Additional considerations must be made for providing robust EMC/EMI immunity. All protection elements should be placed as close to the output connectors as possible to provide a controlled return path for transient currents that does not cross sensitive components. To allow optimum current flow wide, low impedance, low-inductance traces should be used along the output signal path and protection elements. When possible copper pours are used in place of traces. Stitching the pours provides an effective return path around the PCB and helps reduce the impact of radiated emissions.

9.3.1 Layout Recommendations

In order to achieve a high performance, the below Layout Guidelines are recommended

1. Ensure that protection elements such as TVS diodes, capacitors are placed as close to connectors as possible to ensure that return current from high-energy transients does not cause damage to sensitive devices. Further use large and wide traces to ensure a low-impedance path for high-energy transients.
2. Place the decoupling capacitors close to supply pin of IC.
3. It is recommended to use multiple vias for power and ground for decoupling caps.
4. Current sense resistor must be routed as Kelvin Sense connection.
5. SPI lines: For signal integrity the termination resistances should be placed near to the source.
6. Each AVDD/AVSS should have decoupling capacitors placed close to the respective pins.
7. The reference capacitor should be placed close to the voltage reference input pin.

9.3.2 Layout Prints

To download the layer plots of the board, see the design files at: www.ti.com/tools/TIDA-00118
Top Layer
Inner Layer 1 Ground Plane
Inner Layer 2 Power Plane
Bottom Layer
Drill Drawing

<table>
<thead>
<tr>
<th>Symbol</th>
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Drill Table

- Total: 338
Mechanical Layer

![Mechanical Layer Diagram](image-url)
9.4 Altium Project

To download the Altium Project files for the board, see the design files at: www.ti.com/tools/TIDA-00118

9.5 Gerber files

To download the Gerber files for the board, see the design files at: www.ti.com/tools/TIDA-00118
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