TEST REPORT OF MPPT CHARGE CONTROLLER

PMP 7605
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I. INTRODUCTION

The following document is a compilation of test results of the PMP7605 reference design, a 20A MPPT solar charge controller. The test results are taken with simulated solar panel input corresponding to 12V and 24V panels.

II. DESCRIPTION

The PMP7605 is developed around the MSP430F5132 controller IC. The design is targeted for small and medium power solar charger solutions. The present design is capable of operating with 12V/24V panels and 12V/24V batteries with up to 20A output current. However, it can be easily adapted to 48V systems by just changing the MOSFETs to 100V rated parts. Also, it is possible to increase the current to 40A by using TO-220 package version of the same MOSFETs used in the design. The design has an operating efficiency of above 97% at full load in a 24V system. For 12V systems the efficiency is above 96%. This efficiency figure includes the losses in battery reverse protection MOSFET and panel reverse flow protection MOSFET, which are part of the design. The high efficiency is the result of the low gate charge MOSFETs from TI used in the design, and the interleaved buck topology used. The interleaved buck topology reduces the component stresses by a great extent. Another feature is the relatively small sized components used, possible due to the high operating frequency (~200 KHz per stage). The design has built-in battery charge profiles for 12V and 24V Lead acid batteries. The circuit takes only under 10mA of standby current while operating from battery. There is also a provision to connect a load to the battery with overload and short circuit cut-off built in. The design presently uses ‘perturb and observe’ algorithm for MPP tracking. This gives fast acquisition of MPP operation. Software programmable alarms and indications are provided in hardware, but are left non-configured.

Surge protection and EMI filtering components are not present on this design, and has to be added depending upon required specification levels.

III. BLOCK DIAGRAM
IV. SPECIFICATIONS

Input Voltage Range: 15VDC - 44VDC  
Output: 12V or 24V battery  
Output Current: 20A max.  
Board Form Factor: 130 mm x 84 mm x 22 mm  
Expected efficiency: >95%

V. BOARD LAYOUT AND ASSEMBLY
VI. TEST SETUP

Input conditions:
Panel input: 15VDC to 22VDC for 12V system or 30VDC to 44VDC for 24V system
Set current limit to the short circuit current of panel when DC source is used instead of panel

Output:
Electronic load in CV mode to simulate battery or 12/24V battery

Equipment Used:
1. Current limited DC source simulating solar panel
2. Digital Oscilloscope
3. Multimeters
4. Electronic load

Procedure:
1. Connect appropriate battery or electronic load in CV mode to the BAT+ and BAT- terminals of the PMP7605 reference board, maintaining correct polarity.
2. Connect panel or current limited DC source to PANEL+ and PANEL- terminals, maintaining correct polarity.
3. Set the output voltage of DC source to slightly above the MPP voltage of the panel being simulated (if DC source is used instead of panel) and turn on.
4. Observe for gradual build-up of output current.

VII. TEST DATA

a. 12V SYSTEM PERFORMANCE

<table>
<thead>
<tr>
<th>Vi (V)</th>
<th>Ii (A)</th>
<th>Vo (V)</th>
<th>Io (A)</th>
<th>Pi (W)</th>
<th>Po (W)</th>
<th>Efficiency (%)</th>
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<tbody>
<tr>
<td>17.70</td>
<td>0.01</td>
<td>0.00</td>
<td>0.00</td>
<td>0.14</td>
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<td>17.01</td>
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<td>96.2</td>
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<tr>
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<td>7.20</td>
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<td>258.88</td>
<td>248.70</td>
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b. 24V SYSTEM PERFORMANCE

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<td>0.0</td>
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<td>13.50</td>
<td>12.14</td>
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<td>24.15</td>
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<td>370.71</td>
<td>362.55</td>
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Efficiency can be dependent on the type of inductor used. The following plots indicate efficiency change with inductor type:

![Efficiency Graph](chart.png)
12V System Efficiency

24V System Efficiency
VIII. WAVEFORMS

a. Switching Node Waveforms

12V System, 20A Load. Individual channel switch nodes show interleaved operation

12V System, 10A Load. Individual channel switch nodes show interleaved operation
24V System, 15A Load. Individual channel switch nodes show interleaved operation

b. Gate waveforms

12V System, 20A Load. Top and bottom gate waveforms show dead-time implementation
24V System, 15A Load. Top and bottom gate waveforms show dead-time implementation

c. MPP Acquisition

12V System, 20A Load. Red: Input voltage, Yellow: Output current
24V System, 15A Load. Red: Input voltage, Yellow: Output current

File | Vertical | Timebase | Trigger | Display | Cursors | Measure | Math | Analysis | Utilities | Help

LeCroy

Timebase: 0.005
Channel: CH1
Height: 10.0 V/div
Offset: -20.00 V/div

Rise: 2.09 s/div
Hold: 0.5 V/div
Scale: 25 mV/div
Phase: Positive

April 10th, 2013

TII - Reference Designs
IX. SCHEMATIC

a. Power Stage
b. Controller and Bias Supply
<table>
<thead>
<tr>
<th>Item Qty</th>
<th>Reference</th>
<th>Value</th>
<th>Description</th>
<th>Part Number</th>
<th>Manufacturer</th>
<th>Part Number</th>
<th>Size</th>
<th>1K Web Price</th>
<th>Total (US$)</th>
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<td>1</td>
<td>R1, R2, R3</td>
<td>100uF</td>
<td>Capacitor, 50V, ±10%</td>
<td>C0605</td>
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<td>2</td>
<td>C4, C5, C6, C7</td>
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<td>Capacitor, Ceramic, 30V, X7R, 5%</td>
<td>Taiyo-Yuden</td>
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<td>010</td>
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<td>4</td>
<td>C10, C11, C19, C20, C28, C29</td>
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<td>Std</td>
<td>Std</td>
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<td>0.020</td>
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<td>5</td>
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<td>Std</td>
<td>Std</td>
<td>Std</td>
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<td>0.050</td>
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<tr>
<td>6</td>
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<td>Capacitor, Ceramic, 50V, X7R, 5%</td>
<td>Std</td>
<td>Std</td>
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<td>10</td>
<td>C27, C30, C34, C40</td>
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<td>Capacitor, Ceramic, 50V, X7R, 5%</td>
<td>Std</td>
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<td>0.003</td>
<td>0.007</td>
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</tbody>
</table>

X. BILL OF MATERIALS

(All non-TI parts’ costs (except Coilcraft) from DigiKey, TI parts from ti.com)
XI. CONCLUSION

The board is tested for the given specifications and found to meet them. Further optimization of software can be done depending on specific system requirements.
For Feasibility Evaluation Only, in Laboratory/Development Environments. The EVM is not a complete product. It is intended solely for use for preliminary feasibility evaluation in laboratory / development environments by technically qualified electronics experts who are familiar with the dangers and application risks associated with handling electrical / mechanical components, systems and subsystems. It should not be used as all or part of a production unit.

Your Sole Responsibility and Risk. You acknowledge, represent and agree that:

1. You have unique knowledge concerning Federal, State and local regulatory requirements (including but not limited to Food and Drug Administration regulations, if applicable) which relate to your products and which relate to your use (and/or that of your employees, affiliates, contractors or designees) of the EVM for evaluation, testing and other purposes.

2. You have full and exclusive responsibility to assure the safety and compliance of your products with all such laws and other applicable regulatory requirements, and also to assure the safety of any activities to be conducted by you and/or your employees, affiliates, contractors or designees, using the EVM. Further, you are responsible to assure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard.

3. Since the EVM is not a completed product, it may not meet all applicable regulatory and safety compliance standards (such as UL, CSA, VDE, CE, RoHS and WEEE) which may normally be associated with similar items. You assume full responsibility to determine and/or assure compliance with any such standards and related certifications as may be applicable. You will employ reasonable safeguards to ensure that your use of the EVM will not result in any property damage, injury or death, even if the EVM should fail to perform as described or expected.

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