TI Designs - Precision: Verified Design
Single-Supply Analog Input Module Reference Design with 16-Bit, 8-Channel ADC for PLC

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Design Resources
- Design Archive: All design files
- TINA-TI: SPICE simulator
- ADS8688: Product folder
- INA333: Product folder
- OPA320: Product folder
- OPA376: Product folder

Circuit Description
This design is for a 16-bit, 8-channel analog input module for industrial programmable logic controller (PLC) systems. The circuit is realized with an 8-channel, 16-bit, successive-approximation-register (SAR), analog-to-digital converter (ADC) with an integrated precision reference and analog front-end (AFE) circuit. The design explains the design process for implementing different voltage ranges, different current ranges, and temperature inputs for industrial PLC systems.

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1 Design Summary

The primary objective is to design a single-supply (5 V), 8-channel, analog input module. This design can be used to measure bipolar voltage ranges of ±10 V, ±5 V, and ±2.5 V, unipolar voltage ranges of 0 V to 5 V and 0 V to 10 V, a bipolar current range of ±20 mA, and a unipolar current range of 4 mA to 20 mA. The design also has a provision to measure temperature using resistance temperature detectors (RTDs).

The key specifications of the design are:

- System supply voltage: 5.5 V dc to 40 V dc
- ADC supply voltage (AVDD): 5 V dc
- Digital supply voltage (DVDD): 3.3 V dc
- Response time (for the ADC): 2 µs
- System input signal:
  - Voltage inputs: ±10 V, ±5 V, ±2.5 V, 0 V to 5 V, 0 V to 10 V
  - Current inputs: 4 mA to 20 mA, ±20-mA dc current
  - Temperature input: Pt100 RTD (a 200-Ω potentiometer is used to simulate an RTD).

The design goals and performance are summarized in Table 1. The measured ac performance for voltage inputs (±10 V) is illustrated in Figure 1.

Table 1. Comparison of Design Goal, Simulation, and Measured Performance

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>GOAL</th>
<th>SIMULATED, CALCULATED</th>
<th>MEASURED</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>VOLTAGE INPUTS</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Total error (% FSR), without calibration</td>
<td>±0.1%</td>
<td>±0.056%</td>
<td>0.042%</td>
</tr>
<tr>
<td>Voltage inputs: ±10 V</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Calibrated error</td>
<td>±0.05%</td>
<td>—</td>
<td>0.002%</td>
</tr>
<tr>
<td><strong>CURRENT INPUTS</strong></td>
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</tr>
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<td>Total error (% FSR), without calibration</td>
<td>±0.15%</td>
<td>±0.122%</td>
<td>0.028%</td>
</tr>
<tr>
<td>Current inputs: ±20 mA</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>Calibrated error</td>
<td>±0.05%</td>
<td>—</td>
<td>0.007%</td>
</tr>
<tr>
<td><strong>TEMPERATURE INPUT</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Total error (°C), without calibration</td>
<td>±2°C</td>
<td>±1.56°C</td>
<td>1.4°C</td>
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<tr>
<td>Temperature ranges of –40°C to 160°C</td>
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<td></td>
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</tr>
<tr>
<td>Calibrated error</td>
<td>±0.5°C</td>
<td>—</td>
<td>0.38°C</td>
</tr>
</tbody>
</table>
2 Theory of Operation

2.1 Overview of the Programmable Logic Controller (PLC)

The PLC is a programmable logic controller used to control industrial processes and machines. A basic PLC system consists of an analog input module, a CPU, and an analog output module. The analog input module interfaces with sensors (pressure, temperature, flow, and so forth) and converts the analog sensor output into digital. The CPU processes these digital values and provides a digital output that is converted by the analog output module for the actuators to control the industrial process. An example block diagram for the PLC is shown in Figure 2.

![Figure 1. Transfer Characteristics for the ±10-V Voltage Input Range](image)

The input for the analog input module can be as small as 10 mV from temperature sensors and can be as high as ±10 V from actuator controllers. The analog input module consists of a signal-conditioning circuit for filtering and amplification (or attenuation) of input signals, an ADC for conversion of analog signals into digital, and a circuit for isolation from the CPU and power-supply circuit.
The outputs of the analog output module are either the voltage outputs of ±10 V, ±5 V, 0 V to 10 V, and 0 V to 5 V for controlling the relays and actuators or are current outputs of ±20 mA, 0 mA to 20 mA, and 4 mA to 20 mA for process control. The analog output module consists of a digital-to-analog converter (DAC) for converting digital values from the CPU to analog, a signal-conditioning circuit to bring the output of the DAC to the desired voltage or current output range, and an isolation circuit for isolation from the CPU and power-supply circuit.

2.2 Analog Input Module

This TI Design discusses the design of a single-supply analog input module for the PLC. The key requirements for the analog input module for the PLC are high-voltage inputs and high-input impedance. Typically, a resolution of 12 to 16 bits with an overall accuracy of 0.1% to 0.2% is required for the analog input modules. Figure 3 shows the block diagram for the analog input module.

2.3 Considerations for Selecting the Architecture of the Analog Input Module

The analog input module for the PLC is generally used to measure the output of pressure sensors, rotatory encoders, proximity switches, temperature sensors, and so forth. These sensors are installed in the field to measure process variables (such as temperature, pressure, flow, and so forth) and the output of these sensors is either voltage or current output. Design the analog input module to measure the voltage and current outputs from these sensors.

A 24-V power bus is generally available for powering the analog input module. The 24-V field power bus can typically vary from 20 V to 30 V and can have transients up to 42 V. The noise or ripple on a 24-V bus can potentially couple in to input through the AFE or through the ADC. Therefore, an AFE and an ADC with high PSRR are preferred for the analog input module and a low-noise converter or linear regulator with transient immunity up to 42 V is used for powering analog input modules.

With the increasing number of input channels per module, the power and space available per channel is reduced. The analog input module for the PLC must measure an input voltage of ±10 V and a traditional AFE requires a bipolar supply (±15 V or ±12 V) to measure a signal of ±10 V. To generate a bipolar supply, an additional power converter is required. The additional power converter increases the power and space requirements of the analog input module. An AFE and ADC operating on a single supply (for example, 5 V) eliminates the need for an additional power converter and helps in reducing the space and power requirements for the analog input module.

System design goals (such as response time, resolution, accuracy, power consumption, and size) decide the architecture for the analog input module.
The processing cycle for a conventional PLC system is shown in Figure 4.

![Figure 4. PLC Process Cycle](image)

### 2.3.1 Scan Time

Scan time is the time difference between two consecutive readings that the PLC controller takes from a particular analog input channel. Scan time is typically the sum of response times of individual blocks of the PLC system. Scan time is generally in the order from a few milliseconds to 100 milliseconds. As the throughput per channel of the analog input module decreases, the scan time achieved for the PLC system increases.

### 2.3.2 Architectures for Analog Input Module

There can be two architectures for designing the analog input module for a PLC:

- **Simultaneous sampling with a separate ADC for each channel.**

  Simultaneous sampling is useful in systems that require signals to be sampled at the same instant. Because a separate ADC is used for each channel, the throughput (samples per second) from each channel is equal to the throughput of the ADC and the total throughput achieved from this architecture is the sum of the throughput of the ADCs on each channel. Power measurement is a common application in simultaneous sampling. Current and voltage signals are simultaneously sampled for calculating power. Simultaneous sampling requires an ADC for each channel, which leads to larger circuit size and higher power consumption.

- **Single ADC with multiplexed inputs.**

  A single ADC with multiplexed inputs samples the signal on each channel one by one in a sequence. The total throughput achieved from this architecture is the throughput of the ADC. The throughput of the ADC is divided among all the channels and the throughput per channel gets reduced. This architecture requires one ADC, one multiplexer, and multiple AFEs. This architecture generally has lower power and smaller circuit size than a simultaneous sampling architecture.

The second architecture is selected for this design report for its lower power consumption and smaller solution size. Because the throughput per channel in the second architecture with a single ADC gets reduced, an ADC with higher throughput is required to meet the scan time requirement. A SAR ADC with a sufficient throughput (> 100 kSPS, typically) is able to meet the scan time requirement of a typical PLC system.
2.4 Design Considerations for Voltage Inputs

The key requirement for the voltage inputs of an analog input module for the PLC is that they must accept voltage ranges of ±10 V, ±5 V, and ±2.5 V. Because the analog input module has a single ADC for all the input ranges, a programable gain amplifier (PGA) is required to scale and level shift the signals to the analog input ranges of the ADC. The PGA also scales the input signals to within the supply voltage and makes the operation of the analog input module possible on a single supply. Figure 5 provides the simplified circuit of a PGA and Equation 1 gives the dc transfer function of a PGA.

\[
V_{\text{out}} = \frac{R_f}{R_i} \times (V_1 - V_2) + V_b
\]

where:
- \( V_1, V_2 \) are input voltages to the PGA, and
- \( V_b \) is the bias voltage to level shift the output of the PGA.

The ADC output code can be calculated from Equation 2:

\[
\text{ADC\_Output\_Code} = \left[ \frac{R_f}{R_i} \times (V_1 - V_2) + V_b \right] \times \frac{1}{V_{\text{FSR}}} \times \left( 2^N - 1 \right)
\]

where
- \( V_{\text{FSR}} \) is full-scale input range of the ADC and
- \( N \) is the resolution of the ADC.
2.5 Design Considerations for the Current Inputs

In industrial process control, analog 4-mA to 20-mA and ±20-mA inputs are widely used for measuring process variables such as pressure and temperature. The benefits of the current loop are that the accuracy of the signal is not affected by voltage drops in interconnecting wiring. Even if there is significant voltage drop resulting from the wire resistance, the current-loop transmitter maintains the proper current up to its maximum voltage capability. A precision resistor is required to convert the current into voltage so that it can be measured by an ADC. The value of the precision resistor can be calculated from Equation 3.

\[ R_S = \frac{R_i}{R_f} \times \frac{V_{FSR}}{I_{S-max}} \]

where
- \( V_{FSR} \) is the full-scale input range of the ADC,
- \( I_{S-max} \) is the full-scale value of the current, and
- \( V_{FSR} \) is the full-scale input of the ADC.

A simplified circuit for current measurements is shown in Figure 6. The dc transfer function for current input is stated in Equation 4 and the ADC output code can be calculated from Equation 5.

![Figure 6. Simplified Circuit for Current Measurements](image)

\[ V_{out} = \frac{R_f}{R_i} \times (I_S - I_{IN}) \times R_S + V_b \]

where:
- \( V_{FSR} \) is the full-scale input range of the ADC,
- \( I_S \) is the full-scale current, and
- \( R_S \) is the sense resistor for measuring current.

\[ \text{ADC \_ OUTPUT \_ CODE} = \left( \frac{R_f}{R_i} \times (I_S - I_{IN}) \times R_S + V_b \right) \times \frac{1}{V_{FSR}} \times \left( 2^N - 1 \right) \]

where
- \( V_{FSR} \) is the full-scale input range of the ADC
- \( N \) is the resolution of the ADC.

Process variables such as pressure and temperature are nearly static in nature. The dc specifications (gain error, offset error, and INL error) of the analog input module become critical in designing the analog input module for measuring these variables. Gain error, offset error, and INL error contribute to the overall accuracy of the analog input module. As an example, the current output (±20 mA) from a pressure sensor must be measured with an accuracy of 20 µA for an overall accuracy of ±0.1% of the analog input module. For dc (static) conditions, the major portion of error is contributed by the gain error, the offset error, and INL. Total error for static conditions is calculated as the root of sum of squares of gain error, offset error, and INL.
## 2.6 Design Considerations for the Temperature Input

RTDs are sensors that are used to measure temperature by correlating resistance of the element with the temperature. According to the IEC751/ITS-90 standard, the resistance of a platinum resistance temperature detector can be derived from Equation 6.

For $T = -200^\circ C$ to $0^\circ C$

$$R_T = R_0 \times [1 + A \times T + B \times T^2]$$

For $T = 0^\circ C$ to $850^\circ C$

$$R_T = R_0 \times [1 + A \times T + B \times T^2 + C(1 - T)^3]$$

Where

- $R_T$ is RTD resistance at temperature $T$.
- $R_0$ is RTD resistance at 0°C.
- $A = 3.9083 \times 10^{-3} \, ^\circ C^{-1}$
- $B = -5.775 \times 10^{-7} \, ^\circ C^{-2}$
- $C = -4.182 \times 10^{-12} \, ^\circ C^{-4}$

A simplified schematic for temperature measurement using an RTD is shown in Figure 7.

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**A current source is required for exciting the RTD. A low-noise, low-offset, and low-drift operational amplifier is required to make a precise current source for exciting the RTD. The value of $I_{SET}$ is kept at 1 mA to limit the self-heating of the RTD. The excitation current can be derived from Equation 7.**

$$I_{SET} = \frac{V_{REF/2}}{R_{SET}}$$

A low-noise, high-input impedance instrumentation amplifier is required to amplify the voltage across the RTD. The gain required for this stage can be derived from Equation 8.

$$G_{INA} = \frac{V_{FSR}}{(I_{SET} \times R_{RTD-MAX})}$$

where:

- $I_{SET}$ is the excitation current for the RTD,
- $R_{RTD-MAX}$ is the maximum resistance of the RTD for the selected temperature range, and
- $V_{FSR}$ is the full-scale input range of the ADC.

**Equation 9** states the dc transfer function for the instrumentation amplifier stage:

$$V_{INA} = I_{SET} \times R_{RTD} \times G_{INA}$$

where

- $G_{INA}$ is the gain of the instrumentation amplifier

For the temperature range of $-40^\circ C$ to $160^\circ C$:

- $R_{RTD-MIN} = 84.27 \, \Omega$ at $T = -40^\circ C$.
- $R_{RTD-MAX} = 161.05 \, \Omega$ at $T = 160^\circ C$. 

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![Figure 7. Simplified Schematic for Temperature Measurement using an RTD](image-url)
Because the analog input module is designed to operate on a single supply, the output of the instrumentation amplifier can only swing between 0 V and the supply voltage (AVDD). An ADC with a single-ended input and full-scale input range less than the AVDD supply is required for temperature measurement in this analog module.

The output of the instrumentation gain stage covers only a fraction of the full-scale input range of the ADC. Therefore, the output of the instrumentation gain stage must be level shifted and amplified to match the full-scale input range of the ADC. Equation 10 states the dc transfer function for this stage.

\[
V_{OPA} = \left( V_{INA} - \frac{V_{REF}}{2} \right) \times \frac{R_2}{R_1}
\]

where:
- \( V_{OPA} \) is the output voltage of the operational amplifier and
- \( V_{INA} \) is the output voltage of the instrumentation amplifier.

Equation 11 states the complete transfer equation for the temperature input and the ADC output code for the temperature input can be calculated from Equation 12.

\[
V_{OUT} = \frac{R_2}{R_1} \times \left[ G_{INA} \times \frac{V_{REF}}{2} \times \frac{1}{R_{SET}} \times R_{RTD} - \frac{V_{REF}}{2} \right]
\]

\[
ADC\_Output\_Code = \frac{R_2}{R_1} \times \left[ G_{INA} \times \frac{V_{REF}}{2} \times \frac{1}{R_{SET}} \times R_{RTD} - \frac{V_{REF}}{2} \right] \times \frac{1}{V_{FSR}} \times (2^N - 1)
\]

The REF / 2 voltage is generated by a resistor divider from the \( V_{REF} \) voltage and buffered with an operational amplifier to provide a low-impedance REF / 2 source for driving the inverting input of the ADC driver. Figure 8 provides the schematic for the REF / 2 source.

![Figure 8. Schematic for the REF / 2 Source](image-url)

The design considerations for driving a SAR ADC can be found in section 2 of TI Design TIDU181.
2.6.1 Noise Analysis

The last stage for the circuit illustrated in Figure 7 is a level shift and ADC driver stage. The operational amplifier is configured for a differential input and a single-ended output. The total integrated noise at the output of the operational amplifier configured as a differential amplifier can be estimated by Equation 13.

\[
V_{\text{AMP-NOISE}} = \sqrt{\left(2 \cdot (I_n \cdot R_n) + \left(\frac{R_1 + R_2}{R_1}\right) \cdot 8kT \cdot \left(\frac{R_1 + R_2}{R_1}\right) \cdot \sqrt{\text{ENB}}\right)^2 + \left(\frac{E_{\text{INOUT}}}{R_1}\right)^2 + \left(\frac{E_{\text{REF}/2}}{R_1}\right)^2 + \left(\frac{V_{1/f,\text{AMP_PP}}}{6.6}\right)^2}
\]

where:
- \(V_{\text{AMP-NOISE}}\) is the total integrated RMS noise at the output of the operational amplifier,
- \(I_n\) is the white current noise specification of the operational amplifier (\(\text{A/}\sqrt{\text{Hz}}\)),
- \(V_n\) is the white voltage noise specification of the operational amplifier (\(\text{V/}\sqrt{\text{Hz}}\)),
- \(E_{\text{INOUT}}\) is the total noise at the output of the instrumentation amplifier (\(\text{V RMS}\)),
- \(E_{\text{REF}/2}\) is the total noise at the REF / 2 output (\(\text{VRMS}\)),
- \(V_{1/f,\text{AMP_PP}}\) is the flicker noise specification of the operational amplifier specified as peak-to-peak noise (\(\text{V}_{\text{pp}}\)), and
- \(\text{ENB}\) is the effective noise bandwidth.

Details for noise analysis in operational amplifiers can be found in application report SLVA043.

For an ADC with an input range of \(V_{\text{FSR}}\), the RMS value of the input-referred noise can be found from the specified value of SNR in the data sheet by using Equation 14.

\[
V_{n,\text{ADC}_\text{RMS}} = \frac{V_{\text{FSR}}}{2\sqrt{2}} \times 10^{\frac{\text{SNR (dB)}}{20}}
\]

where:
- \(V_{n,\text{ADC}_\text{RMS}}\) is the RMS noise at the input of the ADC and
- \(V_{\text{FSR}}\) is the full-scale input range of the ADC.

The total noise for a temperature measurement system is the root sum square (RSS) of the noise at the output of the amplifier and the input-referred noise of the ADC. The system noise for a temperature input can be calculated using Equation 15.

\[
V_{\text{SYS-NOISE}} = \sqrt{\left(V_{\text{AMP-NOISE}}^2 + V_{n,\text{ADC}_\text{RMS}}^2\right)}
\]
3 Component Selection

3.1 Selection of ADC

The analog input module requires a SAR ADC with multiplexed inputs, a programable input voltage range on each input, and high input impedance. The ADC must be capable of accepting input ranges of ±10V, ±5 V, 0 V to 5 V, and 0 V to 2.5 V and must include an integrated reference. The ADC must have a throughput greater than 500 kSPS to achieve a response time of 2 µs. The gain error, offset error, and INL of the ADC must be less than 0.05% FSR to achieve an overall accuracy of 0.1%

With all these requirements, the ADS8688 is found to be suitable for this design. Each channel of the ADS8688 can be programmed to any of the above voltage ranges by programming the registers of the device. The ADS8688 also provides a constant input impedance of 1 MΩ for channels AIN_0P to AIN_7P. The auxiliary channel of the ADS8688 with a single-ended input range of V_REF makes the device suitable for temperature input.

3.2 Voltage Inputs

The ADS8688 can directly accept voltage inputs of ±10.24 V, ±5.12 V, ±2.56 V, 0 V to 10.24 V, and 0 V to 5.12 V. Any additional components are not required for voltage inputs.

3.3 Current Inputs

A precision resistor is required to convert the current into voltage. The input range selected for current measurements is ±5.12 V for a ±20-mA current input. A lower input range is selected to provide headroom for the voltage drop across connecting wires and to provide flexibility in selecting the voltage supply for the current-loop transmitter. According to Equation 3, the value of the precision resistance for the current input of ±20 mA and 4 mA to 20 mA comes out to be 256 Ω. The tolerance of the current-sensing resistor directly affects the gain error in current measurement, and thus a 0.1%, 249-Ω resistor is used for sensing current for current inputs.

3.4 Temperature Input

An ADC with a single-ended input and full-scale input range less than the AVDD supply is required for the temperature input in a single-supply analog module. Therefore, the auxiliary channel of the ADS8688 is selected for the temperature input because this channel has a full-scale input range of V_REF (4.096 V).

3.4.1 Current Source

The key specifications for the amplifier for the current source are low noise, low offset, and low drift. The amplifier must be able to provide an output current of 1 mA. The OPA376 amplifier is a low-noise amplifier with outstanding dc precision and ac performance. The OPA376 offers a low offset voltage (25 µV, max), low noise (7.5 nV/√Hz), and low drift (2 µV/°C max). These features make the device suitable for a precision current source. The value of R_SET can be calculated by Equation 7 as 2.048 kΩ.

A 2-kΩ (0.1%) resistor is selected for R_SET.
3.4.2 Instrumentation Gain Stage

The key requirements for this stage are low noise, low offset, low offset drift, and single-supply operation.

The INA333 has low offset (25 µV), excellent offset voltage drift (0.1 µV/°C), low noise density (50 nV/√Hz), and can operate from a single supply. The INA333 has auto calibration techniques that ensure precision over the industrial temperature range. These features make the INA333 ideal for temperature measurement applications using RTDs.

The gain required for the instrumentation stage can be calculated from Equation 8. The selected temperature range is −40°C to 160°C. \( R_{RTD-MAX} = 161.05 \, \Omega \) at \( T = 160°C \). \( G_{INA} = 25.46 \, V/V \).

The value for the gain-setting resistor for the INA333 can be calculated by Equation 16.\[ R_G = 100 \, k\Omega / (G_{INA} - 1) \]A 4.12-kΩ (0.1%) resistor is selected for \( R_G \).

3.4.3 REF / 2 Source

The key specifications for the amplifier for the REF / 2 source are low noise, low offset, and low drift. The OPA376 amplifier is a low-noise amplifier with outstanding dc precision and ac performance. The OPA376 offers a low offset voltage (25 µV, max), low noise (7.5 nV/√Hz), and low drift (2 µV/°C max).

3.4.4 Level Shift and ADC Driver Stage

The gain required for the level shift and ADC driver stage can be found by Equation 10 with \( V_{OPA} = V_{REF} \) and \( V_{INA} = V_{REF} \). The gain for this stage is estimated to be 2 V/V. The tolerance of resistors \( R_2 \) and \( R_1 \) for setting gain contribute to the gain error. \( R_2 \) and \( R_1 \) are selected to be 4.02 kΩ and 2.00 kΩ, respectively, with a tolerance of 0.1%. The amplifier is selected to be the OPA320, \( R_{FLT} \) to be 50 Ω, and \( C_{FLT} \) to be 3 nF, as per the design guidelines provided in section 2 of TI Design TIDU181.

Using Equation 13, the total noise at the output of the ADC driver configured as a differential amplifier is estimated to be:

\[ V_{AMP-NOISE} = 32.2 \, \mu V \, \text{RMS} \]

- \( I_N = 0.6 \, fA/\sqrt{Hz} \), \( E_N = 8.5 \, nV/\sqrt{Hz} \), and \( V_{1/f, AMP, PP} = 2.8 \, \mu V_{PP} \) for the OPA320.
- \( R_2 = 4.02 \, k\Omega \), \( R_1 = 2 \, k\Omega \), and \( T = 298 \, K \).
- \( E_{ENB} = 0.8333 \, MHz \) for \( R_{FLT} = 50 \, \Omega \) and \( C_{FLT} = 3 \, nF \).
- \( E_{INA-OUT} = 5.49 \, \mu V \, \text{RMS} \) and \( E_{REF/2} = 7.188 \, \mu V \, \text{RMS} \) from simulation results in Section 4.1.4 and Section 4.1.5.

Using Equation 14, the input-referred noise for the auxiliary channel of the ADS8688 is calculated to be 57.3 µVRms.

With Equation 15, the total system noise for the temperature input is estimated to be 65.7 µVRms.
4 Simulation and Circuit Performance Calculations

4.1 TINA-TI Simulation

4.1.1 DC Transfer Characteristics for Voltage inputs

The TINA-TI schematic shown in Figure 9 is used to simulate the dc transfer characteristics. The input range is selected by setting the voltage for the MODE pin. A dc voltage source is connected at the analog inputs of the ADS8688 model for simulating the voltage output. Figure 10 provides the simulation result for dc transfer characteristics for a voltage range of ±10 V.

![Figure 9. TINA-TI Schematic for the ADS8688 with Voltage Inputs](image)

![Figure 10. TINA-TI Simulation Result: DC Transfer Characteristics for Voltage Inputs](image)
4.1.2 DC Transfer Characteristics for Current Inputs

The TINA-TI schematic shown in Figure 11 is used to simulate the dc transfer characteristics. The model of the ADS8688 in TINA-TI is used with a current-sense resistance for simulation. The input range is selected by setting the voltage for the MODE pin. A dc current source is connected at the analog inputs of the ADS8688 model for simulating the current-loop output.

![Figure 11. TINA-TI Schematic for the ADS8688 with Current Inputs](image1)

Figure 12 shows the dc transfer characteristics for the circuit illustrated in Figure 11 for current range of ±20 mA.

![Figure 12. TINA-TI Simulation Result: DC Transfer Characteristics for Current Inputs](image2)
4.1.3 DC Transfer Characteristics for Temperature Inputs

The TINA-TI schematics illustrated in Figure 13 and Figure 15 are used to check the dc transfer characteristics for stages of temperature input. Figure 14 and Figure 16 illustrate the simulation results. DC transfer characteristics are plotted for an RTD resistance of 85 Ω to 161 Ω. DC transfer characteristics are simulated to check for saturation of the output when the output reaches close to the supply rails. The ideal gain for this stage is also calculated from the dc transfer characteristics.

![TINA-TI Schematic for the RTD Current Source and Instrumentation Amplifier](image1)

**Figure 13. TINA-TI Schematic for the RTD Current Source and Instrumentation Amplifier**

![TINA-TI Simulation Result: DC Transfer Characteristics for the RTD Current Source and Instrumentation Amplifier](image2)

**Figure 14. TINA-TI Simulation Result: DC Transfer Characteristics for the RTD Current Source and Instrumentation Amplifier**

The ideal gain for this stage is calculated as $\Delta V_{INA} / \Delta R_{RTD}$. The gain for this stage is calculated to be 25.875 mV/Ω.
The ideal gain for this stage is calculated as $\frac{\Delta V_{ADC}}{\Delta V_{INA}}$. The gain for this stage is estimated to be 2.0099 V/V.

The total gain for the temperature input is the multiplication of the gain of the two stages. The total gain is calculated to be 52.006 mV/Ω.
4.1.4 Noise Simulation for the REF / 2 Source

Figure 17 shows the TINA-TI schematic for the REF / 2 source and Figure 18 provides the total noise (Vrms) at the output of the REF / 2 source.

![Figure 17. TINA-TI Schematic for the REF / 2 Source](image)

![Figure 18. Total Noise at the Output of the REF / 2 Source](image)
4.1.5 Noise Simulation for the Instrumentation Amplifier Stage

Figure 19 shows the TINA-TI™ for the current source and the INA333. The noise at the output of the INA333 is simulated in TINA-TI to get the total system noise for the temperature input. Figure 20 provides the total noise at the output of INA333. A low-pass RC filter is placed at the output of the INA333 to limit noise.

Figure 19. TINA-TI Schematic for the Current Source and the INA333

Figure 20. Total Noise at the Output of the INA333
4.2 Circuit Performance Calculations

The total error is calculated for voltage, current, and temperature inputs in the sections below.

4.2.1 Analyzing Total Error for Voltage Inputs

Table 2. Total Error for Voltage Inputs

<table>
<thead>
<tr>
<th>Error Source</th>
<th>Error Contributed (%FSR)</th>
<th>Comments</th>
<th>Calculated Error (% FSR)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain error contributed by the PGA and ADC</td>
<td>GE_{ADC, PGA} %</td>
<td>Gain error is specified as ±0.05%FSR for the ADS8688.</td>
<td>±0.05%</td>
</tr>
<tr>
<td>Offset error contributed by the ADC and PGA</td>
<td>(R_i / R_{i} \times OE_{ADC, PGA}) / V_{FSR} %</td>
<td>Offset error is specified as ±0.75 mV for the ADS8688. R_i / R_{i} is the gain of the PGA. V_{FSR} = V_{REF}.</td>
<td>±0.004%</td>
</tr>
<tr>
<td>Gain error contributed by the initial accuracy of the reference</td>
<td>Ref_error / V_{REF} %</td>
<td>Ref_error is the error in the initial voltage of the reference. Ref_error is specified as ±1 mV for the ADS8688.</td>
<td>±0.024%</td>
</tr>
<tr>
<td>INL contributed by the ADC and PGA</td>
<td>INL_{ADC, PGA} / (2^n)%</td>
<td>INL is specified as ±2 LSB for the ADS8688.</td>
<td>±0.003%</td>
</tr>
</tbody>
</table>

Total Error (Root of Sum of Squares) ±0.056%

For the voltage input range of ±10 V, the input range of ±10.24 V is selected for the ADS8688. The PGA has a gain (R_i / R_{i}) of 0.2 for the input range of ±10.24 V.

4.2.2 Analyzing Total Error for Current Inputs

Table 3. Total Error Analysis for Current Inputs

<table>
<thead>
<tr>
<th>Error Source</th>
<th>Error Contributed (%FSR)</th>
<th>Comments</th>
<th>Calculated Error (% FSR)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain error caused by tolerance of the sense resistor, R_s</td>
<td>t %</td>
<td>t is the tolerance of the sense resistor. t = 0.1%.</td>
<td>±0.1%</td>
</tr>
<tr>
<td>Gain error caused by input impedance of the PGA(^{(1)})</td>
<td>I_{IN} / I_{S} %</td>
<td>I_{IN} is the current into the pin of the PGA. I_{S} is the full-scale input current.</td>
<td>±0.04%</td>
</tr>
<tr>
<td>Gain error contributed by the PGA and ADC</td>
<td>GE_{ADC, PGA} %</td>
<td>Gain error is specified as ±0.05% FSR for the ADS8688.</td>
<td>±0.05%</td>
</tr>
<tr>
<td>Offset error caused by input impedance of the PGA(^{(1)})</td>
<td>(R_i / R_{i} \times I_{IN} \times R_{S}) / V_{FSR} %</td>
<td>Offset error caused by current from the PGA pins when I_{S} = 0. R_i / R_{i} is the gain of the PGA. V_{FSR} = V_{REF}.</td>
<td>±0.012%</td>
</tr>
<tr>
<td>Offset error contributed by the ADC and PGA</td>
<td>(R_i / R_{i} \times OE_{ADC, PGA}) / V_{FSR} %</td>
<td>Offset error is specified as ±1 mV for the ADS8688. V_{FSR} = V_{REF}.</td>
<td>±0.0097%</td>
</tr>
<tr>
<td>Gain error contributed by initial accuracy of the reference</td>
<td>Ref_error / V_{REF} %</td>
<td>Ref_error is the error in initial voltage of the reference. Ref_error is specified as ±1 mV for the ADS8688.</td>
<td>±0.024%</td>
</tr>
<tr>
<td>INL contributed by the ADC and PGA</td>
<td>INL_{ADC, PGA} / (2^n)%</td>
<td>INL is specified as ±2 LSB for the ADS8688.</td>
<td>±0.003%</td>
</tr>
</tbody>
</table>

Total Error (Root of Sum of Squares) ±0.122%

\(^{(1)}\) I_{IN} can be calculated from the equation given in the Electrical Characteristics table in the ADS8688 data sheet (SBAS582).

For the current input range of ±20 mA, the input range of ±5.12 V is selected for the ADS8688. The PGA has a gain (R_i / R_{i}) of 0.4 for the input range of ±5.12 V.
4.2.3 Analyzing Total Error for Temperature Inputs

Table 4. Total Error Analysis for Temperature Inputs

<table>
<thead>
<tr>
<th>Error Source</th>
<th>Error Contributed (%FSR)</th>
<th>Comments</th>
<th>Calculated Error (%FSR)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Errors in the REF / 2 Source</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Offset error of the operational amplifier</td>
<td>OE_{OPA} / (V_{REF} / 2)%</td>
<td>Offset error is specified as 25 µV for the OPA376.</td>
<td>±0.0012%</td>
</tr>
<tr>
<td>Reference error</td>
<td>Ref_error / V_{REF}%</td>
<td>Ref_error is the error in the initial voltage of the reference. Ref_error is specified as ±1 mV for the ADS8688.</td>
<td>±0.024%</td>
</tr>
<tr>
<td>Tolerance of resistors(^{(1)})</td>
<td>t / √2%</td>
<td>t is the tolerance of the resistors. t = 1%.</td>
<td>±0.7%</td>
</tr>
<tr>
<td>Errors in the Current Source</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Tolerance of R_{S}</td>
<td>t%</td>
<td>t is the tolerance of the resistor for setting the RTD current. t = 0.1%.</td>
<td>±0.1%</td>
</tr>
<tr>
<td>Offset error of the operational amplifier</td>
<td>OE_{OPA} / (V_{REF} / 2)%</td>
<td>Offset error is specified as 25 µV for the OPA376.</td>
<td>±0.0012%</td>
</tr>
<tr>
<td>Errors in the Level Shift and ADC Driver</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Offset error of the operational amplifier</td>
<td>OE_{OPA} / (V_{REF} / 2)%</td>
<td>Offset error is specified as 150 µV for the OPA320.</td>
<td>±0.007%</td>
</tr>
<tr>
<td>Tolerance of gain setting resistors R1, R2(^{(2)})</td>
<td>√Z t%</td>
<td>t is the tolerance of the resistors R1, R2. t = 0.1%.</td>
<td>±0.14%</td>
</tr>
<tr>
<td>Errors in the AUX Channel of the ADS8688</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Offset error</td>
<td>OE_{ADC} / V_{FSR}%</td>
<td>Offset error is specified as 10 mV for the AUX channel of the ADS8688. V_{FSR} = V_{REF}.</td>
<td>±0.24%</td>
</tr>
<tr>
<td>Gain error</td>
<td>GE_{ADC}%</td>
<td>Gain error is specified as 0.2 % for the AUX channel of the ADS8688.</td>
<td>±0.2%</td>
</tr>
<tr>
<td>INL</td>
<td>INL_{ADC} / (2^N)%</td>
<td>INL is specified as ±4 LSB for the AUX channel of the ADS8688.</td>
<td>±0.006%</td>
</tr>
<tr>
<td>Total Error (Root of Sum of Squares)</td>
<td></td>
<td></td>
<td>±0.78% or ±1.56°C</td>
</tr>
</tbody>
</table>

\(^{(1)}\) See Section 10.1.
\(^{(2)}\) See Section 10.2.

For the temperature input, the auxiliary channel of the ADS8688 is used. For the temperature input range of –40°C to 160°C, the full-scale input range is 200°C.
5 PCB Design

The printed circuit board (PCB) schematic and bill of materials can be found in Section 10.

Use a ground plane underneath the device and partition the PCB into analog and digital sections. Avoid crossing digital lines with the analog signal path and keep the analog input signals and the reference input signals away from noise sources. In this board layout, the analog input and reference signals are routed on the top layer of the board and the digital connections are routed on the bottom of the board.

The power sources to the ADS8688 must be clean and well-bypassed. Avoid placing vias between the AVDD and DVDD pins and the bypass capacitors. Connect all the ground pins to the ground plane using short, low-impedance paths.

There are two decoupling capacitors used for the REFCAP pin. The first is a small 1-µF ceramic capacitor placed close to the device pins for decoupling the high-frequency signals and the second is a 22-µF ceramic capacitor to provide the charge required by the reference circuit of the ADS8688. Both of these capacitors must be directly connected to the pins of the device without any vias between the pins and the capacitors.

The PCB layout for this design is shown in Figure 21.

5.1 PCB Layout

Figure 21. PCB Layout
6 Verification and Measured Performance

The measurement results for verification of this TI Precision Design are listed in this section.

6.1 Measured Performance for Voltage Inputs

The performance for the voltage inputs is measured by providing dc voltage from –10 V to 10 V and capturing the output code of the ADS8688. With \( R_f / R_i = 0.2 \), \( V_b = 2.048 \) V, \( V_{FSR} = 4.096 \) V, and \( N = 16 \), for an input range of ±10.24 V in the ADS8688, Equation 2 can be simplified as Equation 17:

\[
ADC_{Output\ Code} = \left( \frac{0.2 \times V_{IN} + 2.048}{4.096} \right) \times 65535
\]  

Figure 22 and Figure 23 provide the transfer characteristics and total error for voltage input. The total error is calculated as the difference between the expected output code obtained from Equation 17 and the measured output code. The reference and offset of the ADS8688 are calibrated to obtain the calibrated total error.

![Figure 22. Transfer Characteristics for Voltage Inputs](image-url)
Max total error without calibration = –0.042%, max total error with calibration = 0.002%

**Figure 23. Total Error for Voltage Inputs**

**6.2 Measured Performance for Current Inputs**

The performance for the current inputs is measured by providing dc current from –20 mA to 20 mA and capturing the output code of the ADS8688. With \( R_f / R_i = 0.4 \) V, \( V_b = 2.048 \) V, \( V_{FSR} = 4.096 \) V, and \( N = 16 \) for an input range of ±5.12 V in the ADS8688, **Equation 5** can be simplified as **Equation 18**:

\[
ADC\_OUTPUT\_CODE = \left( \frac{0.4 \times (I_s - I_{IN}) \times R_s + 2.048}{4.096} \right) \times 65535
\]

**Figure 24 and Figure 25** provide the transfer characteristics and total error for current input. The total error is calculated as difference between the expected output code obtained from **Equation 18** and the measured output code. The reference of the ADS8688 and current sense resistor (\( R_s \)) are calibrated to obtain the calibrated total error.
Figure 24. Transfer Characteristics for Current Input

Figure 25. Total Error for Current Input

Max total error without calibration = –0.028%, max total error with calibration = –0.007%
6.3 Measured Performance for the Temperature Input

The performance for the temperature input is measured by connecting a potentiometer of 200 Ω in place of a Pt100 RTD and varying the resistance from 85 Ω to 160 Ω. With $R_2 / R_1 = 2.01$ V, $G_{\text{INA}} = 25.27$ V/V, $V_{\text{FSR}} = 4.096$ V, and $N = 16$ for an input range of 0 V to 4.096 V for the AUX channel in the ADS8688, Equation 2 can be simplified as Equation 19:

$$\text{ADC Output Code} = 1.005 \times \left[ \frac{25.27 \times R_{\text{RTD}}}{2000} - 1 \right] \times 65535$$  \hspace{1cm} (19)

Figure 26 and Figure 27 provide the transfer characteristics and total error for temperature input. The total error is calculated as the difference between the expected output code obtained from Equation 19 and the measured output code. The REF / 2 source and the current source are calibrated to obtain the calibrated total error.

![Transfer characteristics for temperature input](image.png)

Figure 26. Transfer Characteristics for Temperature Input
Max total error without calibration = –1.4°C, max total error with calibration = 0.38°C

**Figure 27. Total Error for Temperature Input**

The system noise for the temperature input is measured by capturing 32768 samples for an input close to mid scale. Figure 28 shows the histogram of samples captured. The system noise is calculated using the sigma of the codes and LSB size. The system noise is found to be 57.5 μVrms.

Sigma = 0.92, mean code = 32325.78, peak code = 32326

**Figure 28. DC Histogram for the Temperature Input**
7 Modifications

7.1 Improving the Temperature Drift

The temperature drift can be improved by using an external reference for the ADS8688 and a zero-drift operational amplifier for the REF / 2 source and current source. Table 5 and Table 6 provide suggestions for an external reference and alternative operational amplifier for the current source and REF / 2 source.

Table 5. External Reference for the ADS8688

<table>
<thead>
<tr>
<th>REFERENCE</th>
<th>INITIAL ACCURACY (%)</th>
<th>NOISE (µVpp) (F = 0.1 Hz to 10 Hz)</th>
<th>MAX TEMPERATURE DRIFT (ppm/°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>REF5040I</td>
<td>±0.05</td>
<td>12</td>
<td>3</td>
</tr>
</tbody>
</table>

Table 6. Alternative Operational Amplifier for the Current Source and REF/2 Source

<table>
<thead>
<tr>
<th>ALTERNATIVE OP AMP</th>
<th>MAX OFFSET VOLTAGE (µV)</th>
<th>NOISE (µVpp) (F = 0.1 Hz to 10 Hz)</th>
<th>MAX OFFSET VOLTAGE DRIFT (µV/°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPA378</td>
<td>50</td>
<td>0.4</td>
<td>0.25</td>
</tr>
</tbody>
</table>

7.2 Increasing the Temperature Range for Temperature Input

The components selected for this design are based on the design goals outlined at the beginning of the design process. The temperature input is designed for a Pt100 RTD for a temperature range of –40°C to 160°C. The temperature input can be optimized for a complete temperature range of –200°C to 850°C by changing the circuit for the temperature input as per the schematic shown in Figure 29. Table 7 provides the value of R_G for a temperature range of –200°C to 850°C.

Figure 29. Schematic for the Temperature Input for the Range of –200°C to 850°C

Table 7. Selecting Different Temperature Ranges for the Temperature Input

<table>
<thead>
<tr>
<th>S.NO.</th>
<th>MINIMUM TEMPERATURE</th>
<th>R_RTDMIN</th>
<th>MAXIMUM TEMPERATURE</th>
<th>R_RTDMAX</th>
<th>R_G</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>–200°C</td>
<td>18.52 Ω</td>
<td>850°C</td>
<td>390.48 Ω</td>
<td>11 kΩ</td>
</tr>
</tbody>
</table>
About the Author

Lokesh Ghulyani is a systems engineer in the SAR-ADC team at Texas Instruments (TI) based in Bangalore, India. Prior to this role, he worked as an analog application engineer at TI. Lokesh earned his Bachelor of Technology Degree from the Indian Institute of Technology, Varanasi in India.

References and Acknowledgments

2. Vaibhav Kumar and Rafael Ordonez. 16-bit, 400KSPS, 4-Channel Multiplexed Data Acquisition System for High Voltage Inputs with Lowest Distortion (TIDU181). Available: TIDU181
10 Appendix

10.1 Error Due to Tolerance of Resistors in REF / 2 Source

The transfer function for the circuit shown in Figure 30 can be calculated as Equation 20.

\[ V_{REF/2} = V_{REF} \times \frac{R_4(1 + t_1)}{R_4(1 + t_1) + R_4(1 + t_2)} \]

where

- \( t_1 \) and \( t_2 \) are the tolerance of individual resistors. \( \text{(20)} \)

Equation 20 is simplified in the following steps:

\[ V_{REF/2} = V_{REF} \times \frac{(1 + t_1)}{(2 + t_1 + t_2)} \] \( \text{(21)} \)

\[ V_{REF/2} = \frac{V_{REF}}{2} \times \frac{(1 + t_1)}{1 + (\frac{t_1 + t_2}{2})} \] \( \text{(22)} \)

\[ V_{REF/2} = \frac{V_{REF}}{2} \times (1 + \frac{(t_1 - t_2)}{2}) \] \( \text{(23)} \)

Because \( t_1 \) and \( t_2 \ll 1 \), the maximum value of tolerance \( \frac{(t_1 - t_2)}{2} \) is \( \frac{|t_1| + |t_2|}{2} \) or \( t \).

The R.S.S value of tolerance is \( \sqrt{\frac{t_1^2 + t_2^2}{2}} \) or \( t/\sqrt{2} \).
10.2 Errors Due to Tolerance of Resistors in Level Shift and ADC Driver

The transfer function for the circuit shown in Figure 31 can be calculated as Equation 24.

\[ V_{out} = (V_{INA} - V_{REF/2}) \times \frac{R_2(1 + t_1)}{R_1(1 + t_2)} \]

where
- \( t_1 \) and \( t_2 \) are the tolerance of individual resistors.

**Equation 24** is simplified in the following steps:

\[ V_{out} = K \times \frac{2R(1 + t_1)}{R(1 + t_2)} \]

where
- \( R_2 = 2R, R_1 = R \).

**Equation 25**

\[ V_{out} = K \times 2(1 + t_1 - t_2) \]

**Equation 26**

Because \( t_1 \) and \( t_2 \ll 1 \), the maximum value of tolerance is \( |t_1| \) + \( |t_2| \) or \( 2t \).

R.S.S value of tolerance is \( \sqrt{t_1^2 + t_2^2} \) or \( \sqrt{2}t \).
10.3 Electrical Schematic and Bill of Materials

The electrical schematic and bill of materials for this design are respectively shown in Figure 32 and Table 8.

Figure 32. Electrical Schematic
### Table 8. Bill of Materials

<table>
<thead>
<tr>
<th>Designator</th>
<th>Quantity</th>
<th>Value</th>
<th>Description</th>
<th>Package Reference</th>
<th>PartNumber</th>
<th>Manufacturer</th>
</tr>
</thead>
<tbody>
<tr>
<td>IPCB</td>
<td>1</td>
<td></td>
<td>Printed Circuit Board</td>
<td></td>
<td>6580143</td>
<td>Any</td>
</tr>
<tr>
<td>C1, C2, C3, C6, C7</td>
<td>5</td>
<td>0.1uF</td>
<td>CAP, CERM, 0.1uF, 25V, +/-5%, X7R, 0603</td>
<td>0603</td>
<td>06030C104JAT2AAVX</td>
<td>AVX</td>
</tr>
<tr>
<td>C4</td>
<td>1</td>
<td>220pF</td>
<td>CAP, CERM, 220pF, 100V, +/-10%, X7R, 0603</td>
<td>0603</td>
<td>06030C221KAT2A</td>
<td>AVX</td>
</tr>
<tr>
<td>C17</td>
<td>1</td>
<td>10uF</td>
<td>CAP, CERM, 10uF, 10V, +/-20%, X5R, 0603</td>
<td>0603</td>
<td>C1608X5R1A106M</td>
<td>TDK</td>
</tr>
<tr>
<td>C24</td>
<td>1</td>
<td>1uF</td>
<td>CAP, CERM, 1uF, 10V, +/-10%, X5R, 0603</td>
<td>0603</td>
<td>C06030C105K8ACTU</td>
<td>Kemet</td>
</tr>
<tr>
<td>C5</td>
<td>1</td>
<td>10uF</td>
<td>CAP, CERM, 10uF, 6.3V, +/-20%, X7R, 0603</td>
<td>0603</td>
<td>C06030C106M9ACTU</td>
<td>Kemet</td>
</tr>
<tr>
<td>C8</td>
<td>1</td>
<td>22uF</td>
<td>CAP, CERM, 2.2uF, 16V, +/-20%, X7R, 1210</td>
<td>1210</td>
<td>C3225X7R1C226M</td>
<td>TDK</td>
</tr>
<tr>
<td>C9, C63</td>
<td>2</td>
<td>1uF</td>
<td>CAP, CERM, 1uF, 16V, +/-10%, X7R, 0603</td>
<td>0603</td>
<td>C1608X7R1C105K</td>
<td>TDK</td>
</tr>
<tr>
<td>C10</td>
<td>1</td>
<td>1uF</td>
<td>CAP, CERM, 1uF, 16V, +/-10%, X7R, 0603</td>
<td>0603</td>
<td>C06030C105K4ACTU</td>
<td>Kemet</td>
</tr>
<tr>
<td>C11</td>
<td>1</td>
<td>3000pF</td>
<td>CAP, CERM, 3000pF, 50V, +/-5%, C0G/NP0, 0603</td>
<td>0603</td>
<td>GRM1885C1H302JA01D</td>
<td>MuRata</td>
</tr>
<tr>
<td>C26</td>
<td>1</td>
<td>0.01uF</td>
<td>CAP, 1000pF, 0603, 5%, 50V, COG</td>
<td>0603</td>
<td>C1608C0G1H103J080AA</td>
<td>TDK</td>
</tr>
<tr>
<td>C12, C13, C14, C15, C18, C19, C20, C21</td>
<td>8</td>
<td>NI</td>
<td>Capacitor Not Installed</td>
<td>0603</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>C16</td>
<td>1</td>
<td>0.022uF</td>
<td>CAP, CERM, 0.022uF, 25V, +/-10%, X7R, 0603</td>
<td>0603</td>
<td>C06030C223K3RACTU</td>
<td>Kemet</td>
</tr>
<tr>
<td>C25</td>
<td>1</td>
<td>2.2uF</td>
<td>CAP, CERM, 2.2uF, 16V, +/-10%, X7R, 0805</td>
<td>0805</td>
<td>C08050C225K4RACTU</td>
<td>Kemet</td>
</tr>
<tr>
<td>C62</td>
<td>1</td>
<td>10uF</td>
<td>CAP, CERM, 10uF, 16V, +/-10%, X7R, 0805</td>
<td>0805</td>
<td>GRM21BR71A106KE51L</td>
<td>MuRata</td>
</tr>
<tr>
<td>C64</td>
<td>1</td>
<td>0.1uF</td>
<td>CAP, CERM, 0.1uF, 50V, +/-10%, X7R, 0603</td>
<td>0603</td>
<td>06035C104KAT2A</td>
<td>AVX</td>
</tr>
<tr>
<td>D1</td>
<td>1</td>
<td>30V</td>
<td>Diode, Schottky, 30V, 0.2A, SOT-23</td>
<td>0805</td>
<td>LTST-C170UKT</td>
<td>Lite On</td>
</tr>
<tr>
<td>D9</td>
<td>1</td>
<td>0.8mm</td>
<td>Diode, LED, Red, 2.1-V, 14.2-mcd, 20ma, 0805</td>
<td>0805</td>
<td>LTST-C170UKT</td>
<td>Lite On</td>
</tr>
<tr>
<td>FID1, FID2, FID3, FID4, FID5, FID6</td>
<td>6</td>
<td></td>
<td>Fiducial mark. There is nothing to buy or mount.</td>
<td>Fiducial</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>H1, H2, H3, H4</td>
<td>4</td>
<td></td>
<td>Bumper, Hemisphere, 0.44 X 0.20, Clear</td>
<td>Transparent Bumper</td>
<td>SJ-5303 (CLEAR)</td>
<td>3M</td>
</tr>
<tr>
<td>J1</td>
<td>1</td>
<td>4x1</td>
<td>Header, TH, 100mil, 4x1, Gold plated, 230 mil above insulator</td>
<td>4x1 Header</td>
<td>TSW-104-07-G-S</td>
<td>Samtec</td>
</tr>
<tr>
<td>J2, J3, J4, J5, J6, J7, J9, J10, J15, J16, J21, J22</td>
<td>12</td>
<td></td>
<td>Header, TH, 100mil, 2x1, Gold plated, 230 mil above insulator</td>
<td>2x1 Header</td>
<td>TSW-102-07-G-S</td>
<td>Samtec</td>
</tr>
<tr>
<td>J8, J11</td>
<td>2</td>
<td>4x2</td>
<td>Header, TH, 100mil, 4x2, Gold plated, 230 mil above insulator</td>
<td>4x2 Header</td>
<td>TSW-104-07-G-D</td>
<td>Samtec</td>
</tr>
<tr>
<td>J19</td>
<td>1</td>
<td>Conn Micro High Speed Socket Strip, 0.8mm, 25x2, R/A, SMT</td>
<td>Conn Micro High Speed Socket Strip SKT 50 POS 0.8mm, RA</td>
<td>ERF8-025-01-L-D-RA-L-TR</td>
<td>Samtec, Inc.</td>
<td></td>
</tr>
<tr>
<td>J20</td>
<td>1</td>
<td>SD Memory Card Connector</td>
<td>N/A</td>
<td>502570-0893</td>
<td>Molex</td>
<td></td>
</tr>
<tr>
<td>J32</td>
<td>1</td>
<td>7.0x8.2x6.5mm</td>
<td>Terminal Block, 6A, 3.5mm Pitch, 2-Pos, TH</td>
<td>ED555/2DS</td>
<td>On-Shore Technology</td>
<td></td>
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<tr>
<td>R2, R4</td>
<td>2</td>
<td>100k</td>
<td>RES, 100k ohm, 1%, 0.1W, 0603</td>
<td>0603</td>
<td>ERJ-3EKF1003V</td>
<td>Panasonic</td>
</tr>
<tr>
<td>R3</td>
<td>1</td>
<td>0</td>
<td>RES, 0 ohm, 5%, 0.1W, 0603</td>
<td>0603</td>
<td>CRCW060300000Z0EA</td>
<td>Vishay-Dale</td>
</tr>
</tbody>
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## Table 8. Bill of Materials (continued)

<table>
<thead>
<tr>
<th>Designator</th>
<th>Quantity</th>
<th>Value</th>
<th>Description</th>
<th>Package Reference</th>
<th>PartNumber</th>
<th>Manufacturer</th>
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<tbody>
<tr>
<td>R6, R8</td>
<td>2</td>
<td>499</td>
<td>RES, 499 ohm, 0.1%, 0.063W, 0402</td>
<td>0402</td>
<td>CRCW0402499RFKED</td>
<td>Vishay-Dale</td>
</tr>
<tr>
<td>R9, R22</td>
<td>2</td>
<td>4.02k</td>
<td>RES, 4.02k ohm, 0.1%, 0.063W, 0402</td>
<td>0402</td>
<td>RT0402BRD074K02L</td>
<td>Yageo</td>
</tr>
<tr>
<td>R10, R14, R16, R86, R87, R88, R89, R90, R91, R93, R128</td>
<td>11</td>
<td>49.9</td>
<td>RES, 49.9 ohm, 1%, 0.063W, 0402</td>
<td>0402</td>
<td>CRCW040249R9FKED</td>
<td>Vishay-Dale</td>
</tr>
<tr>
<td>R5, R11, R21</td>
<td>3</td>
<td>2.00k</td>
<td>RES, 2.00k ohm, 0.1%, 0.1W, 0603</td>
<td>0603</td>
<td>RT0603BRD072KL</td>
<td>Yageo</td>
</tr>
<tr>
<td>R13, R15, R18</td>
<td>3</td>
<td>47k</td>
<td>RES, 47k ohm, 5%, 0.063W, 0402</td>
<td>0402</td>
<td>CRCW040247K0JNED</td>
<td>Vishay-Dale</td>
</tr>
<tr>
<td>R19</td>
<td>1</td>
<td>4.12k</td>
<td>RES, 4.12k ohm, 0.1%, 0.1W, 0603</td>
<td>0603</td>
<td>RT0603BRD074K12L</td>
<td>Yageo</td>
</tr>
<tr>
<td>R23, R24, R25, R26, R27, R28, R29, R30, R31, R32, R34, R35, R37, R38, R40, R41</td>
<td>16</td>
<td>0</td>
<td>RES, 0 ohm, 5%, 0.1W, 0603</td>
<td>0402</td>
<td>CRCW06030000Z0EA</td>
<td>Vishay-Dale</td>
</tr>
<tr>
<td>R33, R36, R39, R42, R43, R44, R45, R46</td>
<td>8</td>
<td>249</td>
<td>RES, 249 ohm, 0.1%, 0.1W, 0603</td>
<td>0603</td>
<td>RG1608P-2490-B-T5</td>
<td>Susumu Co Ltd</td>
</tr>
<tr>
<td>R47, R48, R92, R97, R101, R104</td>
<td>6</td>
<td>0</td>
<td>RES, 0 ohm, 5%, 0.063W, 0402</td>
<td>0402</td>
<td>RC0402JR-070RL</td>
<td>Yageo America</td>
</tr>
<tr>
<td>R79, R80, R81, R82, R83, R84, R85</td>
<td>7</td>
<td>10.0k</td>
<td>RES, 10.0k ohm, 1%, 0.063W, 0402</td>
<td>0402</td>
<td>CRCW040210K0FKED</td>
<td>Vishay-Dale</td>
</tr>
<tr>
<td>R7, R94, R95, R96, R98, R99, R100, R102, R103, R105, R107</td>
<td>10</td>
<td>NI</td>
<td>Resistor, Uninstalled</td>
<td>0402</td>
<td>NI</td>
<td>NI</td>
</tr>
<tr>
<td>SD1</td>
<td>1</td>
<td></td>
<td>SanDisk MicroSD Card, 2GB</td>
<td>N/A</td>
<td>SDSDQ-002G</td>
<td>SanDisk</td>
</tr>
<tr>
<td>SH-J2, SH-J3, SH-J4</td>
<td>3</td>
<td>1x2</td>
<td>Shunt, 100mil, Gold plated, Black</td>
<td>Shunt</td>
<td>969102-0000-DA</td>
<td>3M</td>
</tr>
<tr>
<td>U1, U4</td>
<td>2</td>
<td></td>
<td>Low-Noise, Low Quiescent Current, Precision Operational Amplifier e-trim Series, DBV0005A</td>
<td>DBV0005A</td>
<td>OPA376AIDBV</td>
<td>Texas Instruments</td>
</tr>
<tr>
<td>U2</td>
<td>1</td>
<td></td>
<td>16 bit 500KSPS 8 Channel SAR ADC</td>
<td>TSSOP-38</td>
<td>ADS86888DBT</td>
<td>TI</td>
</tr>
<tr>
<td>U3</td>
<td>1</td>
<td>OPA320AIDBVR</td>
<td>IC, Precision, 20MHz, 0.9pA, Low-Noise, HRIO, GMOS Op-Amp</td>
<td>SOT23-5</td>
<td>OPA320AIDBVR</td>
<td>TI</td>
</tr>
<tr>
<td>U5</td>
<td>1</td>
<td></td>
<td>Micro-Power (50mA), Zero-Drift, Rail-to-Rail Out Instrumentation Amplifier</td>
<td>DGK0008A</td>
<td>INA333AIDGK</td>
<td>Texas Instruments</td>
</tr>
<tr>
<td>U11</td>
<td>1</td>
<td>AT24C02B</td>
<td>IC, 2K, Serial EEPROM</td>
<td>SO-8</td>
<td>AT24C02B</td>
<td>Atmel</td>
</tr>
<tr>
<td>U13</td>
<td>1</td>
<td></td>
<td>High-Voltage Ultralow-Iq Low-Dropout Regulator, DGN0008D</td>
<td>DGN0008D</td>
<td>TPS7A6650QDGRNRQ1</td>
<td>Texas Instruments</td>
</tr>
</tbody>
</table>
Revision History

Changes from Original (May 2015) to A Revision

- Added text reference for Figure 20 ................................................................. 18
- Added footnotes to Table 4 ........................................................................... 20
- Changed figure numbers to correct ones in second paragraph of Measured Performance for Current Inputs section .... 23
- Added column headers to first column of Table 5 and Table 6 ........................................ 27
- Added text reference for Table 7 ........................................................................ 27
- Added Error Due to Tolerance of Resistors in REF / 2 Source section .................................. 29
- Added Errors Due to Tolerance of Resistors in Level Shift and ADC Driver section ........................................... 30

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