TI Designs

TI PLC Development Kit Reference Design

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Design Resources

TIDM-INDUSTRIAL-PLC	Tool Folder Containing Design Files
F28035	Product Folder
AFE031	Product Folder

TI E2E™ Community

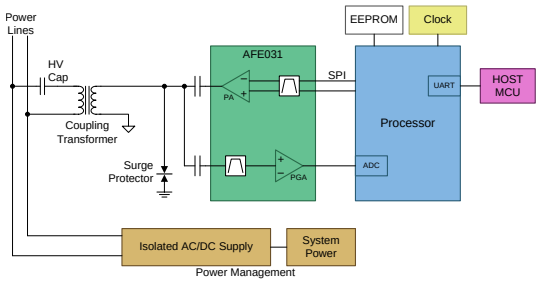
ASK Our E2E Experts
WEBENCH® Calculator Tools

Design Features

- Texas Instrument AFE031 Daughter Card
- Operating Frequency Range: Half-Band (24 kHz) in CENENLEC-A or BCD
- Data Rates up to 21.4 kbps (Half-Band FEC OFF)
- Transmission with OFDM and FEC
- Forty-Eight Data Carriers Used
- Differential Phase Modulation (DBPSK)
- ROBO Mode Provides Repetition Code
- Convolutional Encoder and Viterbi Decoder
- Bit Interleaving for Noise Effect Reduction
- CRC8 in Headers for Error Detection
- Data Randomization for Uniform Power Distribution
- Automatic Gain Control
- Supports PLC-Lite PHY, CSMA/CA MAC layer
- Serial Interface for Host Data Port: UART and HCT
- LEDs and Test Points for Firmware and Hardware Debug
- USB or JTAG for Custom Firmware Download

Featured Applications

- Solar Inverter
- Lighting Control
- Motor Control



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1 System Description

The standard PLC development kit enables easy development of software based power line communication modems. Additionally, flexible hardware modular design allows customers to use different control cards and analog front end modules.

The standard PLC development kit has F28069 control cards with PLC PRIME firmware. For PLC-Lite, users need to replace the F28069 control card with F28035 control cards, which are not included but can be purchased through TI's eStore. The control card should have an external crystal of ±25 ppm. Program the F28035 device with PLC-Lite firmware, and change the jumper settings on the PLC docking board. For detailed instructions on hardware installation, please see Section 1.4.

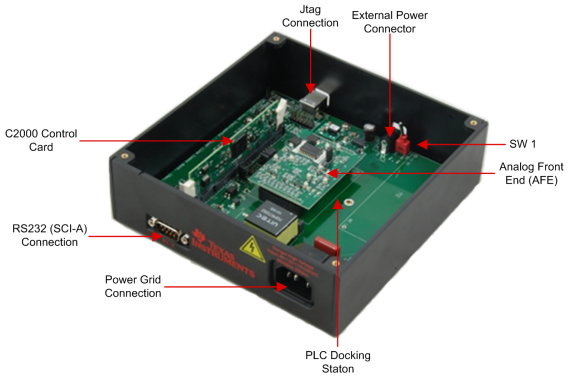

Figure 1. TI PLC Development Kit

1.1 PLC Development Kit Components

The development kit includes the following hardware:

- Two sets of development board, each set contains:
  - One F28035 MCU control card: flashed with PLC-Lite PLC image
  - One docking station
  - One AFE board

The development kit includes the following software:

- PLC-Lite binaries
  - plc_lite.out
- PLC-Lite Software Libraries
  - PLC-Lite CSL Library: csl_f2803x.lib
  - PLC-Lite AFE Library: hal_afe031_f2803x_hb.lib (half-band)
  - PLC-Lite PHY Library: phy_lin_hb.lib (half-band)
- PC Software and GUI
  - Zero configuration GUI v2.92 or up

The development kit includes the following documents:

- PLC-Lite software API specifications
  - HAL API specifications
  - PHY API specifications
  - MAC API specifications
  - UART API specifications
  - Host message protocol specifications
- PLC-Lite hardware documents
  - AFE daughter card schematics and Gerber files
  - Docking board schematics and Gerber files
  - Bill of Materials (BOM)

1.2 System Installation Requirements

To install software package to communicate with the PLC development kit, the PC must meet the following minimum requirements:

- Microsoft® Windows® XP® (SP2) or Windows 2000® (SP4)
- Intel® Pentium® IV 1-GHz processor
- 128-MB RAM (256-MB RAM recommended)
- USB 2.0 interface (if using a JTAG debug interface)
- CD-ROM drive
- Screen resolution 1024×768 or better
- 1-MB of free space on the HDD for the applications (more for LOG files)

1.3 Software Installation

To install the PLC-Lite PLC software package, run the PLC tool installer, TexasInstrumentsPLCLiteDevelopmentEvalPackageVxxxx.exe, included on the CD.

The PLC-Lite PLC software package includes the followings:

- Software documentation and API specification (PLC-Lite PHY or host message protocol) under “doc” directory
- Hardware documents (docking board and AFE daughter card) under “HW” directory
- Software binaries under “SW” directory:
  - plc_lite.out: This image is intended as a point-to-point demonstration or point-to-multipoint communication over a power line.
- Example projects under “SW” directory zip files
  - PLC-Lite PHY example project: Demonstrates the usage of PHY library API
- Tool
  - Zero configuration GUI tool installer: This feature installs PLC zero configuration GUI

1.4 Hardware Setup

The following steps show how to setup PLC-Lite hardware:

NOTE: Make sure the system is off.

1. Remove the F28069 control card from connector J1 on the docking station and replace with F28035 control card.
2. Program the F28035 control card with the binary (plc_lite.out) in the following directory after the PLC development package is installed: C:\Texas Instrument\PLCLiteDevelopmentPackageVxxx\SW\bin\.
3. Modify the jumper settings according to Table 1. For the complete description of the jumper settings, please see Section 1.4.2.

Table 1. Jumper Setting Changes for PLC-Lite

	DEFAULT	PLC-LITE	NOTE
PLC Docking Board			
J12	1-2	2-3	ADCIN0 (2-3), ADCIN1 (1-2)
J13	2-3	1-2	SPIA (1-2), McBSPB (2-3)
J14	2-3	1-2	SPIA (1-2), McBSPB (2-3)
J15	2-3	1-2	SPIA (1-2), McBSPB (2-3)
J16	2-3	1-2	SPIA (1-2), McBSPB (2-3)
J18	1-2	2-3	SPIA/McBSPB (2-3), McBSPA (1-2)
J19	1-2	2-3	SPIA/McBSPB (2-3), McBSPA (1-2)
J20	1-2	2-3	SPIA/McBSPB (2-3), McBSPA (1-2)
J21	1-2	2-3	SPIA/McBSPB (2-3), McBSPA (1-2)
F28035 Control Card			
SW1	ON	OFF	Use UART driver on RevE

4. Insert the AFE card on the docking board. Place connector J2 (AFE card) to connector J4 (docking station) and connector J3 (AFE card) to J10 (docking station).
5. Connect the 15-V-DC power supply to the 15-V power jack. Make sure the power supply for the board is switched off.
6. Connect power cables to connector TB1.
7. Connect the serial cable to the serial connector on the docking station.

NOTE: A null modem cable (transmitter and receiver cross connected) is used between a host PC UART port and the PLC kit. For dock hardware Rev-C, use the ribbon cable provided for serial connection, and for dock hardware Rev-D, use a null modem serial cable.

8. Switch on the power supply for the board.
9. Check that the LED on the F28035 control card is blinking.

1.4.1 PLC-Lite Point-to-Point Hardware Setup

PLC-Lite can be used to demonstrate point-to-point or point-to-multipoint communication over a power line. This communication combines with a zero configuration GUI to test PHY and MAC operability and send data between the two boards over the power line media. Communication requires two PCs and two null modem cables. If the host PC can use two serial ports, then a single PC can run the demo setup, using a different serial port to communicate with each board.

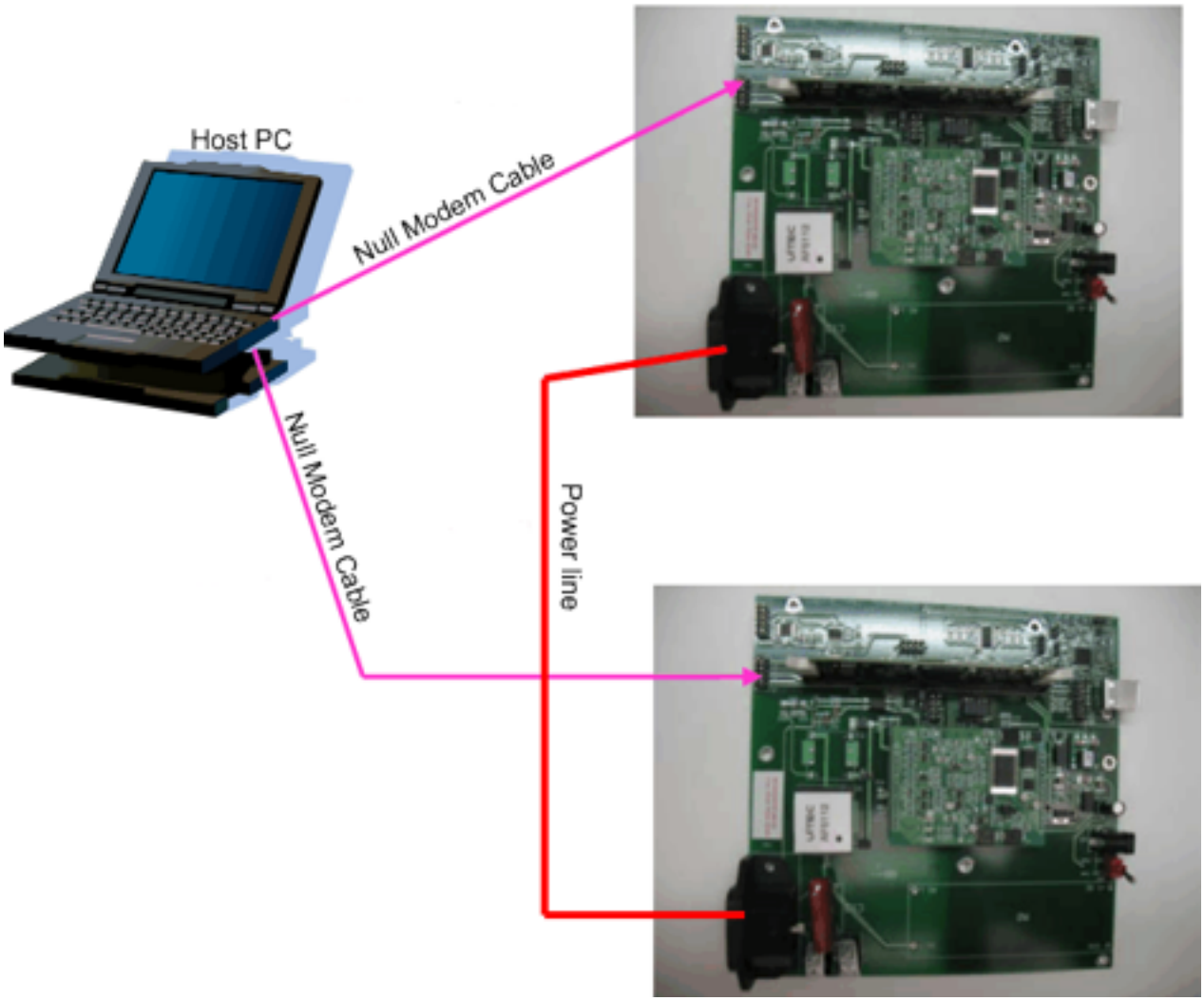

Figure 2. PLC Development Kit Point-to-Point Hardware Setup

1.4.2 PLC Development Kit Default Jumper and Connector Settings

The PLC development kit provided is configured with the default jumper and connector positions. Table 2 and Table 3 identify the jumper and connector names, descriptions, default positions, and other options if available. Users need to modify the jumper settings for PLC-Lite per Table 4.

Table 2. PLC Docking Board Jumper Settings

PLC DOCK JUMPER	DESCRIPTIONS	DEFAULT POSITION	OPTIONS	
J1	DSP control card	Connector		
J2	SCI-A	Connector		
J3	Boot options	Open	Open 1-2 2-3	Boot from Flash Boot from SPI-A Boot from SCI-A
J4	Transformer T2 selection	Close	Open Close	T2 not used T2 is used
J5	ECAP channel selection	2-3	1-2 2-3	ECAP1 ECAP3
J6	SCI-C	Connector		
J7	GPIO test pin	Open	2 4 6	GPIO1 GPIO3 GPIO4
J8	Transformer T1 selection	Open	Open Close	T1 not used T1 is used
J12	ADC channel selection	1-2	1-2 2-3	ADC channel A1 ADC channel A0
J13, J14, J15, J16	SPI or McBSP to PGA selection	1-2	1-2 3-4	SPI to AFE McBSP to AFE
J18, J19, J20, J21	McBSPA, SPI or McBSPB Selection	1-2	1-2 2-3	McBSPA SPI or McBSPB
J10, J17	AC mains	Close	Open Close	Mains not connected Mains connected
M3	AFE daughter card	Connector		
JP1	Power supply	Connector		
TB1	Power line	Connector		

Table 3. PLC USB and JTAG Macro Jumper Settings

USB/JTAG/SCI MACRO	DESCRIPTIONS	DEFAULT POSITION	OPTIONS	
J1	Boot selection	Open	Open Close	Boot from Flash Boot from SCI-A
J2	JTAG	Connector		
J3	N/A	Open		Connected to GPIO34
J4	USB or SCI-B selection	Close	Open Close	SCI-B not connected to USB SCI-B connected to USB

Table 4. PLC-Lite Settings

	DEFAULT	PLC-LITE	NOTE
PLC Docking Board			
J12	1-2	2-3	ADCIN0 (2-3), ADCIN1 (1-2)
J13	2-3	1-2	SPIA (1-2), McBSPB (2-3)
J14	2-3	1-2	SPIA (1-2), McBSPB (2-3)
J15	2-3	1-2	SPIA (1-2), McBSPB (2-3)
J16	2-3	1-2	SPIA (1-2), McBSPB (2-3)
J18	1-2	2-3	SPIA/McBSPB (2-3), McBSPA (1-2)
J19	1-2	2-3	SPIA/McBSPB (2-3), McBSPA (1-2)
J20	1-2	2-3	SPIA/McBSPB (2-3), McBSPA (1-2)
J21	1-2	2-3	SPIA/McBSPB (2-3), McBSPA (1-2)
F28035 Control Card			
SW1	ON	OFF	Use UART driver on RevE

2 Using Demo Application—Zero Configuration GUI

The zero configuration GUI is a Windows application that allows users to immediately transfer text and files, examine the current system information, display the PHY parameters, change the PHY modulation, and display the file and text transfer statistics and save log information.

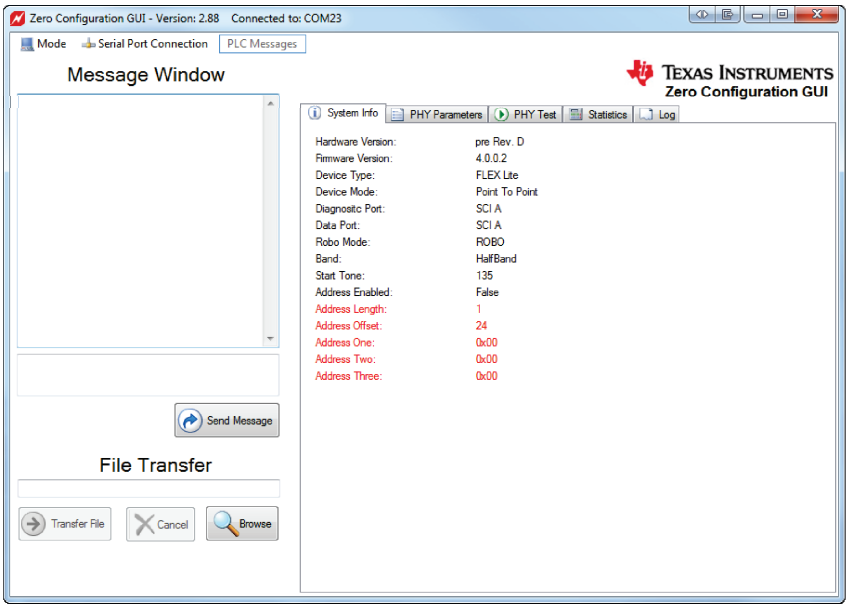

Figure 3. Zero Configuration GUI: Starting Screen

NOTE: Both transmit and receive stations should be running the zero configuration GUI and should not be paired with the PLC quality meter (PQM).

2.1 Configuration

No software or PLC configuration is needed to use the zero configuration GUI. The first available COM port on the PC, which may be a USB-to-Serial port or a standard COM port, connects to the PLC. If no available serial ports are found on the PC, the zero configuration GUI will display an error (as shown in Figure 4) and exit.

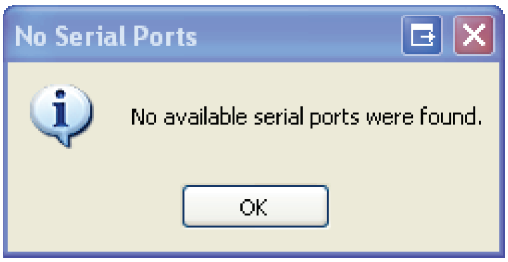

Figure 4. Message Box for No Serial Ports Found

If the COM port selected does not respond, the zero configuration GUI will display a timeout error and remain active as shown in Figure 5.

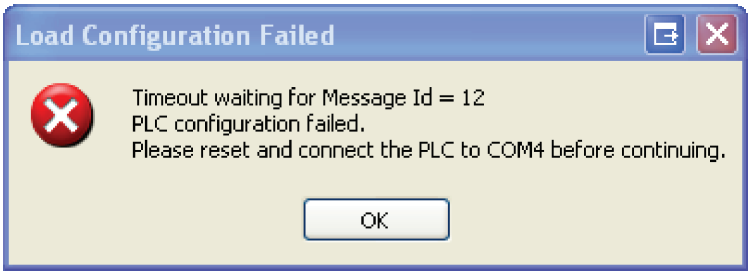

Figure 5. Message Box for Load Configuration Failed

If the PLC is connected to another COM port, the user may use the Serial Port Connection drop-down menu to connect to the desired COM port. If the PLC is not connected, connect the PLC to the desired port and try again. Once the PLC is connected to the correct COM port, reset the PLC.

2.2 Main Screen

The zero configuration GUI consists of the main screen where the user can transfer text and files. The tabs on the right display significant information about the PLC.

The COM port attached is displayed in the title bar. The first available and unopened COM port is automatically chosen. The Serial Port Connection drop-down menu may be used to change the selection to another COM port.

From this screen the user can transfer text messages and files with another PLC controlled by the zero configuration GUI.

The user may also change the mode by using the Mode drop-down menu. The three modes are zero configuration, intermediate, and expert.

- In the zero configuration mode, any available COM port 1 to 99 works with the zero configuration GUI.
- The intermediate mode GUI uses the same COM port as the zero configuration GUI. When the intermediate mode exits, the zero configuration reopens the COM port and takes control once again.
- The expert is currently disabled for this release.

2.3 Hot Keys

Several hot keys are available. The alpha key is not case sensitive.

<Ctrl + I> — Closes the GUI and executes the intermediate GUI.

<Ctrl + R> — Resets the file transfer statistics. The statistics received in the link quality report are not reset. This key stroke combination resets the statistics screen, regardless of which screen has focus in the GUI.

<Ctrl + T> — Toggles the expert mode menu items on and off, depending on their current state.

<Ctrl + S> — Sends a system information request to the PLC and updates the system info panel when the request is received.

2.4 System Info Panel

The PLC system information is displayed in the first tab. Right clicking on the System Info panel reveals a context menu with one menu item, Refresh System Information. This item will resend a system information request to the PLC and refresh the System Info panel with the updated information. Pressing Ctrl + S performs the same function without displaying the context menu.

Any value changed will be displayed in red text as shown in Figure 6.

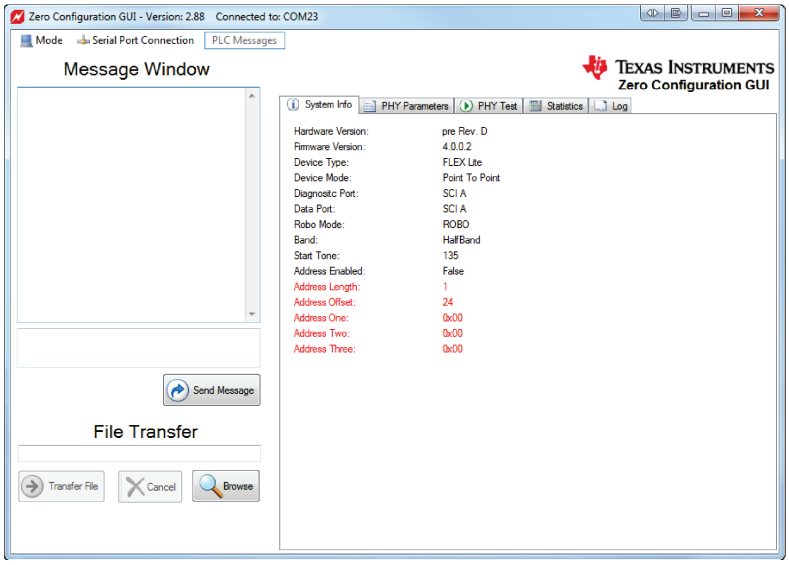

Figure 6. Zero Configuration GUI: System Info Panel

2.5 PHY Parameters Panel

The second tab displays the PHY TX (transmit) and RX (receive) parameters. The TX modulation may be changed using the radio boxes. Changing the modulation schemes affects the reliability and baud rate of the power line transmission.

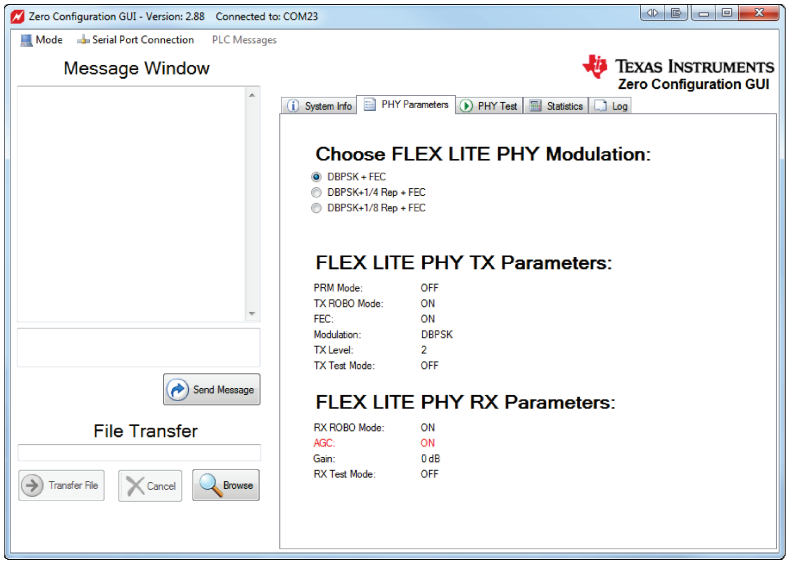

Figure 7. Zero Configuration GUI: PHY Parameters Panel

2.6 Statistics Panel

The Statistic panel displays information concerning the text and file transfers. Items that have changed are displayed in red. Right clicking on the Statistics panel reveals a context menu with one menu item, Reset Application Totals. This item resets totals. Pressing Ctrl + R performs the same function without displaying the context menu.

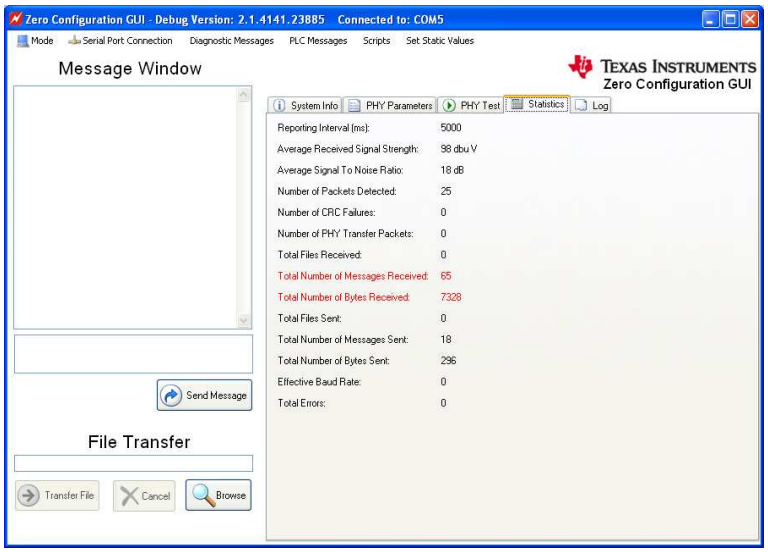

Figure 8. Zero Configuration GUI: Statistics Panel

2.7 PHY Test Panel

The PHY Test panel tests communications between two PLCs using PHY packets. One PLC transmits the PHY packets while the other receives the PHY packets. To start the test, click on the Start Flex Lite PHY Transmit button on either PLC. The statistics will disappear from the panel since there are no statistics collected on the transmitting PLC. See the example in Figure 9.

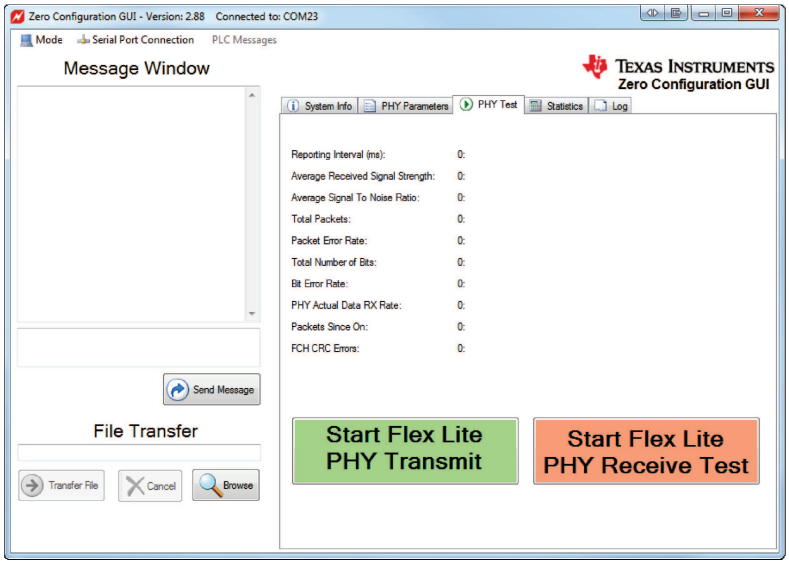

Figure 9. Zero Configuration GUI: PHY Test Panel

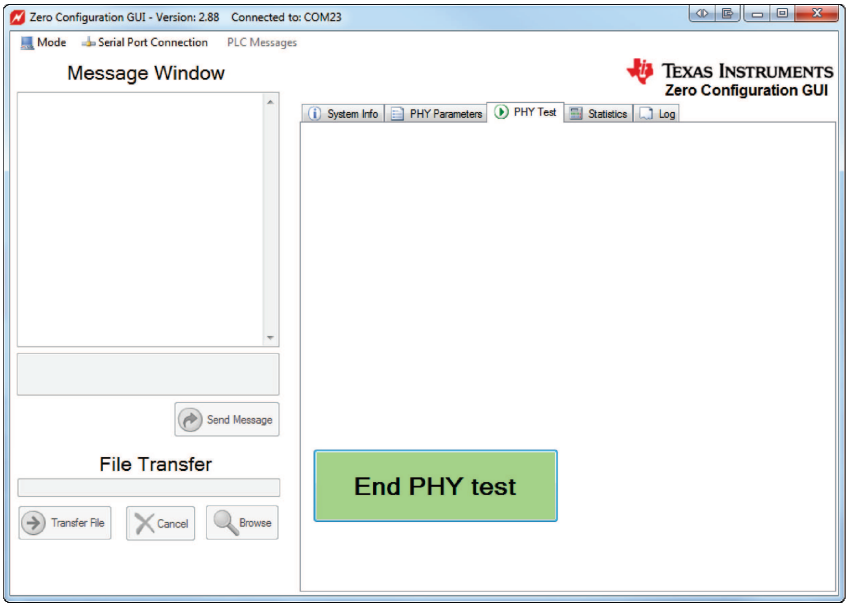

Figure 10. Zero Configuration GUI: PHY TX Transmitting

NOTE: Text and file transfers will not work during PHY testing.

On the receiving PLC, click the Start Flex Lite PHY Receive Test button. This button changes to End PHY test, and the statistics will start updating. See the example in Figure 11.

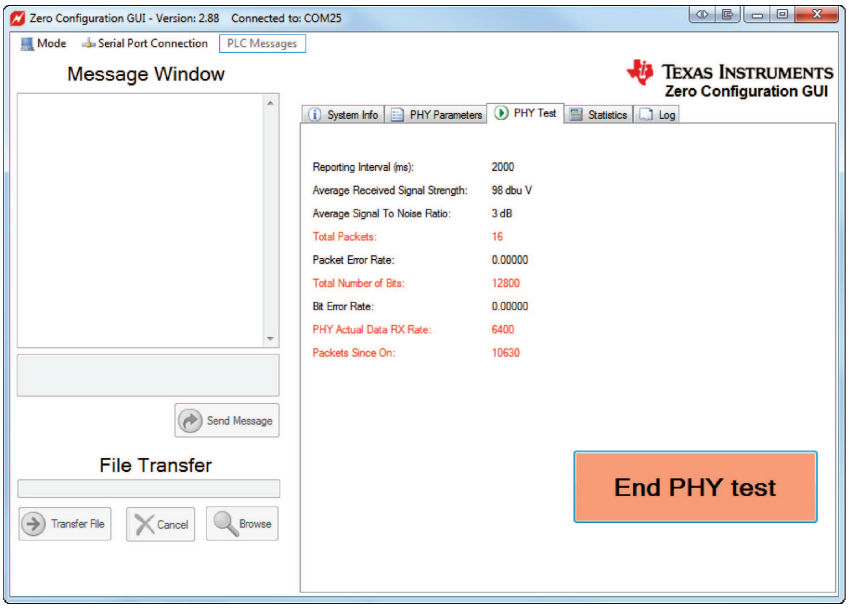

Figure 11. Zero Configuration GUI: PHY RX Receiving

To end the test, click the End PHY test button on both PLCs.

2.8 Log Panel

The Log panel holds about 100,000 characters and then refreshes the display. This action prevents the panel from consuming large amounts of memory and keeps the Log panel responsive to new input.

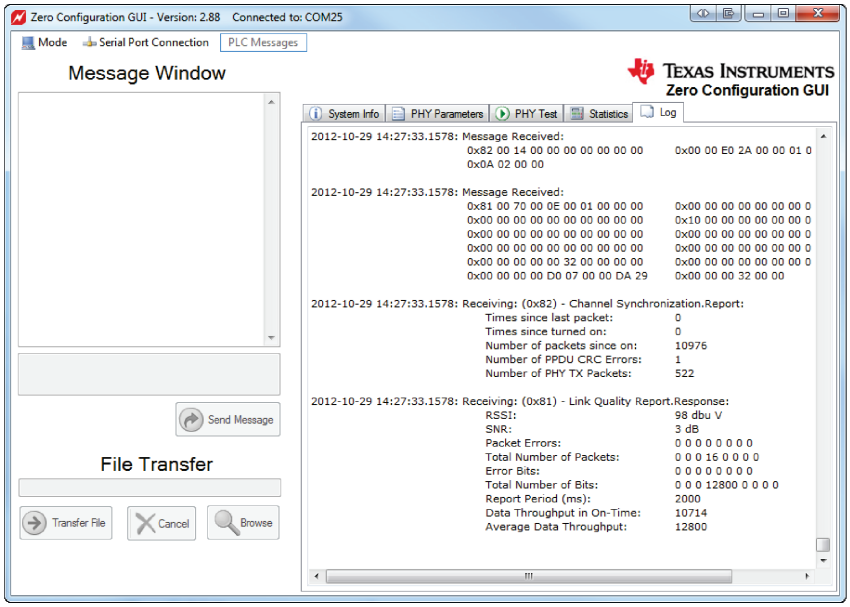

Figure 12. Zero Configuration GUI: Log Panel

The Log panel by default displays very little information, but right clicking on the panel displays the Log panel context menu. Use this menu to display the formatted messages sent and received by the zero configuration GUI. The following is the list of features exposed by the Log panel context menu:

Enable Message Data Display — This feature enables the Log panel to display the message transfers, both sending and receiving. Depending on the other options selected, the raw data, formatted data, or both will be displayed. This option is off by default.

Enable Logging to a File — When selected, this feature prompts the user for a file to save the logged information. When enabled, all data messages sent and received are saved and written to the log.

Log Full Message Data — This feature displays the formatted message data in the Log panel. No data is displayed unless the Enable Message Data Display is enabled.

Log Condensed Data — This feature only displays the message type and no actual message data. This action reduces the amount of data logged to the screen.

Log Raw Message Data — This feature displays the unformatted message data as a byte stream.

Clear Display — This feature clears the Log panel. This action does not affect data being logged to a file.

Save to File — This feature saves the current contents of the log panel to a file of the user's choosing.

2.9 Sending Text Messages

To transfer text between two connected PLC devices using the zero configuration GUI, type text in the small text box and click on the Send Message button. Pressing Enter while entering the text adds a line. The key will not send the text message.

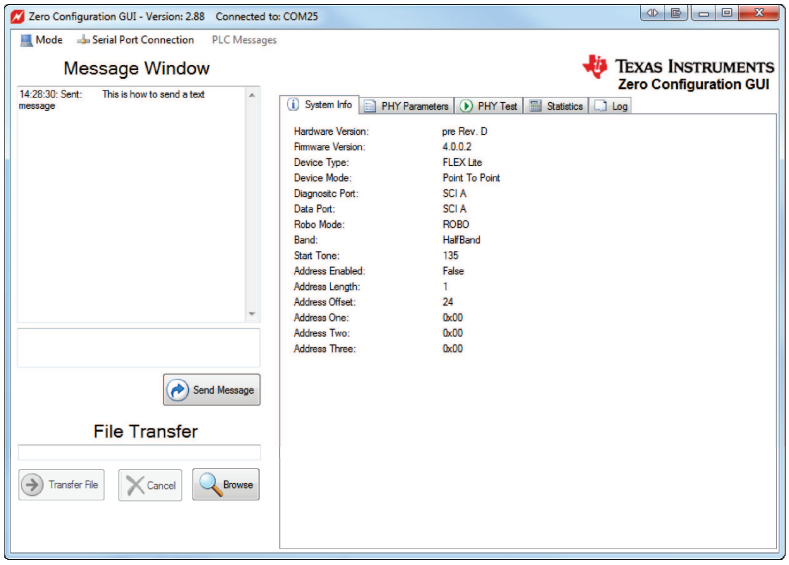

Figure 13. Zero Configuration GUI: Send Text Message

When the text is sent, the text is moved to the top text box and displayed by the receiving PLC.

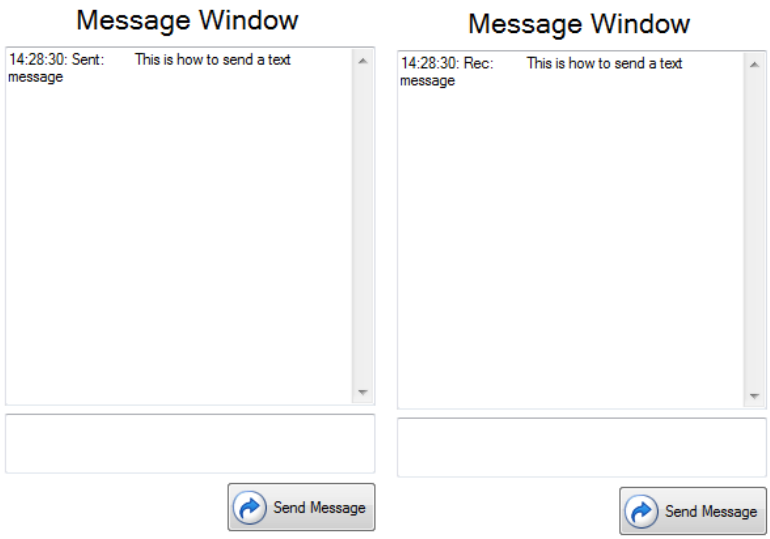

Figure 14. Zero Configuration GUI: Message Window

The form on the left in Figure 14 is the sender and the form on the right is the receiver. The user may send text from either PLC device.

If the text transfer fails, the message box below will be displayed as shown in Figure 15.

Figure 15. Message Box for Failed Text Message

2.10 File Transfers

The File Transfer function is contained in the bottom left-hand corner. Click on the Browse button to choose the file to transfer. Only one file at a time may be chosen for the file transfer.

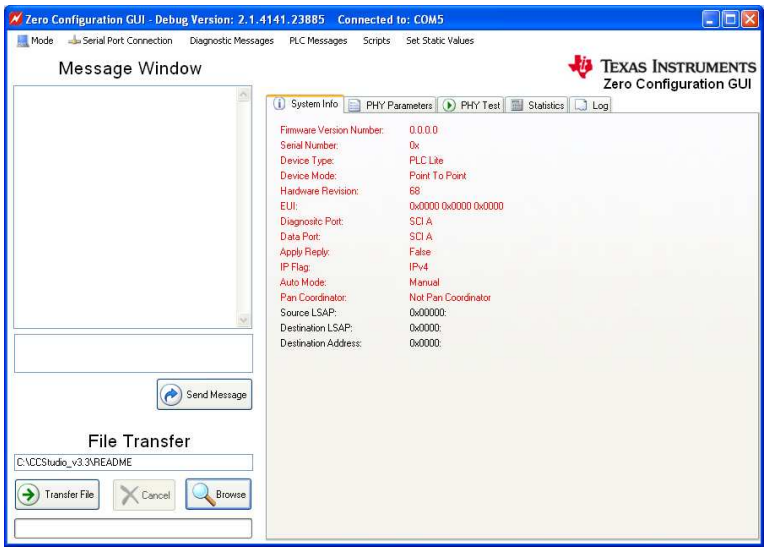

Figure 16. Zero Configuration GUI: File Transfer Window

NOTE: The file location for transmit and receive should be different when a single PC is used. The total length of the file name and path should not exceed 80 characters.

After the file is chosen, click on the Transfer File button. The zero configuration GUI must control the other PLC.

When the transfer starts, the GUI displays a progress bar on both zero configuration GUIs. The GUI in Figure 17 is the receiving zero configuration GUI and displays the path and file name where the received file is being copied. The user is not allowed to change the directory path of the received file.

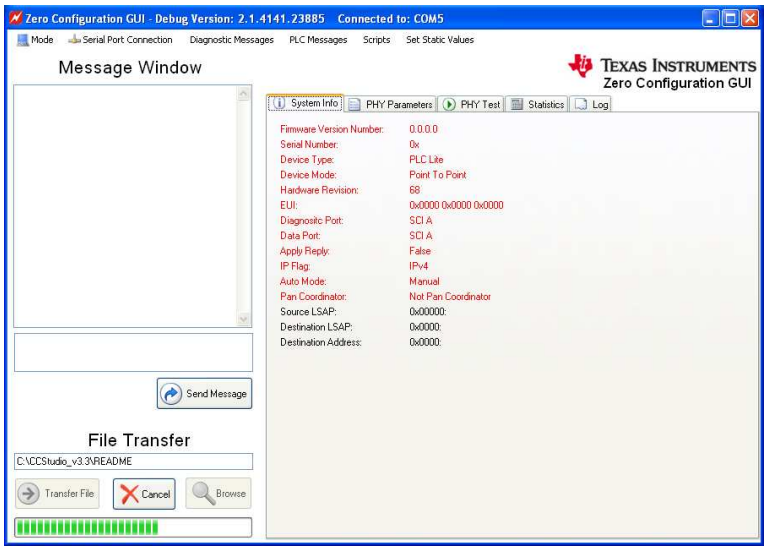

Figure 17. Zero Configuration GUI: File Transferring

When the file transfer is complete, both zero configuration GUIs display the message box shown in Figure 18.

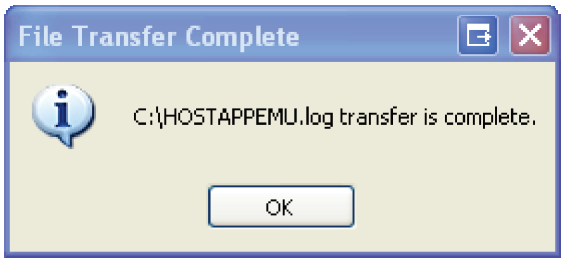

Figure 18. Message Box for File Transfer Complete

If the file transfer fails, the sending GUI displays the message box as shown in Figure 19.

Figure 19. Message Box for Unable to Transfer Files

The user can cancel the file transfer by clicking the Cancel button on either GUI.

3 Using the Intermediate GUI

The intermediate mode is chosen from the Mode drop-down menu.

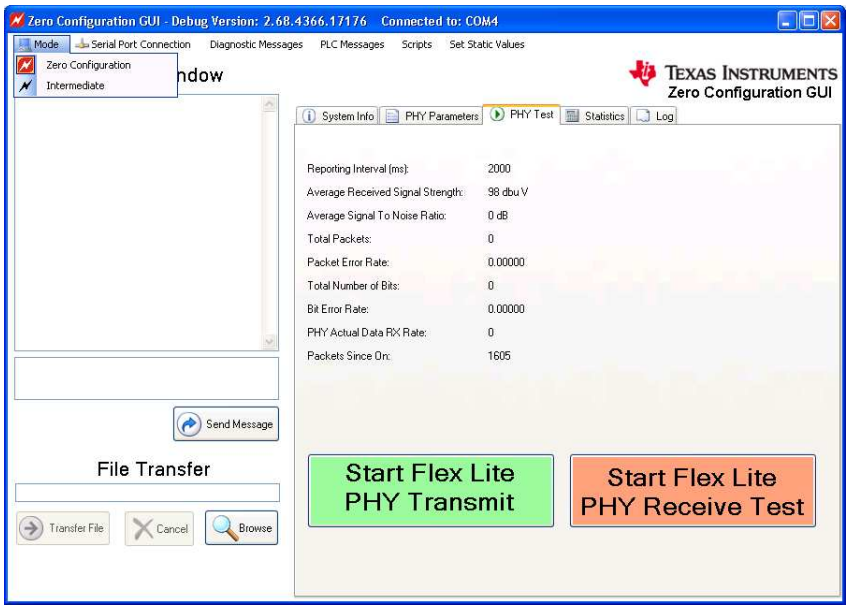

Figure 20. Choosing the Intermediate GUI

3.1 User Interface

The intermediate GUI consists of the following:

- Main menu: All operations are initiated from the main menu with toolbars and buttons.
- Graphical displays of PHY parameters: PHY parameters configuration (see Figure 21).
  - RSSI graph: Plot is in dBuV, limited between 70 and 98 dBuV.
  - SNR graph: Plot is in dB.
  - Bit error rate graph: Plots of PHY layer bit error rate, one line for each MCS (only applicable to PHY test mode operation).
  - Packet error rate graph: Plots of PHY layer packet error rate, one line for each MCS
- PHY statistics: This panel provides statistics in the physical link.
- Transfer statistics: This panel provides statistics when a file transfer is in operation.
- System information: This panel provides system version information and PHY or MAC configurations.

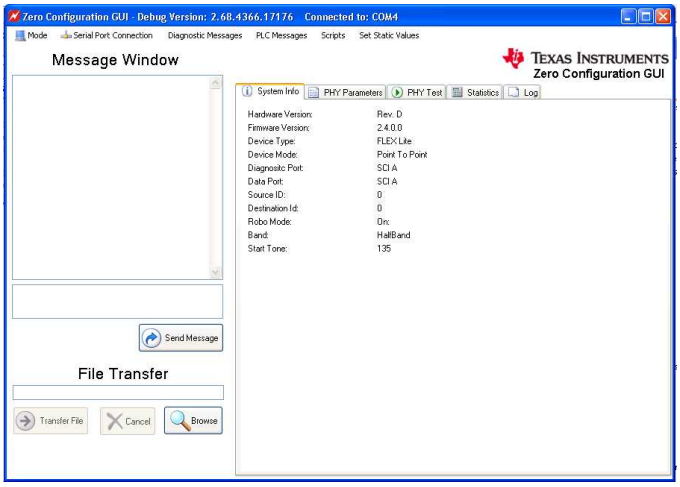

Figure 21. Intermediate GUI: User Interface

3.2 System Configuration

The system configuration provides a way to configure the PLC-Lite device (Menu → Options → Set System Config).

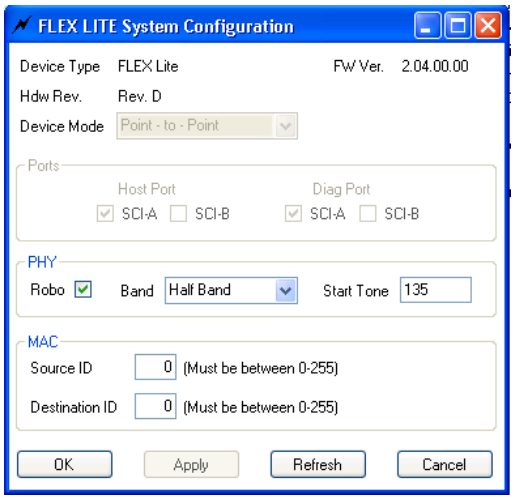

Figure 22. Intermediate GUI: System Configuration

The following describes the configuration settings:

- PHY settings
  - ROBO: Set the PHY mode (ROBO or Non-ROBO)
  - Band: Set the band to Cenelec-A/B/C/D half-band
  - Start tone: Set the start tone index. The start frequency is calculated as (start tone index)*500kHz/1024. Examples include:
    - Cenelec-A upper half band (65.9-89.3kHz): (start tone index)=135
    - Cenelec-BC half-band (99.1-122.6kHz): (start tone index)=203
- MAC settings
  - Source ID: MAC ID of the source device
  - Destination ID: MAC ID of the destination device

3.3 Getting System Information

The Get System Info option (Menu → Options → Get System Info) retrieves the current system information values from the PLC. These values are represented in the system information view. These values may be set using the Set System Config option (Menu → Options → Set System Config).

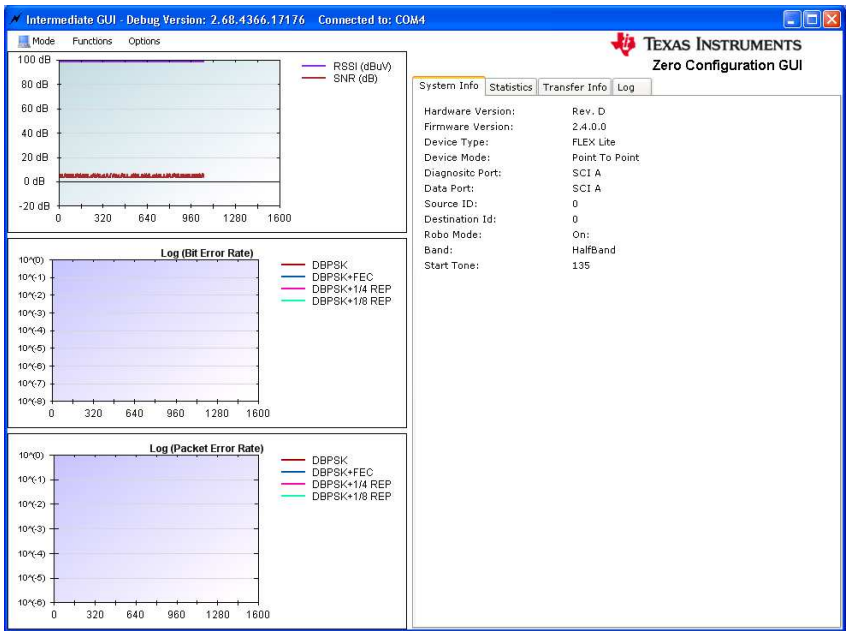

Figure 23. Intermediate GUI: System Information

3.4 Control Set Up

The Control Setup option (Menu → Options → Control Setup) allows the following:

- Channel status update: Select the Enable Synchronization Parameter check box for a status display in the statistic window.
- Link quality report update: Select the Enable Link Quality Report check box for RSSI/SNR/BER/PER to display in the statistics window.
- Period between statistics update: Enter the duration (in seconds) in Report Output Period.

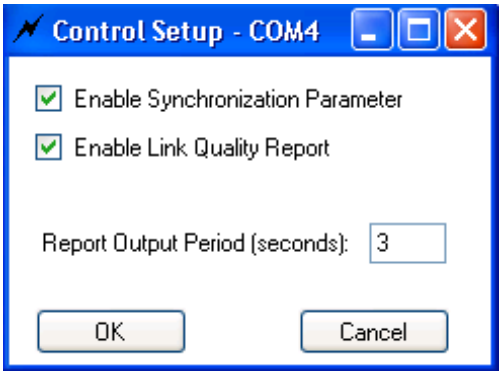

Figure 24. Intermediate GUI: Control Setup

3.5 Configuring PHY Parameters

The PHY Parameters configuration (Menu → Options → PHY Parameters) is used for configuring the PHY TX and RX parameters.

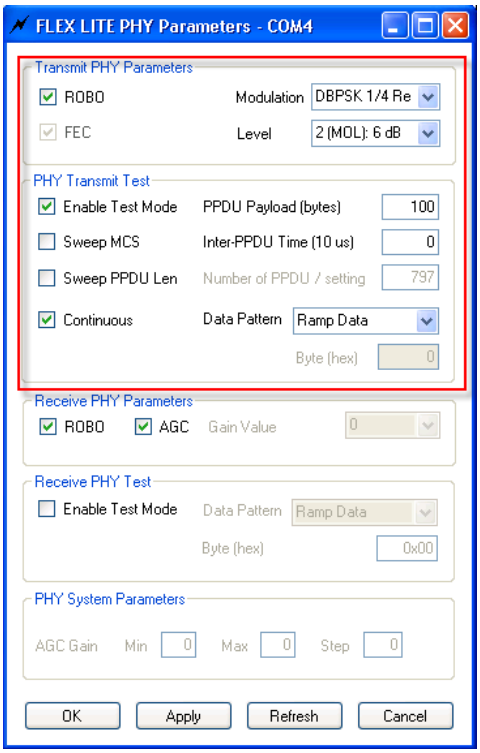

Figure 25. Intermediate GUI: PHY TX Parameters

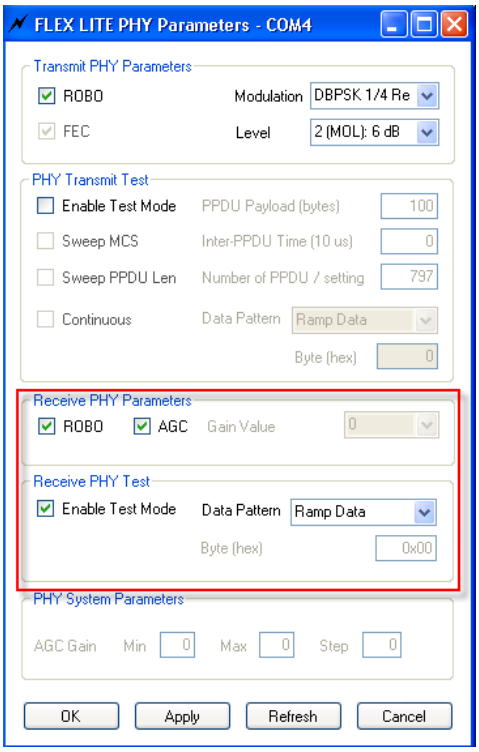

Figure 26. Intermediate GUI: PHY RX Parameters

The following describes the PHY TX parameters that can be configured:

- ROBO: PHY robust mode
- Modulation: DBPSK. If ROBO mode is selected, then DBPSK + 1/4 repetition or DBPS + 1/8 repetition can be selected.
- FEC: ON or OFF. If ROBO mode is selected, this field is not valid since FEC is always on.
- Level: Transmit Level
  - 0: Maximum output level (MOL)
  - 1: MOL – 3 dB
  - 2: MOL – 6 dB
  - 3: MOL – 9 dB
  - 4: MOL – 12 dB
  - 5: MOL – 15 dB
  - 6: MOL – 18 dB
  - 7: MOL – 21 dB

The following describes the PHY TX parameters that can be configured for PHY TX test mode only:

- Test mode: When enabled, this mode configures the transmitter in test mode and transmits a fixed data pattern (selected in the data pattern box) for BER testing.
- Sweep PPDU length: When enabled, the test will sweep through all valid PPDU length in increasing order for the modulation used.
- Continuous: When enabled, the test will continuously transmit PPDUs as specified. When disabled, the test will transmit the “number of PPDUs per setting” as specified and stop.
- Data pattern: When PHY test mode is enabled, the data pattern for the packet payload to be transmitted can be selected. The following data patterns are available:
  - A ramp data pattern from 0 to 255
  - A fixed data byte set by octet value. The data pattern is repeated for the duration of the payload
- PPDU length: PPDU length in bytes. The current firmware version supports a PPDU length of 1 to 100 bytes.

NOTE: This field will be ignored when sweep PPDU length is selected.

- Inter-PPDU time: The gap time between PPDU is in units of 10 microseconds.
- Number of PPDUs per setting: The number of PPDU per setting during a PPDU length sweep.

The following describes the PHY RX parameters that can be configured:

- Automatic gain control (AGC): If selected, the receiver performs AGC. If unselected, manual gain setting is used. Valid gain values are from 0 to 7 with step of 6 dB.

The following describes the PHY RX parameters that can be configured in PHY RX test mode only:

- Test mode: When enabled, the receiver compares to the receive packet using the data pattern selected and computes BER for BER testing.
- Data pattern: When test mode is enabled, this parameter can select the data pattern used for comparison in computing BER. A ramp data pattern from 0 to 255 or a fixed data byte set by octet value.

NOTE: This pattern should be identical to the selection in the transmitter for valid BER result.

The following describes the PHY system parameters:

- AGC gain min: Minimum AGC gain in dB
- AGC gain max: Maximum AGC gain in dB
- AGC gain step: Step size of AGC in dB

3.6 Testing PHY Performance

The PHY performance can be tested in a point-to-point configuration where the system configuration steps described in Section 2.6 should be used. One modem must be configured as a transmitter in test mode and the other modem as a receiver in test mode (Menu → Options → PHY Parameters). The hardware should be set up as described in Section 1.4. Figure 27 shows an example of PHY test with DBPSK+FEC, transmitting at a level of 6 dB, PPDU length of 100 bytes, and an inter-PPDU interval of 0 ms in continuous mode.

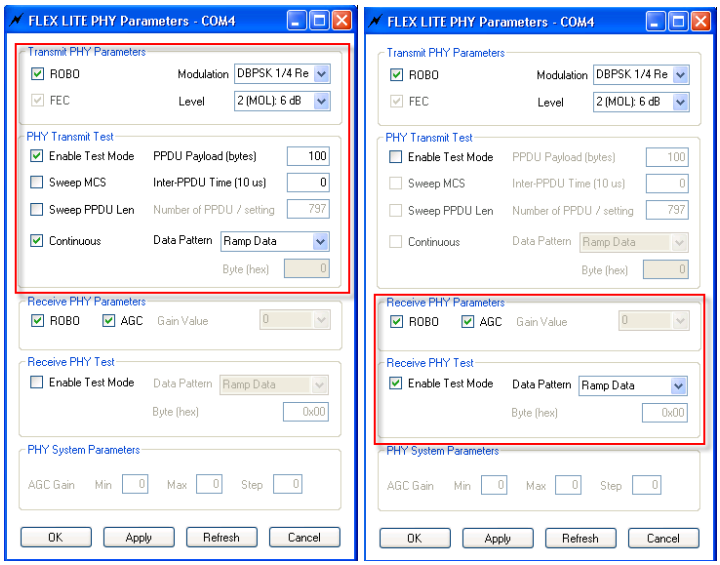

Figure 27. Intermediate GUI: PHY TX and RX Test Mode Setup

NOTE: This example does not support concurrent bi-directional data transfer.

By enabling the channel status and link quality report and setting report period (as described in Section 2.5), the PHY performance (SNR/RSSI/PER/BER) will be displayed in the graphs and the statistics will be displayed in the statistics panel.

3.7 Sending and Receiving Message

The Send Message function (Menu → Function→ Send Message) sends a small text message from one device to another in point-to-point configuration. The function is intended to test and verify communication between the two systems in a point-to-point configuration. To specify an ID for both TX and RX stations, if the user is using more than one kit to establish a network, select Set System Config in the Options menu. If the user is only using one kit for point-to-point test, ignore this step.

For the RX station, Source ID is the RX ID, Destination ID is the TX ID. For the TX station, Source ID is the TX ID, Destination ID is the RX ID. For more information, refer to Section 3.2.

When this option is selected, the user may fill in a message and press send, and the other host will display the message (see Figure 28).

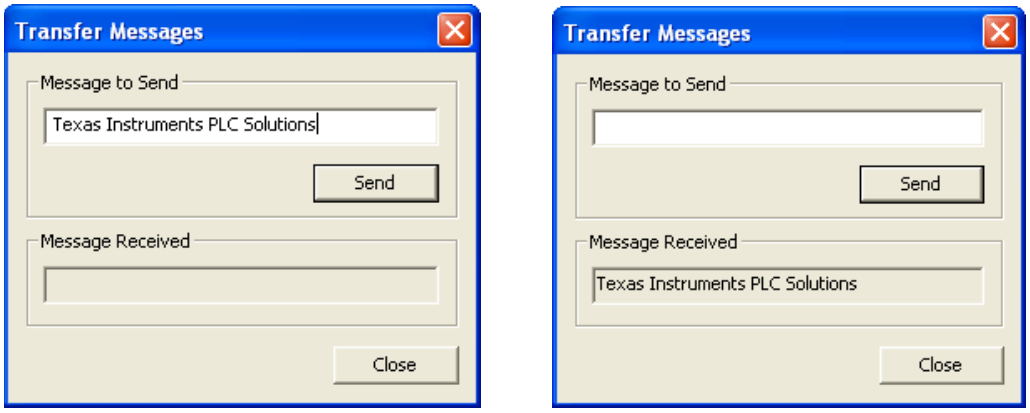

Figure 28. Intermediate GUI: Message Sending

3.8 Sending and Receiving Files

The Send File function (Menu → Function → Send File) sends a file from one device to another in a point-to-point configuration. This function is not a guaranteed error-free delivery (the file received may have dropped packets) and is a means to push data from one board to another. The receiver will note both the payload CRC and missing packet errors and will attempt to notify the sender of these errors.

To specify an ID for both TX and RX stations, if the user is using more than one kit to establish a network, select Set System Config in the Options menu. If the user is only using one kit for point-to-point test, ignore this step.

For the RX station, Source ID is the RX ID, Destination ID is the TX ID. For the TX station, Source ID is the TX ID, Destination ID is the RX ID. For more information, see Section 3.2.

Once the file transfer begins, a file transfer status window is displayed (Figure 29), and the Transfer Information section reflects transfer statistics (Figure 30).

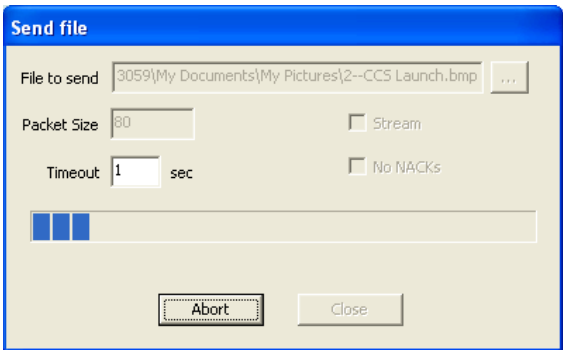

Figure 29. Intermediate GUI: File Transferring

Figure 30. Intermediate GUI: File Transferring Statistics

Statistics may be cleared by selecting File/New or by pressing the New File button. Either the sender or receiver can abort the transfer. The sender may abort by pressing the Abort button, and the receiver may abort by selecting the menu option Functions/Abort File Receive.

4 System Troubleshoot

4.1 Troubleshoot for GUI Tool-to-Device Communications

- To check that the GUI tool is communicating to the device, check that the tool can read system information following the steps in Section 2.4.
- If a USB serial converter is being used, check that the correct COM port has been selected. The COM port may not be enumerated to the same port number when the port is unplugged and then re-plugged or a new USB port is being used.
- If the GUI tool has previously been communicating to the device and the tool was kept opened while the device has been reset or power cycled, close and re-open the GUI.

Appendix A PLC-Lite Hardware Resource Usage

Table 5. PLC-Lite GPIO Pins Configurations

GPIO PIN	CONNECTED TO	PLC-LITE BUILD USAGE
GPIO00		
GPIO01	TP	
GPIO02		
GPIO03	TP	
GPIO04	TP	
GPIO05		
GPIO06	AFE	
GPIO07	AFE	AFE031 DAC
GPIO08	AFE	
GPIO09		
GPIO10		
GPIO11		
GPIO12	AFE	AFE031 SD
GPIO13		
GPIO14		
GPIO15		
GPIO16	SPI (SPISIMOA)	AFE031
GPIO17	SPI (SPISOMIA)	AFE031
GPIO18	SPI (SPICLK)	AFE031
GPIO19	SPI (SPISTEA)	AFE031
GPIO20		
GPIO21		
GPIO22		
GPIO23		
GPIO24		
GPIO25		
GPIO26		
GPIO27		
GPIO28	SCI (SCIRXDA)	UART host port
GPIO29	SCI (SCITXDA)	UART host port
GPIO30		
GPIO31	LED2	System heart beat
GPIO32	(I2C) SDAA	
GPIO33	(I2C) SCLA	
GPIO34	LED1	Blink during TX and RX

Table 6. PLC-Lite Peripherals and Interrupts Use

PERIPHERALS	PLC-LITE BUILD USAGE	INTERRUPT
32-Bit CPU Timers		
Timer 0	TX delay	PIE1.7
Timer 1	Absolute timer (PLC-Lite PHY time stamp)	
Timer 2	Statistics report	
Watchdog Timer (Unused)		
ADC		
ADCINA0	RX ADC samples	PIE1.1
ADCINA2	Reserved	
ADCINA4	Reserved	
SCI		
SCIA	Host port	PIE9.1—RX PIE9.2—TX
SPI		
SPIA	AFE031	
I2C	Interface to EEPROM	
EPWM		
EPWM1	ADC trigger	PIE3.7
EPWM2	ADC trigger	
EPWM6	CSMA timer	
EPWM7	TX samples	
EQEP1	PHY TX task	PIE5.1
LVF	PHY RX task	PIE12.7

Table 7. PLC-Lite Flash Configurations and Use

SECTORS	SIZE (WORDS)	PLC-LITE BUILD USAGE
ABC	24 K	PLC-Lite code: 20.6-K words
D	8 K	0
E	8 K	0
F	8 K	0
G	8 K	0
H	8 K	PHY algorithm code: 600 words

Table 8. PLC-Lite System Memory and MIPS Use

MEM/MIPS	BENCHMARK
Flash	21.2-K words
RAM	8.7-K words
MIPS	Average: 45 MIPS Peak: 58 MIPS

Appendix B PHY Example Project

The PHY example project demonstrates the use of PHY library APIs when hardware is setup with two devices connected via power line. One device sends one packet, waits for one receive packet, and then transmits another packet. This process alternates between TX and RX. The packet size is 40 bytes with a repeating ramp data pattern using the following:

- ROBO mode: Non-ROBO
- Modulation: DBPSK with FEC enabled
- Transmit level: 3

NOTE: The user must have Code Studio Composer (CCS) 5.5 installed in order to compile the project.

Follow these steps to complete the PHY example project:

1. Unzip ti_PLC-Lite_phy_example.zip.
2. In CCS, import PHY test project test_tx_rx from the following directory: \dsp_28x\plc_lite\src\phy\test\test_tx_rx_swi\.
3. Skip this step if the user doesn't want to re-build the project and re-use the binary file from the delivered package. In CCS, select the Debug_AFE031_HB configuration, and build the project. The build should produce the following binary file:
   - \dsp_28x\plc_lite\src\phy\test\ test_tx_rx_swi\Debug_AFE031_HB\phy_tx_rx.out
4. In CCS, select the target configuration and connect target.
5. In CCS, load test_tx_rx.out.
6. In CCS, run the target to execute the code and LED flashes. The user may also disconnect the debugger and power cycle the board to execute the code.
7. Load the same code to the second board.
8. Connect the two boards via power line cables. After the code in the second board start to execute, both boards should alternate between RX and TX and the LEDs should blink.

B.1 Source File Description

- Test Bench
  - Project file: located in \dsp_28x\plc_lite\src\phy\test\ test_tx_rx_swi\
  - Test bench: test_tx_rx.c demonstrates alternating PLC-Lite PHY TX and PHY RX using provided PHY library
  - Linker command: 28035_FLASH_lnk.cmd
  - Test example for flash
- Header Files
  - PHY common: phy.h
  - PHY TX: phy_tx.h
  - PHY RX: phy_rx.h
  - HAL: hal_afe.h
  - Chip support library header files
- Libraries
  - PHY lib: phy_lin_hb.lib
  - HAL lib: hal_afe031_f2803x_hb.lib
  - Chip support lib: csl_f2803x.lib

B.2 PHY Library Demonstration

The example of a PHY library project demonstrates packet transmission and reception at the physical layer in a TDD fashion.

1. Flash two F28035 boards with PHY library example executable.
2. Connect via power line.
3. Sequence of operation:
   - Board A sends a packet.
   - Board B receives packet and sends a packet back to Board A.
     - These steps will repeat.
   - LEDs on the DSP control card will blink if the packet continues to transmit and receive.

B.3 Hardware Resource Usage

The PHY library uses the following hardware resources:

- ADC
  - ADCINA0: PLC Receive
- CPU timers
  - CPU Timer 0: PHY timer
  - CPU Timer 1: PLC-Lite PHY system timer, 20 bits in 10-us increments
  - CPU Timer 2: Statistics report timer
- CPU Timers
  - EPWM1: ADC trigger
  - EPWM2: ADC trigger
  - EPWM6 Timer: CSMA/CA timer
  - EPWM7 Timer: PHY TX sampling (2 us)
- GPIO Peripherals
  - GPIO 7: AFE DAC select
  - GPIO 12: AFE SD
  - GPIO 16: SPISIMOA
  - GPIO 17: SPISOMIA
  - GPIO 18: SPICLKA
  - GPIO 19: SPISTEA
  - GPIO 28: SCIRXDA
  - GPIO 28: SCITXDA

B.4 PHY Library Test Bench Steps

1. Initialize hardware (using F28035 specifics).
2. Configure flash.
3. Install ISR:
   - Timer 0 (HAL_afe_cpuTimer0_isr)
   - EPWM7 Timer (HAL_afe_pwm7Timer_isr)
   - ADCINT1 (HAL_afe_adc_isr)
   - PHY TX task and PHY RX task (PLC_LITE_tx_swi, PLC_LITE_rx_swi)
4. Initialize AFE:
   - HAL_afeInit
5. Initialize PHY library:
   - PHY_txInit
   - PHY_rxInit
6. Generate packet to transmit.
7. Start PHY RX to listen to line.
   - PHY_rxStart (0xFFFF, cb_ppdu)

NOTE:
- Call back for PHY_rxStart - cb_ppdu.
- If status succeeds, do some processing if needed and release a buffer back to PHY:
  - PHY_rxPpduRelease
  - LED toggle
  - rxppdu_done = 1

8. Start the first packet transmission

NOTE:
- Call back for PHY_txPpdu - cb_tx.
- If status succeeds, do some processing if needed:
  - LED toggle

9. Enable system interrupt.
10. Repeat the main loop.

B.5 ISR Description

- CPU Timer 0 ISR
- EPWM7 Timer ISR
  - Interrupts every 2 us
  - Every interrupt transmits one sample
  - Once the symbol is finished, set txSymbDone
  - Once the symbol is finished, trigger tx_swi.
- ADC Channel ISR
  - Interrupts every 8 us
  - Every interrupt processes four samples
  - Once the symbol is finished, set afeReadyFlag
  - Once the symbol is finished, trigger rx_swi.

B.6 SWI Descriptions

- PLC_LITE_tx_swi: Start TX state machine run

```
interrupt void PLC_LITE_tx_swi()
{
txSymbDone = 0;
PHY_txSmRun();
}
```

- PLC_LITE_rx_swi: Start RX state machine run

```
{
afeReadyFlag = 0;
PHY_rxSmRun();
}
```

B.7 Main Loop

When the RX package is finished, start another packet transmission.

```
While(1)
{
if (rxppdu_done == 1)
{
rxppdu_done = 0;
PHY_txPpdu(&PHY_tx_ppdu_s, cb_tx);
}
}
```

Appendix C User Application Integration Guide

The following serves as a guideline when integrating with user applications:

- Carefully arrange user-peripheral and hardware resources to avoid any conflict with PLC-Lite. The PLC-Lite PHY resource usage is listed in Appendix A.
- Follow the PHY example project in Appendix B to see the initialization sequence and PLC-Lite PHY, HAL, and CSL library API usages.
- PLC-Lite PHY sampling rates:
  - TX: 500 kHz, through EPWM7 timer.
  - RX: 500 kHz, through EPWM1 and EPWM2 triggered ADCIN0.
- The following are critical interrupts for the PLC-Lite PHY to operate properly:
  - TX sampling interrupt: PIE group 3 (PIE3.7) occurs every 2 us, and each interrupt takes 40 to 50 cycles or approximately 29 MIPS;
  - RX sampling interrupt: PIE group 1 (PIE1.1) occurs every 8 us, and each interrupt takes 110 to 160 cycles or approximately 17 MIPS;
  - TX symbol interrupt: PIE group 5 (PIE5.1) occurs every 2.048 to 2.24 ms, and each interrupt takes approximately 64000 cycles or 28 MIPS;
  - RX symbol interrupt: PIE group 12 (PIE12.7) occurs every 2.048-2.24ms, and each interrupt takes approximately 78000 cycles or 35 MIPS.
- (Optional) If UART is enabled: PIE group 9 (PIE9.1, PIE9.2).
- When the user application uses interrupts:
  - User interrupts should use PIE groups with a lower priority than the PLC-Lite PHY sampling interrupts.
  - If the user's interrupt timings are critical, those interrupts should have a higher priority than the PLC-Lite PHY symbol interrupts.
  - Always enable nested interrupts in user ISR by adding “EINT” at the beginning of the user ISR.
- All of the previous interrupt configurations are open to users in the HAL library. Should the user need to re-configure interrupts, their priorities should be in the following order:
  1. RX sampling interrupts
  2. TX sampling interrupts
  3. User interrupts
  4. TX symbol interrupts
  5. RX symbol interrupts

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