**TI Designs**

**Data Concentrator Cape for BeagleBone Black**

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**Design Resources**

- **TIDA-00225**
  - Tool Folder Containing Design Files
- **TIDM-SOMPLC-F28M35**
  - Product Folder
- **CC2543EM**
  - Product Folder
- **TRS3386ECPWR**
  - Product Folder
- **TPS61093DSK**
  - Product Folder
- **SN74LV125APWR**
  - Product Folder
- **SN74LVC1G57DBVR**
  - Product Folder

**Design Features**

- Interface to BeagleBone Black
- Interface to PLC SOM for FCC, ARIB/Prime, or CENLEC Frequency Band
- Interface for CC2543, CC2544, or CC2545 RF SOCs
- Compatible with CC112x SOM Modules
- RS232 DTE Interface
- On-Board DC-DC Power Supply for PLC 15 V
- 3-Phase Power Input and Zero Cross Detectors

**Featured Applications**

- Power Line Communication Modem for Electric Power Utilities to Transfer Vital Information for the Operation and Protection of the Electric Power Grid
- Industrial Automation/AMR (Smart E-Meter: AMR and AMI): The PLC Communication Networks can be Used to Give Electric Energy Related Services, such as Meter Reading, Demand Management, and Remote Billing
- Reading of Flow Meters using RF
- Solar Power Inverters and Micro Inverters
- Remote Data Collection Using Modems

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1 System Description

1.1 Advanced Metering Infrastructure (AMI)

Advanced Metering Infrastructure (AMI) is one of the major applications for data concentrators.

Advanced Metering Infrastructure is a communications service that permits the transfer of data from utility meters to a utility company’s metering collection system. AMI automates the previously manual process of reading meters. Also, AMI allows the collection of much more and different types of information to benefit the utility and customer alike.

Lowered costs can increase the resources available for product development and other needs. Further detailed data provides better insight into an increasingly complex power market, as well as an opportunity to differentiate service via various options. These options include on-line daily usage information, outage status, and customer outage notification.
AMI Communications Technologies

AMI technology decisions are dominated by the choice of a communications scheme. Cost is part of the communications scheme choice.

The following are the choices for an AMI communications scheme:

- Power line communications (PLC) technology uses power lines as media for sending and receiving low-bandwidth data at very low speed. This option tends to be cost effective for meters served by a single substation. In the US, this technology has been widely adopted by rural cooperatives.

- Telephone-based technology uses telephone lines (either dedicated or shared with voice communications) to send and receive meter data. With dial outbound systems, the utility must know the customer’s phone number to get the data, which can cause administrative problems. This factor, along with the relatively high prices charged by phone companies for this type of service, has made this option less attractive. With dial-inbound systems, by contrast, meters are equipped with an automated dialer that can call the utility at pre-assigned times, when an alarm condition is detected, or when signaled by the utility.

- Telephone-based systems tend to be cost effective for selected meters that are sparsely spread throughout a service territory, and are typically used for large commercial and industrial customers.

- Wireless radio-frequency (RF) AMI technologies rely on the use of a transmitter on the meter to communicate with a receiver that can be handheld, located in a vehicle, or installed at a fixed location. Wireless approaches tend to be more cost-effective for meters within a clustered geographic area. Mobile radio systems that use handheld or van-based receivers cannot provide two-way real-time communications, and are best suited as replacements for manual meter reading, especially where the cost of manual reading is high. Fixed-network wireless systems, by contrast, can support a wide variety of applications, including metering, real-time pricing, energy management, and outage or theft detection. Of course, there is additional cost for these extended features.

The Data Concentrator Cape (called DC-Cape in this document) for BeagleBone Black can interface with multiple nodes (electricity meter, water meter, and so forth) via power line communication (PLC), low-power RF, or serially using RS-232.

Data Terminal Equipment (DTE) is typically either a dumb terminal or the serial port on a computer or workstation. Data Communications Equipment (DCE) is typically a modem, Data Service Unit (DSU), Channel Service Unit (CSU), or other piece of data communications equipment.
2 Design Features

Table 1. Design Features

<table>
<thead>
<tr>
<th>Feature</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Processor (CPU) interface</td>
<td>2 x 46-Pin expansion header for interfacing to BeagleBone Black</td>
</tr>
<tr>
<td>Power line interface (PLC)</td>
<td>34-Pin interface for PLC SOM modules</td>
</tr>
<tr>
<td>AC mains input</td>
<td>3-Phase inputs with Zero Cross</td>
</tr>
<tr>
<td>Low power RF</td>
<td>Header 10 x 2, x 2 to mount RF SOC</td>
</tr>
<tr>
<td>RS232 serial interface</td>
<td>RS232 level shifter for modem interface</td>
</tr>
<tr>
<td>Onboard power supply</td>
<td>Onboard DC-DC converters for powering PLC</td>
</tr>
</tbody>
</table>

3 Block Diagram

![Block Diagram Image]

- UART TRS3386ECPWR
- D89
- PLC SOM Interface
- Zero Cross SN74LVC1G57
- PLC_TX
- Coupling Transformers
- 3 Phase AC Input
- SN74LV125APWR LEDs
- TPS61093
- RF SOM2 CC2543EM
- 5 V
- 15 V
4 **Highlighted Products**

For more information on each of the devices in Section 4, see the respective product folders at [www.ti.com](http://www.ti.com). See also the links for Product Folders in Design Resources.

4.1 **BeagleBone Black**

The BeagleBone Black is the newest member of the BeagleBoard family. BeagleBone Black is a lower-cost, high-expansion focused BeagleBoard. BeagleBone Black uses a low cost Sitara AM3359AZCZ100 Cortex A8 ARM processor from Texas Instruments.

4.2 **PLC SOM Interface**

The DC-Cape supports power line communication over a three-phase power system. All three phases are capacitively coupled and routed to the PLC SOM connector for transmit and receive. The PLC SOM acts as a transceiver (PHY) for all PLC operations.

The processor communicates with the PLC via UART. Two GPIO pins on the processor are used to control the reset (PLC_RESET) and enable (PLC_EN) signals on the PLC SOM. Each phase can be configured for CENELEC and FCC band operation or fully disconnected through a series of jumpers. The board includes a zero-crossing detection circuit for each phase. The output of each zero-crossing circuit is routed to the PLC SOM connector.

4.3 **Low Power RF Interface**

The DC-Cape includes an RF daughter cards interface. The daughter card interface consists of a pair of 20-pin connectors. The CC2543EM (evaluation module) contains the RF IC and necessary external components and matching filters for getting the most out of the radio.

4.4 **Serial Communication - RS232 Interface**

The DC-Cape provides an RS232 interface for modem or GSM communication. The same UART can also be used for PLC characterization.

4.5 **Power Supply and EEPROM**

A DC-DC converter TPS61093 is used to generate the required power supplies for PLC operation. The board contains a serial EEPROM with the board specific data which allows the processor to automatically detect which board is connected and the version of the board that is connected. Other hardware specific data can be stored in this memory as well. An I2C EEPROM is provided to detect the version of the BeagleBone Black Cape board.
## 5 Circuit Design and Component Selection

### 5.1 BeagleBone Black Features

#### Table 2. BeagleBone Black Features

<table>
<thead>
<tr>
<th>FEATURE</th>
<th>DETAILS</th>
</tr>
</thead>
</table>
| Processor | Sitara AN3357BZCZ100  
1 GHz, 2000 MIPS |
| Graphics Engine | SGX530 3D, 20 M Polygons/S |
| SDRAM Memory | 512 MB DDR3L 800 MHz |
| Onboard Flash | 2 GB, 8-Bit Embedded MMC |
| PMIC | TPS65217C PMIC Regulator and One Additional LDO |
| Debug Support | Optional Onboard 20-Pin CTI/JTAG, Serial Header |
| Power Source | MiniUSB, USB, or DC Jack  
5-V DC External via Expansion Header |
| PCB | 3.4" x 2.1"  
6 Layers |
| Indicators | 1-Power, 2-Ethernet, 4-User Controllable LEDs |
| HS USB 2.0 Client Port | Access to USB0, Client Mode via MiniUSB |
| HS USB 2.0 Host Port | Access to USB1, Type A Socket, 500-mA LS/FS/HS |
| Serial Port | UART0 Access via 6-Pin 3.3-V TTL Header. Header is Populated |
| Ethernet | 10/100, RJ45 |
| SD/MMC Connector | MicroSD, 3.3 V |
| User Input | Reset Button  
Boot Button  
Power Button |
| Video Output | 16 B HDMI, 1280 x 1024 (MAX)  
1024 x 768, 1280 x 720, 1440 x 900, 1920 x 1080 at 24 Hz  
w/EDID Support |
| Audio | Via HDMI Interface, Stereo |
| Expansion Connectors | Power 5 V, 3.3 V, VDD_ADC (1.8 V)  
3.3 V I/O on All Signals  
McASP0, SPI1, I2C, GPIO (69 MAX), LCD, GPMC, MMC1, MMC2, 7 AIN (1.8 V MAX), 4 Timers, 4 Serial Ports, CAN0,  
EHRPWM (0,2), XDMA Interrupt, Power Button, Expansion Board ID  
(Up to 4 Can Be Stacked) |

(1) See Reference #1.
Two 23 x 2 connectors are used to interface the DC-cape to the BeagleBone Black board. Figure 1 shows the interface connector. The signals not used by DC-Cape are shown as X (not connected on the DC-Cape).

Figure 1. BeagleBone Black Interface Connector on DC-Cape
5.2 PLC SOM Interface

5.2.1 Zero-Crossing Detection

The board includes a zero-crossing detection circuit for each phase. The output of each zero-crossing circuit is routed to the PLC SOM connector. Zero-crossing detectors can be used to synchronize communications signals to the AC line or sources of noise. Typically, in single-phase applications, only a single zero-crossing detector is used. In three-phase applications, two or three zero-crossing detectors can be used.

NOTE: A single phase zero cross output is shown in Figure 2. In the DC-Cape, there are three zero cross detectors for three phases.

Figure 2. PLC SOM Interface Zero-Crossing Detection
5.2.2  AC Power Input

Line coupling circuitry to connect to mains power to the PLC is shown in Figure 3.

Figure 3. PLC SOM Interface AC Power Input
This design supports single-phase and three-phase power-line communication. To use power-line communication, connect each phase input and neutral to the power-line communication system as shown in Table 3. The earth ground input is not connected to any components on the board and can be left unconnected.

**CAUTION**

⚠️ Do not leave the board powered when unattended.

**CAUTION**

⚠️ Electric shock possible when connecting board to live wire. Board should be handled with care by a professional. For safety, use of isolated test equipment with overvoltage and overcurrent protection is highly recommended.

<table>
<thead>
<tr>
<th>INPUT</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>Phase-A and AC power Input</td>
</tr>
<tr>
<td>B</td>
<td>Phase-B</td>
</tr>
<tr>
<td>C</td>
<td>Phase-C</td>
</tr>
<tr>
<td>N</td>
<td>Neutral</td>
</tr>
<tr>
<td>E</td>
<td>Earth ground</td>
</tr>
</tbody>
</table>

Table 3 shows the characteristics of a PLC transformer 750510476 designed for PLC modems using TI Analog Front-End PLC. For more details, refer to PLC Transformer for Texas Instruments AFE030 / AFE031 / AFE032

Table 4 shows the characteristics of a PLC transformer 750510476 designed for PLC modems using TI Analog Front-End PLC. For more details, refer to PLC Transformer for Texas Instruments AFE030 / AFE031 / AFE032

<table>
<thead>
<tr>
<th>CHARACTERISTIC</th>
<th>VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Isolation voltage</td>
<td>5000-V AC at 1 second</td>
</tr>
<tr>
<td>Operating temperature</td>
<td>-40°C to 125°C</td>
</tr>
<tr>
<td>Standards</td>
<td>Conforms to IEC60950-1, EN60950-1, UL60950-1/CSA60950-1, AS.NZS60950.1</td>
</tr>
<tr>
<td>RoHS</td>
<td>Lead free</td>
</tr>
<tr>
<td>Insulation</td>
<td>Reinforced</td>
</tr>
</tbody>
</table>

**5.2.3 System-on-Module Interface**

The SOMPLC-F28M35 is a single-board system-on-module (SOM) for PLC in the ARIB frequency band. This single hardware design SOMPLC-F28M35 supports several popular PLC industry standards including G3 and IEEE-1901.2. TI's certified PLC software is available along with the SOMPLC-F28M35. Engineers can integrate the SOM design into their overall system board. Alternatively, engineers can keep the SOM design as an add-on board to their application. The only additional hardware required is the AC mains line coupling circuitry.

This reference design includes hardware schematics and Gerber files to simplify the task for engineers to add PLC to their end systems. OEMs benefit by having the ability to rapidly evaluate and prototype Power Line Communications technology in their application.
SOMPLC-F28M35 Features

- Support for ARIB frequency band
- Supports G3 and IEEE-1901.2 PLC industry standards
- Comprehensive two-chip solution with MCU and AFE032-integrated analog front-end
- 34-pin mini header provides flexibility for interfacing to custom board and other TI Designs like the PLC Data Concentrator and TMDSPLCKIT-V4

Figure 4 shows the SOMPLC-F28M35 interface.
Table 5 shows the SOM connector pinouts.

Table 5. PLC SOM Connector Pinout

<table>
<thead>
<tr>
<th>PIN #</th>
<th>SIGNAL</th>
<th>PIN #</th>
<th>SIGNAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>AC GND</td>
<td>2</td>
<td>PLC Signal</td>
</tr>
<tr>
<td>3</td>
<td>NC</td>
<td>4</td>
<td>NC</td>
</tr>
<tr>
<td>5</td>
<td>Digital GND</td>
<td>6</td>
<td>Digital GND</td>
</tr>
<tr>
<td>7</td>
<td>15-V DC</td>
<td>8</td>
<td>3.3-V DC</td>
</tr>
<tr>
<td>9</td>
<td>PLC_EN [GPIO2[0]]</td>
<td>10</td>
<td>ZERO_PLC_A</td>
</tr>
<tr>
<td>11</td>
<td>UART3_TXD</td>
<td>12</td>
<td>UART3_RXD</td>
</tr>
<tr>
<td>13</td>
<td>Pull-down</td>
<td>14</td>
<td>Pull-down</td>
</tr>
<tr>
<td>15</td>
<td>NC</td>
<td>16</td>
<td>NC</td>
</tr>
<tr>
<td>17</td>
<td>NC</td>
<td>18</td>
<td>Digital GND</td>
</tr>
<tr>
<td>19</td>
<td>ZERO_PLC_C</td>
<td>20</td>
<td>Digital GND</td>
</tr>
<tr>
<td>21</td>
<td>NC</td>
<td>22</td>
<td>Digital GND</td>
</tr>
<tr>
<td>23</td>
<td>PLC_LED2</td>
<td>24</td>
<td>PLC_LED1</td>
</tr>
<tr>
<td>25</td>
<td>NC</td>
<td>26</td>
<td>NC</td>
</tr>
<tr>
<td>27</td>
<td>NC</td>
<td>28</td>
<td>NC</td>
</tr>
<tr>
<td>29</td>
<td>PLC_RESET [GPIO2[1]]</td>
<td>30</td>
<td>ZERO_PLC_B</td>
</tr>
<tr>
<td>31</td>
<td>NC</td>
<td>32</td>
<td>NC</td>
</tr>
<tr>
<td>33</td>
<td>PLC_SCIB_RXD</td>
<td>34</td>
<td>PLC_SCIB_TXD</td>
</tr>
</tbody>
</table>

(1) See Reference #2.

5.3 Low Power RF Interface

Different frequency bands can be considered:

- 2.4 GHz ISM band
- Sub 1GHz ISM bands - 902-928

SOMs for evaluating different frequency bands are available from TI.
5.3.1 SOM - Interface Connector

The DC-Cape includes the RF daughter card interface CC1. The daughter card interface consists of a pair of 20-pin connectors. The daughter card interface CC1 uses the connector pair P5 and P6.

Table 6 gives the full pin out of each pair of RF interface connectors.

Table 6. CC1 (P5 and P6) Pinout

<table>
<thead>
<tr>
<th>PIN #</th>
<th>SIGNAL NAME</th>
<th>PIN #</th>
<th>SIGNAL NAME</th>
<th>PIN #</th>
<th>SIGNAL NAME</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>GND</td>
<td>2</td>
<td>NC</td>
<td>1</td>
<td>NC</td>
</tr>
<tr>
<td>3</td>
<td>VREGGEN2 (GPIO1[15])</td>
<td>4</td>
<td>NC</td>
<td>3</td>
<td>NC</td>
</tr>
<tr>
<td>5</td>
<td>RESET (GPIO0[13])</td>
<td>6</td>
<td>UART2 TX¹</td>
<td>5</td>
<td>NC</td>
</tr>
<tr>
<td>7</td>
<td>UART2 TX¹</td>
<td>8</td>
<td>UART2 RX¹</td>
<td>7</td>
<td>3.3-V</td>
</tr>
<tr>
<td>9</td>
<td>UART2 RX¹</td>
<td>10</td>
<td>GPIO1[12]</td>
<td>9</td>
<td>3.3-V</td>
</tr>
<tr>
<td>11</td>
<td>NC</td>
<td>12</td>
<td>GPIO1[15]</td>
<td>11</td>
<td>NC</td>
</tr>
<tr>
<td>13</td>
<td>NC</td>
<td>14</td>
<td>SPI1_CS0N³</td>
<td>13</td>
<td>NC</td>
</tr>
<tr>
<td>15</td>
<td>NC</td>
<td>16</td>
<td>SPI1_CLK²</td>
<td>15</td>
<td>RESET (GPIO0[13])</td>
</tr>
<tr>
<td>17</td>
<td>NC</td>
<td>18</td>
<td>SPI1_D0 (SIMO)²</td>
<td>17</td>
<td>NC</td>
</tr>
<tr>
<td>19</td>
<td>GND</td>
<td>20</td>
<td>SPI1_D1 (SOMI)²</td>
<td>19</td>
<td>GPIO1[14]</td>
</tr>
</tbody>
</table>

¹ GPIO0[13]
² SIMO
³ SOMI
Figure 5 shows the schematic for the interface connector on DC-Cape.

Figure 5. RF Interface Connector on DC-Cape
5.4 Serial Communication - RS232 DTE Interface

TRS3386ECPWR is the RS232 transceiver used on the DC-Cape board. The TRS3386ECPWR DB-9 male connector brings out UART pins for expansion purposes. Table 7 gives the pin outs of the TRS3386ECPWR connector and Figure 6 shows the schematics.

Table 7. P9 DB9 Connector

<table>
<thead>
<tr>
<th>PIN #</th>
<th>SIGNAL NAME</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>RSA_RXD</td>
</tr>
<tr>
<td>3</td>
<td>RSA_TXD</td>
</tr>
<tr>
<td>8</td>
<td>RSA_CTS</td>
</tr>
<tr>
<td>7</td>
<td>RSA_RTS</td>
</tr>
<tr>
<td>5</td>
<td>GND</td>
</tr>
</tbody>
</table>

Figure 6. RS232 Interface
5.5 Power Supply and EEPROM

TPS61093 is a 1.2-MHz, fixed-frequency boost converter designed for high integration and high reliability. The IC integrates a 20-V power switch, an input/output isolation switch, and a power diode. When the output current exceeds the overload limit, the IC’s isolation switch opens up to disconnect the output from the input. The isolation switch protects the IC and input supply. The isolation switch also disconnects the output from the input during shutdown to minimize leakage current.

Figure 7 shows the Power Supply and EEPROM.

The DC-DC converter converts 5 V to 15 V, which is required for PLC operation.

The board contains a serial EEPROM with the board-specific data, which allows the processor to automatically detect which board is connected and the version of that board. Other hardware specific data can be stored in the EEPROM memory as well. The part number of the EEPROM memory device used is CAT24C256W.
6 Software Description

6.1 U-Boot

The U-boot on AM335x uses a two-stage approach. The size of the internal RAM in AM335X is 128 KB. Of the 128 KB, 18 KB at the end is used by the ROM code. Also, 1 KB at the start (0x402f0000 - 0x402f0400) is secure, and cannot be accessed. The reserved RAM places a limit of 109 KB on the size of the U-Boot binary which the ROM code can transfer to the internal RAM and use as an initial stack before initialization of DRAM.

Since it is not possible to squeeze in all the functionality that is normally expected from a U-Boot in less than 110KB (after setting aside some space for stack, heap, and so forth), a two-stage approach has been adopted. The first stage initializes only the required boot devices (NAND, MMC, I2C, and so forth). The second full stage installs all other devices (ethernet, timers, clocks, and so forth).

NOTE: In the rest of this document when referring to the binaries, the binary for the first stage is referred to as SPL and the binary for the second stage is called U-Boot.

6.1.1 Building U-Boot

6.1.1.1 Prerequisite

Verify that SDK 6.00 is installed on the host computer. GNU toolchain for the ARM processor from Arago is recommended to build U-Boot. Arago toolchain can be found in the linux-devkit directory of the SDK. If not already done, add this compiler to the path by executing the following code.

$ export PATH="$<SDK install dir>/linux-devkit/sysroots/i686-arago-linux/usr/bin : $PATH"

Change to the base of the U-Boot directory.

$ cd ./ti-sdk-am335x-evm-MM.mm.pp.bb/board-support/u-boot-MM.mm.pp.bb

6.1.1.2 U-Boot Patch

The U-boot patch can be found on the SD card in the START_HERE/Software/patches folder. Locate the U-Boot patch and apply the patch to the U-Boot source.

$ patch -p1 < 0001-Baseline-u-boot-patch-for-EVM-SDC.patch

6.1.1.3 Compile

Below are instructions on how to generate binaries for the memory or peripheral devices. Building into a separate object directory with the "O=" parameter is strongly recommended.

6.1.1.3.1 UART

Execute the following code.

$ [ -d ./am335x ] && rm -rf ./am335x
$ make O=am335x CROSS_COMPILE=arm-linux-gnueabihf- ARCH=arm am335x_evm

In the am335x directory, SPL is spl/u-boot-spl.bin and U-Boot is u-boot.img.

6.1.1.3.2 NAND

Execute the following code.

$ [ -d ./am335x ] && rm -rf ./am335x
$ make O=am335x CROSS_COMPILE=arm-linux-gnueabihf- ARCH=arm am335x_evm

In the am335x directory, SPL is MLO and U-Boot is u-boot.img.
6.1.3.3 SPI

Execute the following code.

```bash
$ [ -d ./am335x ] && rm -rf ./am335x
$ make O=am335x CROSS_COMPILE=arm-linux-gnueabihf- ARCH=arm am335x_evm_spiboot
```

In the am335x directory, SPL is MLO.byteswap and U-Boot is u-boot.img.

6.2 Kernel

This section will cover the basic steps for building the Linux kernel and drive modules.

6.2.1 Building Linux Kernel

6.2.1.1 Prerequisite

Verify that SDK 6.00 is installed on the host computer. GNU toolchain for the ARM processor from Arago is recommended to build the kernel. Arago toolchain can be found in the linux-devkit directory of the SDK. If not already done, add this compiler to the path by executing the following code.

```bash
$ export PATH="<sdk install dir>>/linux-devkit/sysroots/i686-arago-linux/usr/bin/:$PATH"
```

Change to the base of the Kernel directory.

```bash
$ cd ./ti-sdk-am335x-evm-MM.mm.pp.bb/board-support/linux-MM.mm.pp.bb
```

6.2.1.2 Kernel Patch

The kernel patch can be found on the SD card in the START_HERE/Software/patches folder. Locate the kernel patch and apply the patch to the kernel source.

```bash
$ patch -p1 < 0001-Baseline-kernel-patch-for-EVM-SDC.patch
```

6.2.1.3 Cleaning the Kernel Sources

Prior to compiling the Linux kernel, it is often a good idea to make sure that the kernel sources are clean and that there are no remnants left over from a previous build.

**NOTE:** The next step will delete any saved .config file in the kernel tree as well as the generated object files. If a previous configuration has already been created, save a copy of the configuration file before proceeding in order to prevent the loss of the configuration file.

Clean the kernel.

```bash
$ make ARCH=arm CROSS_COMPILE=arm-linux-gnueabihf- mrproper
```

6.2.1.4 Configure the Kernel

Before compiling the Linux kernel, it needs to be configured to select what components will become part of the kernel image, which components will be built as dynamic modules, and which components will be left out all together.

Set using the default configuration.

```bash
$ make ARCH=arm CROSS_COMPILE=arm-linux-gnueabihf- tisdk_am335x-evm_defconfig
```

To customize the kernel configuration if desired, run the following command.

```bash
$ make ARCH=arm CROSS_COMPILE=arm-linux-gnueabihf- menuconfig
```
6.2.1.5 **Compile**

Once the kernel has been configured, it must be compiled to generate the bootable kernel image, as well as any dynamic kernel modules that were selected.

Build the kernel image. The resulting kernel image file will be located in the arch/arm/boot directory called uImage.

```
$ make ARCH=arm CROSS_COMPILE=arm-linux-gnueabihf- uImage
```

Build the dynamic modules. This will result in .ko (kernel object) files being placed in the kernel tree. These .ko files are the dynamic kernel modules.

```
$ make ARCH=arm CROSS_COMPILE=arm-linux-gnueabihf- modules
```

6.3 **Flashing Images**

6.3.1 **Boot Modes**

There are four boot modes supported.

6.3.1.1 **eMMC Boot**

eMMC Boot is the default boot mode and allows for the fastest boot time. eMMC Boot enables the board to boot out of the box without having to purchase an SD card or an SD card writer.

6.3.1.2 **SD Boot**

SD Boot boots from the uSD slot. SD Boot can be used to override what is on the eMMC device. SD Boot can be used to program the eMMC when used in the manufacturing process or for field updates.

6.3.1.3 **Serial Boot**

Serial Boot uses the serial port to allow downloading of the software directly. A separate serial cable is required to use the serial port.

6.3.1.4 **USB Boot**

USB Boot supports booting over the USB port.

6.3.2 **Boot Mode Switch**

A switch is provided to allow switching between modes. Holding the switch down during boot without an SD card forces the boot source to be the USB port. If nothing is detected on the USB port, the switch will go to the serial port for download. Without holding the switch, the board boots from eMMC. If eMMC is empty, then the switch will try booting from the uSD slot, followed by the serial port, and then the USB port.

6.3.3 **U-Boot Network Configuration**

In order to download images from the TFTP server, the network settings in U-Boot need to be configured.

When booting for the first time, U-Boot tries to fetch the MAC address from the env space. If MAC address returns empty, U-Boot looks for the MAC address in the eFuse registers in the Control module space and sets the "ethaddr" variable in the env appropriately. The ethaddr can also be set using the setenv/saveenv commands. In such cases, the user-set MAC address will take effect on subsequent reboot only.

To set a different MAC address, use the following command.

```
U-Boot# set ethaddr <MAC address, e.g. 08:11:23:32:12:77>
```
## Dynamic IP

Run the dhcp command to obtain the IP address from the DHCP server on the network which the EVM is connected to.

```bash
U-Boot# setenv serverip <tftp server in the network>
U-Boot# dhcp
U-Boot# saveenv
```

### UART Boot

This section describes how to boot from UART using TeraTerm.

1. Turn on EVM with switch settings for **UART boot**.
2. When "CCCC" characters appear on the TeraTerm window, from the File Menu, select Transfer → XMODEM → Send (1K mode).
3. Select "u-boot-spl.bin" for the transfer.
4. After the image is successfully downloaded, the ROM will boot the SPL.
5. When "CCCC" characters appear on the TeraTerm window, from the File Menu, select Transfer → YMODEM → Send (1K mode).
6. Select "u-boot.img" for the transfer.
7. After the image is successfully downloaded, U-Boot will boot.
8. Hit <Enter> and go to the U-Boot prompt "U-Boot#".

## Flasing Images to SPI in UART Boot Mode

This section describes how to flash the SPI images from UART boot mode.

1. Boot using **UART boot mode**. After the U-Boot prompt comes up, the images for the first and second stages can be flashed to SPI for persistent storage.
2. Configure the **U-Boot network settings** for either static or dynamic IP.
3. Set the tftp server.

```bash
U-Boot# setenv serverip <tftp server in the network>
```
4. Select the SPI flash for SPL and U-Boot images.

```bash
U-Boot# sf probe 0
```
5. Erase the SPI flash.

```bash
U-Boot# sf erase 0 +E0000
```
6. Download SPL from the TFTP server and write to the SPI flash.
7. Execute the following code.

```bash
U-Boot# tftp MLO.byteswap
U-Boot# sf write ${loadaddr} 0 ${filesize}
```
8. Download U-Boot from the TFTP server and write to the SPI flash.
9. Execute the following code.

```bash
U-Boot# tftp u-boot.img
U-Boot# sf write ${loadaddr} 0x80000 ${filesize}
```
10. Download the kernel image from the TFTP server, erase, and write to the SPI flash.
11. Execute the following code.

```bash
U-Boot# tftp uImage
```
12. Execute the following code.

```bash
U-Boot# sf erase 0xE0000 0x362000
U-Boot# sf write ${loadaddr} 0xE0000 ${filesize}
```
13. Set boot switch settings for **SPI boot** and reboot the board.
14. If no error messages are display and the U-Boot prompt comes up, SPI boot is successful.
6.3.5 Flashing Images to NAND in UART Boot Mode

This section describes how to flash the NAND images from UART boot mode.

1. Boot using UART boot mode. After the U-Boot prompt comes up, the images for the first and second stages can be flashed to SPI for persistent storage.

2. Configure the U-Boot network settings for either static or dynamic IP.

3. Set the tftp server.
   
   U-Boot# setenv serverip <tftp server in the network>

4. Download SPL from the TFTP server, erase, and write image to NAND flash.

5. Execute the following code.
   
   U-Boot# tftp MLO

6. Execute the following code.
   
   U-Boot# nand erase 0x0 0x20000
   U-Boot# nand write ${loadaddr} 0x0 0x20000

7. Download U-Boot from TFTP server, erase, and write image to NAND flash.

8. Execute the following code.
   
   U-Boot# tftp u-boot.img

9. Execute the following code.
   
   U-Boot# nand erase 0x80000 0x1e0000
   U-Boot# nand write ${loadaddr} 0x80000 0x1e0000

10. Download the kernel image from the TFTP server, erase, and write image to NAND flash.

11. Execute the following code.
    
    U-Boot# tftp uImage

12. Execute the following code.
    
    U-Boot# nand erase 0x280000 0x500000
    U-Boot# nand write ${loadaddr} 0x280000 0x500000

13. Set boot switch settings for NAND boot and reboot the board.

14. If no error messages are display and the U-Boot prompt comes up, NAND boot is successful.
7 Test Data

- Hardware set
  - Tx: DC board
  - 15-V Power Supply
  - Used WE transformer

- Software set
  1. Prime version 7.9.1.0 software tested at the single phase meter and Prime version 3.5.0.0 tested at the DC side
  2. G3 version 7.0.1.2 software tested at the single phase meter and GE version 4.0.0.1 tested at the DC side

- EVM at room temperature
  - 18-dB EVM achieved
  - Uncoded D8PSK received without any errors

Table 8. Three Phase Data Concentrator Test Results

<table>
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<tr>
<th>TEST NUMBER</th>
<th>TEST TYPE</th>
<th>TEST DATE</th>
<th>TEST RESULT SUMMARY</th>
<th>PASS/NO PASS</th>
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<tbody>
<tr>
<td>1</td>
<td>CENELEC compliance with PRIME</td>
<td>8/16/2013</td>
<td>CENELEC pass with 3 dB margin</td>
<td>Pass</td>
</tr>
<tr>
<td>2</td>
<td>PRIME signal injection on 2 Ohm load &gt; 1 Vrms with 100% duty cycle</td>
<td>8/16/2013</td>
<td>Measured ~1.02 Vrms on 2-Ohm load</td>
<td>Pass with 1.02 Vrms</td>
</tr>
<tr>
<td>3</td>
<td>EVM Tests</td>
<td>8/16/2013</td>
<td>18-dB EVM at the room temp</td>
<td>Pass</td>
</tr>
<tr>
<td>4</td>
<td>Sensitivity tests</td>
<td>8/16/2013</td>
<td>82-dB attenuation for PRIME BPSK (spec = 60)</td>
<td>Pass (PRIME Tested at 83-dB attenuation)</td>
</tr>
<tr>
<td>5</td>
<td>Maximum input level</td>
<td>8/16/2013</td>
<td>Max input level of 123 dB to receive uncoded 8PSK</td>
<td>Pass (1.28 Vrms input, uncoded D8PSK coding is ok)</td>
</tr>
<tr>
<td>6</td>
<td>ARIB mask</td>
<td>8/16/2013</td>
<td>ARIB conducted emission passed with 3-dB margin</td>
<td>Pass</td>
</tr>
</tbody>
</table>

![Figure 8. CENELEC Mask (PRIME) External Power Supply](d001)

![Figure 9. CENELEC Mask (PRIME) Onboard Power Supply](d002)
Figure 10. CENELEC Mask (G3) External Power Supply

Figure 11. CENELEC Mask (G3) Onboard Power Supply

Figure 12. Conducted Emission For ARIB (G3)

Figure 13. BER Measurements
8 Design Files

8.1 Schematics

To download the Schematics, see the design files at TIDA-00225.

Figure 14. Schematics Page 2 BeagleBone Black Interface Connector on DC-Cape
Figure 15. Schematics Page 3 PLC SOM Connector
Figure 16. Schematics Page 4 PLC Interface
Figure 17. Schematics Page 5 Zero Crossing Detector
NOTE: DIMENSIONS AND LOCATIONS OF THESE CONNECTORS MUST MEET SPECIFICATION FOR INTERFACE MODULES
REFERENCE CC2530EMK USER GUIDE (SWRU208) OR SMART GRID EVM DESIGN FILES
Connector P/N: TFM-110-02-SM-D-A-K-TR (Samtec)

Figure 18. Schematics Page 6 CC Interface 1
Figure 19. Schematics Page 7 RS232
BeagleBone must supply 5VDC power from external power supply.
Recommended power supply: CUI Inc., 5V/2A, EMM505200-P5.
# 8.2 Bill of Materials

To download the bill of materials (BOM), see the design files at [TIDA-00225](https://www.ti.com/).
<table>
<thead>
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<th>ITEM</th>
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<th>VALUE</th>
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8.3  Layer Plots

To download the layer plots, see the design files at [TIDA-00225].

Figure 21. Layer 1 Primary Side
Figure 22. Layer 2 Ground Plane 1

Figure 23. Layer 3 Power
Figure 24. Layer 4 Secondary Side

Figure 25. Primary Side Soldermask
Figure 26. Primary Side Silkscreen
8.4 Multilayer Composite Prints

To download the Altium project files for each board, see the design files at TIDA-00225.
8.5 **Assembly Drawings**

To download the Assembly drawings, see the design files at [TIDA-00225](#).
8.6 **Gerber Files**
To download the Gerber files, see the design files at [TIDA-00225](#).

8.7 **Software Files**
To download the software files for the reference design, see the design files at [TIDA-00225](#).

9 **References**
1. *Beagleboard:BeagleBoneBlack* (Link: [BeagleBone Black](#))
2. *Smart Data Concentrator EVM (TMDSDC3359) Hardware Manual - Key Features* (Link: [TMDSDC3359](#))

10 **About the Author**
*KALLIKUPPA MUNIYAPPA SREENIVASA* is a Systems Architect at Texas Instruments, where he is responsible for developing reference design solutions for the industrial segment. Sreenivasa brings to this role his experience in high-speed digital and analog systems design. Sreenivasa earned his Bachelor of Electronics (BE) in Electronics and Communication Engineering (BC-E&C) from VTU, Mysore, India.
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