TI Designs

24-V DC, 10-A eFuse and Protection Circuit for Programmable Logic Controllers (PLC)

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Design Resources

- **TIDA-00233** Tool Folder Containing Design Files
- **LM5069-2** Product Folder
- **LM5050-1** Product Folder
- **CSD18532Q5B** Product Folder

Design Features

- Protection
  - Configurable Undervoltage Lockout (UVLO) and Overvoltage Lockout (OVLO)
  - Overcurrent Protection (OCP)
  - Reverse Current protection
  - Reverse Polarity Protection
  - Miswire Protection
  - Surge Protection (IEC61000-4-5)
- Low Power Operation
  - 0.5-mA Quiescent Current
  - 99% Efficiency in Normal Operation

Featured Applications

- Programmable Logic Controller
  - Power Supply
  - CPU
  - I/O Module
- Distributed Control System (DCS)
- Motor Control
- Sensor Concentrators

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Figure 1. Use of This Design (Orange Block) in System Context (High Side Driver with 24-V Field Supply)

PLC or Distributed Control System (DCS) I/O modules connected to a field power supply capable of delivering stable 24-V DC at high power benefit from protection on the 24-V, field-input connectors. The reason that the PLC or DCS modules may benefit from protection is due to power-supply faults or miswiring. Power-supply faults or miswiring might damage the modules or cause the modules to not operate correctly. OVLO and UVLO protect integrated circuits (ICs) on the I/O module from voltages outside of the operating range which might permanently damage the modules, make the modules nonfunctional, or cause the modules to operate in an undesired region. An example of an undesired region is the linear region of MOSFETs, with large resulting power dissipation.

A field power supply is often connected to multiple I/O modules. A field power supply is capable of delivering more current than a single I/O module can handle. OCP limits the current from the power supply to the module so that the maximum current does not rise above what the board is designed for. OCP also acts as a short circuit protection (SCP) as the maximum current is limited to 10 A.

The design also acts as a smart diode with protection against reverse current. A reverse current could damage the field power supply and cause other ICs on the module to run hot or cause permanent damage. A Schottky diode is often used to provide protection against reverse current with the disadvantage that the forward-voltage drop causes a permanent power loss. At high currents, a permanent power loss becomes significant in normal operation mode. At 10 A, the forward loss with a Schottky diode is approximately 7 W. At 10 A, the forward loss with the smart diode function in this design is approximately 1 W.

If the field power supply is connected with reverse polarity (which is not unlikely as field power supplies are usually connected with screw terminals), ICs connected after connecting the power supply will not operate as desired and potentially receive permanent damage. The reverse polarity protection in this design will prevent the reverse power from getting into the module. If the field power supply is connected to an input or output of the module, the miswire protection breaks the path that might cause the current to flow from an input or output to the field supply input.

NOTE: Status LEDs on the board indicate input and output voltage.
2 Design Features

2.1 Specifications

Table 1. Specifications(1)

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>SPECIFICATION</th>
<th>UNIT</th>
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<td></td>
<td>SYMBOL</td>
<td>PARAMETER</td>
<td>CONDITIONS</td>
<td>SPECIFICATION</td>
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<td>V\text{IN}</td>
<td>Input voltage</td>
<td>Normal operation</td>
<td>-33</td>
<td>24</td>
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<tr>
<td>I\text{O}</td>
<td>Quiescent current (2)</td>
<td>Normal operation</td>
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<td>µs</td>
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<td>OCP delay</td>
<td>I\text{IN} = 12 V to 30 V</td>
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<td>SCP delay</td>
<td>I\text{IN} &gt; 2 × I\text{OCP}</td>
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<td>µs</td>
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<td>Reverse polarity protection current</td>
<td>V\text{IN} = -30 V or -10 V</td>
<td>0.1</td>
<td>1</td>
</tr>
<tr>
<td>I\text{MIS}</td>
<td>Miswire and reverse-current protection current</td>
<td>V\text{IN} = 10 V, 12 V, or 30 V</td>
<td>2.0</td>
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<td>Miswire and reverse-current protection delay</td>
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<td>40</td>
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</table>

(1) Ambient temperature T\text{A} = 25°C
(2) Without indicator LEDs, the quiescent current is reduced by 2 × I\text{LED} = 2 × 2.2 mA (Vin = 24 V) = 4.4 mA.

3 Block Diagram

![Simplified Block Diagram with the High Power Path between V\text{IN} and V\text{OUT}](image)

Figure 2. Simplified Block Diagram with the High Power Path between V\text{IN} and V\text{OUT}
4 Component Description

4.1 MOSFET Controllers

This design is using two MOSFET controllers to regulate the circuit’s high power path. The LM5069-2 (U1) is a high voltage controller with OVLO, UVLO, and current sense capability over an external shunt resistor. OVLO and UVLO are set with external resistor dividers. The OCP is set with a shunt resistor in the high power path. The LM5069-2 is controlling MOSFET Q1.

The LM5050-1 (U2) is also a MOSFET controller, that with an external MOSFET (Q2), becomes an ideal diode. The ideal diode is used to protect the high power path from reverse current due to miswiring or reverse polarity.

4.2 MOSFET

Two CSD18532Q5B (Q1 and Q2), 60-V, 2.5-mΩ $R_{DS(on)}$ MOSFETs are used in the high power path, connected back-to-back, to control the current. The low $R_{DS(on)}$ helps reduce the power loss and heat dissipation.

5 Circuit Design and Component Selection

![Figure 3. Circuit Schematics](image)

5.1 UVLO and OVLO

From $V_{IN(MIN)}$ to $V_{UVLO\_EN}$, the design blocks $V_{IN}$ from reaching the output terminals (J3 and J4). From $V_{UVLO\_EN}$ to $V_{OVLO\_DIS}$, the design passes $V_{IN}$ to the output. From $V_{OVLO\_DIS}$ to $V_{IN(MAX)}$, the design blocks $V_{IN}$ from reaching the output. For $V_{IN} < V_{IN(MIN)}$ or $V_{IN} > V_{IN(MAX)}$, the behavior is set by the TVS diodes (D1 and D4), which block surge voltages above the reverse standoff voltage $V_R = 33$ V.

Therefore, $V_{IN(MAX)} = 33$ V.

UVLO and OVLO is performed by a function in U1. The resistor divider R1 and R2 is setting the threshold level for OVLO. The resistor divider R3 and R4 is setting the threshold for UVLO. Keeping both dividers separate enables different hysteresis settings for UVLO and OVLO. The resistor values are calculated with Equation 1 through Equation 4.
Once U1 detects a $V_{\text{IN}}$ undervoltage or overvoltage condition, the output is turned off. Shifting load current on the output can lead to input-voltage variations in the supply voltage and trigger repeated lockout conditions. The hysteresis should be selected so that an input-voltage change due to output-current changes does not trigger a lockout. In this design, the overvoltage hysteresis, $V_{\text{OV(HYS)}} (V_{\text{OVLO_DIS}} - V_{\text{OVLO_EN}})$ has been set to 2 V and the undervoltage hysteresis, $V_{\text{UV(HYS)}} (V_{\text{UVLO_EN}} - V_{\text{UVLO_DIS}})$ has been set to 1 V.

UVLO and OVLO resistor divider equations are shown in Equation 1 through Equation 4:

$$R_1 = \frac{V_{\text{OV(HYS)}}}{21 \mu \text{A}}$$  
(1)

$$R_2 = \frac{2.5 \text{ V} \times R_1}{V_{\text{OVLO_DIS}} - 2.5 \text{ V}}$$  
(2)

$$R_3 = \frac{V_{\text{UV(HYS)}}}{21 \mu \text{A}}$$  
(3)

$$R_3 = \frac{V_{\text{UV(HYS)}}}{21 \mu \text{A}}$$  
(4)

If an overvoltage lockout condition is detected by U1, the gate of Q1 will be discharged with 2 mA. Using Q1’s gate capacitance of 5.6 nF as the turn off time, $t_{\text{OVLO}} = 50 \mu\text{s}$.

5.2 Overcurrent Protection (eFuse)

OCP is set by R6 and R7. If the voltage drop across the parallel resistors exceeds 55 mV, which equals 11 A in the high power path, U1 pulls the gate voltage of Q1 low. The $t_{\text{OCP}}$ is measured to 50 µs. If the voltage drop exceeds 110 mV, which equals 22 A (2 × $I_{\text{OCP}}$, short circuit condition) in the high power path, $t_{\text{SCP}}$ is 0.5 µs to prevent damage of Q1. C2 = 0.47 µF gives a 340-ms insertion time. Ambient conditions (for example, temperature and air flow) can vary depending on implementation. Therefore, a thermal analysis is needed to select C2 and R5. R5 = 57.6 kΩ with R6||R7 = 5 mΩ, which corresponds to 100-W power dissipation in Q1. See LM5069 Positive High Voltage Hot Swap / Inrush Current Controller with Power Limiting, Data Sheet LM5069-2 for selection information on selection of C2 and R5.

R6||R7 sets the over current protection, $I_{\text{OCP(MAX)}} = 11$ A. R6||R7 are non-Kelvin type resistors without separate voltage sense pins which cause additional resistance in the layout so that $I_{\text{OCP(TYP)}} = 10.3$ A.

5.3 Reverse Polarity Protection

If the input (J1 and J2) is connected to a power supply with reverse polarity, so that $V_{\text{IN}}$ becomes negative, the design will block this voltage from reaching the output. The input current under this condition is specified by $I_{\text{REV_POL}}$. A negative $V_{\text{IN}}$ will connect D2 with the GND pins of U1 and U2 to $V_{\text{IN}}$. As the $V_{\text{DD}}$ pins of U1 and U2 are connected to the same potential, both devices remain unpowered and Q1 and Q2 remain in high-impedance state. At negative $V_{\text{IN}}$, the body diode of Q1 conducts the input voltage to the drain of Q2. The high impedance in Q2 is blocking the voltage from the output of the design.

5.4 Miswire and Reverse Current Protection

Miswire and reverse-current protection are implemented using U2 to measure the source-drain voltage drop of Q2. If the voltage drop is negative, the gate of Q2 is pulled low, preventing a reverse-current flow to the input. This function also prevents the charge from an external output capacitor to flow back into the power supply, eliminating adverse effects from an input-voltage drop. A short turnoff time is desired to reduce the capacitor discharge from this reverse current. In this design the turnoff time $t_{\text{REV(MAX)}} = 100$ ns.
5.5 Surge Protection

Surge protection is implemented using multiple stages. The first level of protection is given by the TVS diode, D1. When tested at 0.5 kV over 2 Ω, the surge pulse reaches 250 A. In this case, the voltage across D1 will rise above 55 V, and an additional protection stage is activated. The high voltage across D1 is causing a current higher than 22 A through D4, which triggers the short-circuit protection described in Section 5.2. As $t_{SCP} = 0.5$ µs, Q1 will turn to a high-impedance state before the 8/20 us current pulse generates a voltage exceeding 45 V across D4. The designer may add a capacitor to the output of the design covering the power interrupt caused by the surge pulse.
6 Test Setup

6.1 UVLO and OVLO

Power Supply: Hewlett Packard E3631A triple-output DC power supply 0 V to 6V, 5 A and, 0 - ±25 V, 1A
Multimeter: Wavetek 23XT

J1 (red) of the DUT is connected to the positive terminal of the power supply and J2 (black) to the negative terminal. The negative supply is set to 10 V and the positive supply can be adjusted from 0 V to 25 V. For safety reasons, the current limit is set to 50 mA.

The overvoltage lockout thresholds ($V_{OVLO\_DIS}$ and $V_{OVLO\_EN}$) are tested by increasing the positive supply from 20 V until D8 turns off and then decreasing the positive supply until D8 turns on.

The undervoltage lockout thresholds ($V_{UVLO\_DIS}$ and $V_{UVLO\_EN}$) are tested by increasing the positive supply from 0 V until D8 turns on and then decreasing the positive supply until D8 turns off.

![Figure 4. Measurement setup for over and under voltage lockout](image)

6.2 Overcurrent Protection (eFuse)

Power Supply: Agilent 6574A 0 – 60V, 0-A to 35-A DC power supply
Electronic Load: Agilent 6060B 3-V to 60-V, 0-A to 60-A system DC electronic load
Multimeter: METRAHIT pro professional TRMS

J1 (red) of the DUT is connected to the positive terminal of the power supply and J2 (black) to negative terminal. In the first test $V_{IN} = 12$ V, and in the second test, $V_{IN} = 30$ V with the electronic load connected to J3 (red) and J4 (black). Under both test conditions, the load of the DUT is sequentially set to 2 A, 6 A, 8 A, and 10 A. The board temperature is monitored at each test point. At 10 A, the load current is slowly increased until the DUT turns off the output voltage.

WARNING
The operator has to take the usual precautions when handling high currents.
6.3 Reverse Polarity Protection

Power Supply: Hewlett Packard E3631A triple-output DC power supply 0 V to 6V, 5 A and 0 - ±25 V, 1A
Multimeter: Wavetek 23XT

The DUT is connected to the ±25 V output of the power supply. J1 (red) is connected to the negative terminal of the power supply and J2 (black) is connected to the positive terminal. The negative supply is set to 10 V. The positive supply is set to 0 V, resulting in $V_{IN} = -10$ V. This process is repeated for $V_{IN} = -30$ V, with the positive supply set to 20 V. For safety reasons, the current limit is set to 50 mA.

6.4 Miswire and Reverse Current Protection

Power Supply: Hewlett Packard E3631A triple-output DC power supply 0 V to 6V, 5 A and, 0 - ±25 V, 1A
Multimeter: Wavetek 23XT

The DUT is connected to the ±25 V output of the power supply. J3 (red) is connected to the positive terminal of the power supply and J4 (black) is connected to the negative terminal. The negative supply is set to 10 V. The positive supply is set to 0 V, resulting in $V_{IN} = 10$ V. This process is repeated for $V_{IN} = 30$ V, with the positive supply set to 20 V. For safety reasons, the current limit is set to 50 mA.

$I_{MIS}$ is measured with the multimeter (ampere meter) connected to J1 (red) and J2 (black).
6.5 Surge Protection

EFT/Surge/ESD Generator: AMETEK, EM TEST UCS500N
Oscilloscope: Tektronix TPS2014B

The design is tested according to IEC61000-4-5 (1.2/50 µs, 2.0 Ω, 18 uF) ±0.5 kV surge specification. Compliance is confirmed in two separate tests.

6.5.1 Test 1: Power Supply Surge Test

\( V_{IN} = 28 \text{ V} \). The surge pulse is injected using a surge generator with coupling network as described in Figure 8. Test 1 is performed with 4 different loads: open circuit, \( I_L = 280 \text{ mA}, 10\text{A}, \) and short circuit, connected to J3 (red) and J4 (black). The correct function of the design is first verified using a multimeter with a peak detector. A battery-powered oscilloscope is then connected in parallel with the load to record \( U_L \). The surge pulse is applied 5 times at 0.5 kV and 5 times at -0.5 kV.

6.5.2 Test 2: Reverse Power Surge Test

The power supply is connected to J3 and J4 with a voltage set to 28 V. An oscilloscope is connected between J1 and J2 to record transients. The surge pulse is injected using a surge generator with coupling network to J3, as described in Figure 9.

To verify proper operation of the surge protection, Test 1 is repeated after Test 2 with the same DUT, to ensure Test 2 caused no derating.
Reverse surge protection

Figure 9. Measurement Setup for Reverse Power Surge Test
### 7 Test Results

#### 7.1 Measurement Results

Table 2 shows the test results for normal operation and during surge conditions.

**Table 2. Test Results Compared to Design Specification**

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>SPECIFICATION</th>
<th>MEAS.</th>
<th>UNIT</th>
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<tr>
<td></td>
<td></td>
<td></td>
<td>MIN.</td>
<td>TYP.</td>
<td>MAX.</td>
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<tr>
<td>$V_{\text{IN}}$</td>
<td>Input voltage</td>
<td>Normal operation</td>
<td>-33</td>
<td>24</td>
<td>33</td>
</tr>
<tr>
<td>$I_Q$</td>
<td>Quiescent current$^{(1)}$</td>
<td>Normal operation</td>
<td>5</td>
<td>7.6</td>
<td>10</td>
</tr>
<tr>
<td>$V_{\text{OVLO_DIS}}$</td>
<td>OVLO output disabled</td>
<td>$V_{\text{IN}}$ increasing</td>
<td>-</td>
<td>32.5</td>
<td>33.0</td>
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<tr>
<td>$V_{\text{OVLO_EN}}$</td>
<td>OVLO output re-enabled</td>
<td>$V_{\text{IN}}$ decreasing</td>
<td>29.9</td>
<td>30.5</td>
<td>-</td>
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<td>$t_{\text{OVLO}}$</td>
<td>OVLO delay</td>
<td>$V_{\text{IN}}$ increasing</td>
<td>-</td>
<td>50</td>
<td>TBM</td>
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<td>$U_{\text{UVLO_EN}}$</td>
<td>UVLO output enabled</td>
<td>$V_{\text{IN}}$ increasing</td>
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<td>12.64</td>
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<td>$U_{\text{UVLO_DIS}}$</td>
<td>UVLO output disabled</td>
<td>$V_{\text{IN}}$ decreasing</td>
<td>11.29</td>
<td>11.4</td>
<td>-</td>
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<td>$I_{\text{OCP}}$</td>
<td>OCP</td>
<td>$V_{\text{IN}}$ = 12 V or 30 V</td>
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<td>11</td>
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<td>$t_{\text{OCP}}$</td>
<td>OCP delay</td>
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<td>TBM</td>
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<td>$t_{\text{SCP}}$</td>
<td>SCP delay</td>
<td>$I &gt; 2 \times I_{\text{OCP}}$</td>
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<td>TBM</td>
<td>μs</td>
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<td>$I_{\text{REV_POL}}$</td>
<td>Reverse polarity protection current</td>
<td>$V_{\text{IN}}$ = -30 V or -10 V</td>
<td>0.1</td>
<td>1</td>
<td>0.1</td>
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<tr>
<td>$I_{\text{MIS}}$</td>
<td>Miswire and reverse-current protection current</td>
<td>$V_{\text{IN}}$ = 10 V, 12 V, or 30 V</td>
<td>2.0</td>
<td>2.2</td>
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<td>$t_{\text{REV}}$</td>
<td>Miswire and reverse-current protection delay</td>
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<td>40</td>
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<td>TBM</td>
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<td>$V_{\text{SURGE_pp}}$</td>
<td>Peak output voltage during surge</td>
<td>$V_{\text{IN}}$ = 30 V + 500 V surge</td>
<td>0.0</td>
<td>45</td>
<td>V</td>
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$^{(1)}$ Without indicator LEDs, the quiescent current is reduced by $2 \times I_{\text{LED}} = 2 \times 2.2 \text{ mA} (V_{\text{IN}} = 24 \text{ V}) = 4.4 \text{ mA}$. 

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7.2 Surge Protection

Figure 10 through Figure 15 show the output voltage of the protection device at different load conditions during a surge pulse of 500 V. The device is effectively blocking all dangerous input voltages towards the load. The maximum output voltage exists during lightly loaded conditions. In that case, the output voltage reaches its maximum at 45 V before it shuts down for 250 ms. Also, a negative output voltage could be observed, which is low energy and results from capacitive coupling through MOSFETs Q1 and Q2.

Figure 10. Output Voltage of the Protection Device during Surge at No Load

Figure 11. Zoom into the Waveform in Figure 10 at the Surge Location

Figure 12. Output Voltage of the Protection Device during Surge at 100-Ω Load

Figure 13. Zoom into Figure 12
Figure 14. Output Voltage of the Protection Device during Surge at 15-Ω Load

Figure 15. Zoom into Figure 14
8 Design Files

8.1 Schematics

To download the Schematics, see the design files at TIDA-00233.
# Bill of Materials

To download the bill of materials (BOM), see the design files at [TIDA-00233](https://www.ti.com).  

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<td>Texas Instruments</td>
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<td>U2</td>
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8.3 Layout Guidelines

To withstand the IEC61000-4-5 (1.2/50 µs) ±0.5 kV surge specification, the PCB layout needs special attention. The surge current is passed over the pads of D1 and D4. The trace width has to be at least 8 mm for longer traces in free air to support $I_{OCP(MAX)} = 11$ A. As the 24-V pin of D1 has a short trace, D1 provides additional cooling area and the trace width is reduced to 6 mm. The other high power traces are laid out as copper areas.

Q1 and Q2 are cooled using PCB copper area. The PCB copper area size needs to be large enough to dissipate the heat over the design’s operating temperature range. Q1 has a copper area of 1.2 cm² available on the top layer and 1.1 cm² on the bottom layer. Q2 has a copper area of 0.5 cm² available on the top layer and 1.8 cm² on the bottom layer.

R6||R7 are preferably resistors of Kelvin type, where the high power path uses separate connection pads in addition to the pads for the SENSE and V$_{IN}$ pins of the U1. See Figure 17. To optimize the design for footprint, resistors of non-Kelvin type are used, which adds the R6||R7 pads’ resistance so that $I_{OCP(TYP)} = 10.3$ A.

![Figure 17. U1 SENSE and V$_{IN}$ Pin Pad Connection using Resistors of Kelvin Type](image)

![Figure 18. All Layers](image)
8.4 Layer Plots

To download the layer plots, see the design files at TIDA-00233.

Figure 19. Top Silkscreen
Figure 20. Top Solder Mask
Figure 21. Top Layer
Figure 22. Bottom Layer
Figure 23. Bottom Solder Mask
Figure 24. Bottom Silkscreen
Figure 25. Drill Drawing

Figure 26. Board Dimensions
8.5 **Altium Project**

To download the Altium project files, see the design files at [TIDA-00233](#).

![Figure 27. All Layers](image)

8.6 **Gerber Files**

To download the Gerber files, see the design files at [TIDA-00233](#).

8.7 **Assembly Drawings**

![Figure 28. Top Assembly Drawing](image)

![Figure 29. Bottom Assembly Drawing](image)

8.8 **Software Files**

To download the software files, see the design files at [TIDA-00233](#).

9 **References**

1. **LM5050-1/LM5050-1-Q1 High Side OR-ing FET Controller**, Data Sheet [LM5050-1](#)
10 About the Author

INGOLF FRANK is a systems engineer in the Texas Instruments Industrial Automation Team, focusing on programmable logic controller I/O modules. Ingolf works across multiple product families and technologies to leverage the best solutions possible for system level application design. Ingolf earned his Electrical Engineering degree (Dipl. Ing. (FH)) in the field of information technology at the University of Applied Sciences Bielefeld, Germany in 1991.

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