PMP10520 Test Report

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1) Block Diagram

Xilinx Ultrascale Virtex MGT Reference Design

Figure 1. Block Diagram
2) Board Photos

Figure 2. Board Photo Top

Figure 3. Board Photo Bottom
3) Efficiency

The efficiency of the converters is shown in the figures below. The input voltage is set to 5V.

![Diagram](image)

Figure 4. VIN = 5V, MGTAVCC Efficiency
Figure 5. VIN = 5V, MGTA
tTT Efficiency
Figure 6. VIN = 5V, MGTVCCAUX Efficiency
4) **Load Regulation**

The images below show the output load regulation. The input voltage is 5V.

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**Figure 7. VIN = 5V Load Regulation**
Figure 8. VIN = 5V Load Regulation
Figure 9. VIN = 5V Load Regulation
5) **Startup No Load**

The images below shows the startup waveforms. The output is not loaded. The input voltage is set to 5V.

![Waveform Image]

Ch.1: VIN = 5V  
Ch.2: MGTAVCC = 1.0V  
Ch.3: MGTAVTT = 1.2V  
Ch.4: MGTVCXAUX = 1.8V

Figure 10. VIN = 5V Startup with No Load
6) Output Voltage Ripple

The images below shows the output voltage ripple when load is fully applied. The input voltage is 5V.

Figure 11. VIN = 5V, VOUT = 1.0V, IOUT = 20A Output Ripple Voltage
Figure 12. VIN = 5V, VOUT = 1.2V, IOUT = 30A Output Ripple Voltage
Figure 13. VIN = 5V, VOUT = 1.8V, IOUT = 4A Output Ripple Voltage
7) Load Transients

The transient response of the converters is shown below. The input voltage is 5V. The output current is pulsed from no load to 50% load.

Figure 14. VIN = 5V, VOUT = 1.0V, 0A to 10A Load Transient
Figure 15. VIN = 5V, VOUT = 1.2V, 0A to 15A Load Transient
Figure 16. VIN = 5V, VOUT = 1.8V, 0A to 2A Load Transient

8) Bode Plots

Figure 17. MGTAVCC Bode Plot
9) **Thermal Images**

Thermal images for each power supply rail are shown below at full load. While each individual rail is at full load, the remaining rails do not draw any current.
Figure 20. VIN = 5V, VOUT = 1.0V, IOUT = 20A Thermal Image
Figure 21. VIN = 5V, VOUT = 1.2V, IOUT = 30A Thermal Image
Figure 22. VIN = 5V, VOUT = 1.8V, IOUT = 4A Thermal Image
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