**TI Designs**

Adaptive Power Supply for Programmable Logic Controller Analog Output Module With Output Channel Protection

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TI Designs provide the foundation that you need including methodology, testing, and design files to quickly evaluate and customize the system. TI Designs help you accelerate your time to market.

**Design Resources**

- TIDA-00231: I/P O/P Module Design
- TIDA-00123: I/O Controller Design Files
- LM5069: Product Folder
- LM5017: Product Folder
- TPS70933: Product Folder
- DAC8760: Product Folder
- ISO7420: Product Folder
- ISO7141: Product Folder
- TPS70950: Product Folder
- TS5A3159: Product Folder
- TPS61170: Product Folder
- OPA2171: Product Folder

**Design Features**

- 16-Bit User Configurable Analog Current Output
- Programmable Current Range: 0 to 20 mA, 4 to 20 mA, 0 to 24 mA
- Accuracy:
  - Un-Calibrated Accuracy: ±0.2% Full-Scale Range (FSR)
  - Calibrated Accuracy: 0.053% FSR at 25°C
- Adaptive Power Supply Reduces System Power Dissipation—FET Power Losses Limited to > 50 mW for Typical Load Resistance > 300 Ω
- Reverse Voltage Protection for Analog Output (AO)
- Onboard Isolated Fly-Buck™ Power Supply With Inrush Current Protection
- Slim Form Factor 96 × 50.8 × 10 mm (L × W × H)
- Pluggable to I/O Controller Platform (TIDA-00123) for Easy Evaluation
- LabVIEW™-Based GUI for Signal-Chain Analysis and Functional Testing
- Designed to Comply With IEC61000-4 Standards for ESD, EFT, and Surge

**Featured Applications**

- Programmable Logic Controller (PLC), DCS, and PAC
  - AO
  - Mixed Modules
  - Transducer Modules Data Acquisition Systems
- Test and Measurement

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1 Introduction

In PLC systems, analog output (AO) modules are used to control actuators, valves, and motors in process control environments. The load resistor value for standard analog current output modules can range typically from 1 to 1000 $\Omega$. The traditional 0- to 20-mA output driver stages must operate on at least 24 V to provide a sufficient voltage to drive high value resistive loads. However, for the low-value resistive loads, the fixed value high-voltage supply results in significant internal power dissipation that can impact overall efficiency and additional board space is required.

The TIDA-00231 design provides a unique power saving solution for a digital-to-analog converter (DAC)-based analog current output modules with an adaptive power supply. The module operates on an industrial standard 24-V DC supply. The design uses digital isolators and a Fly-Buck converter along with transformer for isolation. The isolation barrier isolates the module from the field to protect against ground loops and to ensure robustness against external events often encountered in harsh industrial environments.

The module has been designed to be pluggable to the I/O controller platform (TIDA-00123) for quick testing and evaluation. The AO channel includes onboard protection circuitry in compliance with regulatory IEC61000-4 standards: electrostatic discharge (ESD), electrical fast transient (EFT), and electrical surge requirements. The design files such as schematics, bill of material (BOM), PCB layout plots, Altium files, Gerber files, performance test reports, and TM4C123 Tiva™ C Series MCU software are provided.
2 Design Specification and Features

Table 1 provides specifications and features of the AO module with adaptive power supply.

Table 1. Specifications of AO Module

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SPECIFICATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of channels</td>
<td>Single channel (current programmable)</td>
</tr>
<tr>
<td>Output range</td>
<td>Current 0 to 20 mA, 4 to 20 mA, 0 to 24 mA</td>
</tr>
<tr>
<td>Load impedance</td>
<td>1 to 1000 Ω</td>
</tr>
<tr>
<td>Settling time (adaptive power supply disable)</td>
<td>25 µs</td>
</tr>
<tr>
<td>Output current settling time (adaptive power supply enable)</td>
<td>1 ms</td>
</tr>
<tr>
<td>Overall accuracy (un-calibrated)</td>
<td>Current input: &lt; ±0.2% full scale at 25°C</td>
</tr>
<tr>
<td>Input supply voltage range</td>
<td>24 V nominal (18 to 30 V)</td>
</tr>
<tr>
<td>Power supply isolation</td>
<td>1500-V AC for one minute (withstand)</td>
</tr>
<tr>
<td>ESD immunity</td>
<td>IEC 61000-4-2 8-KV air discharges</td>
</tr>
<tr>
<td></td>
<td>4-KV contact discharges</td>
</tr>
<tr>
<td>EFT immunity</td>
<td>IEC 61000-4-4: ±2 KV @ 5 KHz on signal ports</td>
</tr>
<tr>
<td>Surge transient immunity</td>
<td>IEC 61000-4-5: ±1 KV line-earth (CM) on signal ports</td>
</tr>
<tr>
<td>Ambient operating temperature</td>
<td>0°C to 60°C</td>
</tr>
<tr>
<td>Form factor (L x W)</td>
<td>90 x 50.8 mm (Small industrial form factor)</td>
</tr>
</tbody>
</table>

3 System Block Diagram

Figure 1. Top-Level Block Diagram
4 Circuit Description

The design uses the DAC8760, a 16-bit programmable current output DAC suitable for PLCs and distributed control systems (DCSs). The DAC8760 is a fully programmable 16-bit voltage and current output DAC, capable of programming ranges from 4 to 20 mA, 0 to 24 mA, 0 to 5 V, 0 to 10 V, ±5 V, and ±10 V. The TIDA-00231 reference design is focusing on the current output. The current output needs about a 2-V headroom, meaning the 24-mA current output can drive a load up to approximately 1000 Ω with a 26-V supply. The AVDD supply range of the DAC8760 is from 11 to 36 V.

The adaptive power supply uses the TPS61170, which drives the output stage of the DAC8760 by dynamically adjusting boost voltage based on voltage drop across current output driver FET inside the DAC8760. The boost converter operates on 12 V and maintains the 2-V headroom on the output stage regardless of the load resistance, thereby reducing the internal power dissipation by a factor of approximately one-third compared with the fixed value supply. The boost converter output can be as high as 28 V for the light loads, which is within the operating value of 11- to 36-V specifications for the DAC8760.

The OPA2171 is configured as a differential amplifier with unity gain and used to sense the drop across output FET driver inside DAC8760. The drop across FET is feedback to the TPS61170 feedback pin to regulate the output voltage dynamically. The design can be customized for the DAC8552, XTR111, or a different current output driver keeping adaptive power supply block same.

To generate isolated power supply, the design uses a low-cost LM5017, a constant on-time synchronous buck regulator in Fly-Buck configuration with an external transformer. The LM5017 has a wide-input supply range, making it ideal for accepting 24-V industrial supplies. The device can accept up to 100 V, making it reliable against input transients. The Fly-Buck power supply isolates and steps down the input voltage to 6.5 V and 12 V. The LM5017 features a number of other safety and reliability functions, such as undervoltage lockout (UVLO), thermal shutdown, and peak current limit protection. The module is hot-swappable, so it can be inserted or removed from the socket in the backplane without disturbing system power. The hot-swappable feature is accomplished using the LM5069.

The digital interface of the DAC8760 circuit operates on a 5-V supply. The TPS70950, a low-drop regulator, generates 5 V from a 6.5-V rail. The functional isolation of digital signals between the host microcontroller and the process control side is achieved using ISO7141 and ISO7420 digital isolators. The module has an onboard EEPROM to store calibration data and configuration data. This reference design also highlights the TI products like the inrush current-limit controller, the isolated Fly-Buck controller, and the low-noise LDO that can be used in the PLC signal chain.
The system has a protection circuitry which makes use of reverse polarity, transient voltage suppressors (TVSs), and ESD diodes. It protects the AO signal against the following:

- External reverse voltage
- Short circuit encountered due to wiring mistakes
- High voltage fast transient events, which are often expected in an industrial harsh environment

Figure 2. Conceptual Schematic Diagram
5 Circuit Design and Component Selection

5.1 Isolated Power Supply

Functional requirements for isolated power supply block:

- Input voltage: 24 V (±20%)
- Output voltage rails: 12 V and 5 V
- Module shall be hot-swappable and shall limit the inrush current
- UV and OV protection
- Power and signal isolation between controller and field side
- Cost and space effective

The module is rated for a nominal power supply input of 24-V DC. For maximum flexibility, module can accept supply voltages in the range of 18-V to 30-V DC.

The LM5069, a positive voltage inrush current protection controller, provides intelligent control of the power supply connections during insertion and removal of a module from live system or power source. The LM5069 provides inrush current limiting during turn-on and monitoring of the load current for faults during normal operation. Additional functions include UVLO and overvoltage lockout (OVLO) to ensure voltage is supplied to the load only when the system input voltage is within a range. The inrush current of the module is limited to 2.75 A. The current limit and power dissipation in the external series pass N-Channel MOSFET are programmable, ensuring operation within the safe operating area (SOA).

![Inrush Current Limit Circuit](image)

The desired current limit threshold:

\[
I_{\text{LIM}} = \frac{55 \text{ mV}}{R_{28}} = \frac{55 \text{ mV}}{20 \text{ m}\Omega} = 2.75 \text{ A}
\]  

For proper operation of the device, the current sense resistor R3 must be smaller than 100 mΩ.

**NOTE:** The current sense resistor (R3) must be placed close to the LM5069. Make connections from R3 to the LM5069 using the Kelvin technique. Refer to Figure 4.
Kelvin sense connection

Figure 4. Kelvin Sense Connection for Sense Resistor

UVLO and OVLO

![Schematic diagram of UVLO and OVLO using external resistor](image)

Figure 5. UVLO and OVLO Using External Resistor

To define all four thresholds accurately, use two resistors each for UVLO and OVLO.
Upper and Lower UVLO Thresholds

\[ V_{UV(HYS)} = \frac{V_{UVH} - V_{UVL}}{2V} = \frac{2V}{21\mu A} = \frac{2.5V \times R46}{V_{UVL} - 2.5V} = \frac{2.5 \times 71.5k}{15V - 2.5V} = 14.3k \]  

Therefore, \( V_{UVH} = 16.50 \) V and \( V_{UVL} = 15 \) V with hysteresis of 1.5 V that keeps the device from responding to power-on glitches during start up.

Choose Upper and Lower OVLO Thresholds

\[ R1 = \frac{V_{OVH} - V_{OVL}}{2V} = \frac{2V}{21\mu A} = 95.3k \]  
\[ R3 = \frac{2.5V \times R1}{V_{OVH} - 2.5V} = \frac{2.5V \times 95.3k}{36V - 2.5V} = 7.11k = 7.15k(\text{standrd value}) \]  

Therefore, \( V_{OVH} = 35.82 \) V and \( V_{OVL} = 33.82 \) V with hysteresis of 2 V.

---

Refer to the LM5069 datasheet and the LM5069EVAL Evaluation Board for device operation, design procedure, and recommended PCB layout guidelines.

In industrial systems, signals are transmitted from a variety of sensors to a central controller for processing and analysis. To maintain safe voltages at the user interface, and to prevent transients from being transmitted from the sources, galvanic isolation is required. Galvanic isolation also avoids ground loops which reduces ground bounce. The LM5017 is a synchronous buck regulator with integrated MOSFET. The LM5017 is configured in Fly-Buck topology to generate non-isolated 3.3 V and isolated 5 and 12 V from 24-V DC. An isolated Fly-Buck converter uses a coupled inductor windings to generate isolated outputs. In Fly-Buck topology, there is no need for an opto-coupler or auxiliary winding as the secondary output closely tracks the primary output voltage, resulting in a cost-effective and smaller-sized solution.
<table>
<thead>
<tr>
<th>SR. NUMBER</th>
<th>DESIGN SPECIFICATIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Input voltage range ($V_{IN}$)</td>
</tr>
<tr>
<td>2</td>
<td>Primary output voltage ($V_{OUT1}$)</td>
</tr>
<tr>
<td>3</td>
<td>Secondary output voltage ($V_{OUT2}$)</td>
</tr>
<tr>
<td>4</td>
<td>Secondary output voltage ($V_{OUT3}$)</td>
</tr>
<tr>
<td>6</td>
<td>Primary load current ($I_{OUT1}$)</td>
</tr>
<tr>
<td>7</td>
<td>Secondary load current ($I_{OUT2}$)</td>
</tr>
<tr>
<td>8</td>
<td>Secondary load current ($I_{OUT3}$)</td>
</tr>
<tr>
<td>9</td>
<td>Switching frequency ($f_{SW}$)</td>
</tr>
</tbody>
</table>

The non-isolated output voltage ($V_{CC\_NON\_ISO}$) is set by two external resistors (R3, R70).

The regulated output voltage is calculated as follows:

$$V_{CC\_NON\_ISO} = 1.225 \times \left(1 + \frac{R41}{R4}\right) = 1.225 \times \left(1 + \frac{196 \, k}{9.09 \, k}\right) = 10.40 \, V$$  \hspace{1cm} (6)

The operating frequency can be calculated as follows:

$$F_{SW} = \frac{V_{OUT}}{10^{-10} \times R_{ON}}$$

$$R_{ON} = \frac{10.4 \, V}{10^{-10} \times 1 \, MHz} = 104 \, k\Omega$$  \hspace{1cm} (7)

The closest standard available value is 100 kΩ. The minimum recommended on-time is 100 ns at max input voltage.

$$T_{ON\, MAX} = \frac{10^{10} \times R_{ON}}{V_{IN\, MIN}} = 0.67 \, \mu s$$  \hspace{1cm} (8)

Similarly,

$$T_{ON\, MIN} = \frac{10^{10} \times R_{ON}}{V_{IN\, MAX}} = 0.29 \, \mu s$$  \hspace{1cm} (9)

$V_{CC\_NON\_ISO}$ is given to TPS70933DBVT LDO that generates $+3.3V_{\_NON\_ISO}$ and capable of delivering 20 mA of output current. The $+3.3V_{\_NON\_ISO}$ is used to power-up an EEPROM and two digital isolators.

**Selection of Rectifier Diode D2**

The reverse bias voltage across D2 when the high side buck switch is on:

$$V_{D2} = \frac{N_{sec}}{N_{pri}} \times V_{IN\, MAX} = \frac{1.55}{1} \times 35 = 23 \, V$$  \hspace{1cm} (10)

Considering safety margin the PIV of secondary diode should be greater than 35 V. Therefore, a 60-V Schottky diode PMEG6010CEH,115 is selected.

Rectified output ($+V_{CC\_ISO}$) on the secondary side will be

$$+V_{CC\_ISO\_1} = \left(\frac{N_{sec1}}{N_{pri}} \times V_{CC\_NON\_ISO}\right) - VFD = 6.71 - 0.3 = 6.41 \, V$$

$$+V_{CC\_ISO\_2} = \left(\frac{N_{sec2}}{N_{pri}} \times V_{CC\_NON\_ISO}\right) - VFD = 13.1 - 0.5 = 12.51 \, V$$  \hspace{1cm} (11)

Refer to the LM5017 datasheet for device operation and AN2292 application note for Fly-Buck converter design procedure and recommended PCB layout guidelines.
Table 3. Design Specification and Key Design Parameters

<table>
<thead>
<tr>
<th>SR. NO.</th>
<th>DESIGN SPECIFICATIONS</th>
<th>KEY PARAMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Input Voltage Range ($V_{IN}$)</td>
<td>6.5-V DC</td>
</tr>
<tr>
<td>2</td>
<td>Output Voltage ($V_{OUT}$)</td>
<td>5 V (Fixed)</td>
</tr>
<tr>
<td>3</td>
<td>Output current ($I_{OUT}$)</td>
<td>50 mA</td>
</tr>
<tr>
<td>4</td>
<td>$V_{DO}$</td>
<td>200 to 300 mV @ 50 mA</td>
</tr>
<tr>
<td>5</td>
<td>Thermal shutdown at V$_{J,A}$</td>
<td>170°C</td>
</tr>
<tr>
<td>6</td>
<td>$T_{J,MAX}$</td>
<td>125°C</td>
</tr>
<tr>
<td>7</td>
<td>Junction-to-ambient thermal resistance ($\theta_{JA}$)</td>
<td>66.2°C/W</td>
</tr>
</tbody>
</table>

Input and Output Capacitors
The TPS7A16 family linear regulators achieve stability with a minimum input capacitance of 0.1 µF and output capacitance of 2.2 µF. The 22-µF, X5R ceramic capacitor is connected to maximize AC performance and to achieve better stability over temperature.

Although an input bulk capacitor is not required for stability, it is good analog design practice to connect a 1- to 22-µF capacitor from $V_{IN}$ to GND. This design has a connected 22-µF capacitor at the input. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR.

Thermal Protection
Thermal protection in TPS7A1650 disables the output when the junction temperature rises to approximately 170°C, allowing the device to cool. When the junction temperature cools to approximately 150°C, the output circuitry is again enabled.

Power Dissipation

Power dissipation, $PD = (V_{IN} - V_{OUT}) \times I_{OUT}$

$= (6.5 - 5) \times 50$ mA

$= 75$ mW

$T_{J} = T_{A,MAX} + (\theta_{JA} \times PD)$

$= 70 + (66.2 \times 75$mW$)$

$= 74.97$°C

$T_{J} < T_{J,IC}$; therefore, there is no need for a heat sink for the TPS7A1650.

Refer to the TPS7A1650 datasheet for device operation and recommended PCB layout guidelines.
5.2 DAC8760

The DAC8760 is designed for industrial and process control applications. The DAC8760 can be programmed as a current output with a range of 4 to 20 mA, 0 to 20 mA, or 0 to 24 mA; or as a voltage output with a range of 0 to 5 V, 0 to 10 V, ±5 V, or ±10 V, with a 10% overrange (0 to 5.5 V, 0 to 11 V, ±5.5 V, or ±11 V). The TIDA-00231 reference design focuses on the current output. The DAC8760 internal block diagram is shown in Figure 7.

![Figure 7. Internal Block Diagram of DAC8760](image_url)

5.2.1 Current Output

Design requirements and specifications:
- 16-bit resolution
- Current output: 4 to 20 mA; 0 to 20 mA; 0 to 24 mA
- ±0.1% FSR total unadjusted error (TUE) max
- Internal 5-V reference (10 ppm/°C, max)
- Wide temperature range: –40°C to 125°C

The DAC8760 current output stage consists of a pre-conditioner and a current source. This stage provides current output according to the DAC code. The output range can be programmed as 0 to 20 mA, 0 to 24 mA, or 4 to 20 mA. The maximum compliance voltage on pin IOUT equals (AVDD – 2 V). In single power supply mode, the maximum AVDD is 36 V, and the maximum compliance voltage is 33.5 V. After power-on, the IOUT pin is in Hi-Z state, with no output. A 15-kΩ precision, low-drift current-setting resistor (R33) is connected to ISET-R pin to improve stability of the current output over temperature. The equation for DAC 16-bit code to current output is:

\[
I_{\text{OUT}} = 20 \text{ mA} \times \frac{\text{Code}}{2^N}
\]

For a 0- to 20-mA output range:

\[
I_{\text{OUT}} = 20 \text{ mA} \times \frac{\text{Code}}{2^N}
\]

For a 0- to 24-mA output range:

\[
I_{\text{OUT}} = 24 \text{ mA} \times \frac{\text{Code}}{2^N}
\]

where
- Code in the decimal equivalent of the code loaded to the DAC
- \(N\) is the bits of resolution, 16 for DAC8760
5.2.2 SPI to DAC8760

The DAC8760 is controlled over a versatile four-wire serial interface (SDI, SDO, SCLK, and LATCH) that can operate at clock rates of up to 31 MHz and is compatible with SPI, QSPI™, Microwire™, and digital signal processing (DSP) standards. The SPI communication command consists of a write address byte and a data word for a total of 24 bits.

![Figure 8. DAC8760 Write Mode Timing](image)

![Figure 9. DAC8760 Readback Mode Timing](image)

5.2.3 Digital Signal Isolation

In industrial systems, signals are transmitted from a long distance and a variety of sensors to a central controller for processing and analysis. To protect from damage, the AO modules require isolation from the backplane and other AO modules. This isolation is typically accomplished by isolating the digital signals between the host processor or controller and the DAC in the AO circuit. To maintain safe voltages at the user interface, and to prevent transients from being transmitted from the sources, galvanic isolation is preferred.

The four serial data signals required to communicate bi-directionally with the DAC8760 are SCLK, DIN, SDO, and LATCH. The ISO7141CC is a 40-Mbps digital isolator that features a 2.5-kVRMS galvanic isolation for one minute. Similarly, the ISO7421 Dual Digital Isolator isolates control signals of power supply and feedback to the TPS601170. Both the devices have achieved UL, CSA, and VDE safety approvals.
5.3 Adaptive Power Supply

The onboard TPS61170-based DC-to-DC boost converter uses a constant frequency scheme to step up an input of 12 V to drive the DAC8760 output driver. When a channel current output is enabled, the converter regulates the Vboost_out supply to 12 V or (IOUT × RLOAD + Headroom), whichever is greater. The value of the headroom voltage is approximately 2 V.

The TS5A3159A Analog Switch is used to connect the feedback pin of the TPS61170 either to the fixed resistor divider network or to the differential amplifier output, which senses the drop across the DAC8760 driver FET. When the analog switch is set, the feedback pin of the TPS61170 makes connection with fixed value resistor divider network and output of the boost converter is set to fixed value of 29-V DC, meaning adaptive power supply is disabled. When the feedback pin of the TPS61170 is connected to output of the differential amplifier, the TPS61170 regulates its output dynamically based on the DAC8760 internal driver FET drop, meaning an adaptive power supply is enable. The analog switch is used to evaluate the effect of adaptive power supply. In application, the user can directly connect output of differential amplifier output to the feedback pin of the TPS61170.

Figure 10. Simplified Block Diagram for Adaptive Power Supply Block

5.3.1 DC-to-DC Boost Converter

Table 4. Design Specification and Key Design Parameters

<table>
<thead>
<tr>
<th>SR. NO.</th>
<th>DESIGN SPECIFICATIONS</th>
<th>KEY PARAMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Input voltage</td>
<td>12 V (±10%)</td>
</tr>
<tr>
<td>2</td>
<td>Output voltage (VOUT)</td>
<td>12 to 28 V (variable)</td>
</tr>
<tr>
<td>3</td>
<td>Output current (IOUT)</td>
<td>30 mA</td>
</tr>
</tbody>
</table>

\[
D_{\text{MAX}} = \frac{V_{\text{OUT}} - V_{\text{IN}}}{V_{\text{OUT}}}
\]
\[
D_{\text{MAX}} = \frac{28 - 10.5}{28}
\]
\[
D_{\text{MAX}} = 63\% 
\]

This value is less than the TPS61170 maximum duty cycle of 90%.
\[ I_{OUT \text{ MAX}} = \frac{V_{IN} \times I_{\text{LIM}} \times I_{\text{est}}}{1 + \left( \frac{K_{\text{IND}}}{2} \right) \times V_{OUT}} \]
\[ I_{OUT \text{ MAX}} = \frac{10.5 \times 0.96 \times 0.92}{1 + \left( \frac{0.4}{2} \right) \times 28} \]
\[ I_{OUT \text{ MAX}} = 0.27 \text{ A} \]

\[ I_{\text{IN DC}} = \frac{V_{OUT} \times I_{OUT}}{V_{IN \text{ MIN}} \times 0.92} \]

\[ I_{\text{IN DC}} = \frac{(28 \times 30 \text{ mA})}{(10.5 \times 0.92)} \]
\[ I_{\text{IN DC}} = 87 \text{ mA} \]

**Inductor:**

\[ L > \frac{1}{F_S \times \left( \frac{1}{V_{OUT} + V_F - V_{IN \text{ MIN}}} + \frac{1}{V_{IN \text{ MIN}}} \right) \times I_P} \]

\[ L > \frac{1}{1 \text{ MHz} \times \left( \frac{1}{28 + 0.5 \times 10.5} + \frac{1}{10.5} \right) \times 0.4 \times 87 \text{ mA}} \]
\[ L > 190.30 \mu \text{H} \]
\[ L = 220 \mu \text{H} \]

The TPS61170 has minimum ON pulse width of 40 ns, which sets the limit of the minimum duty cycle of the PWM switch, and it is independent of the switching frequency. As the output current drops, the boost converter enters discontinuous conduction mode (DCM). In DCM, the on time is a function of load current. The TPS61170 enters pulse-skipping mode at light load current as light load current requires the switch-on time to be less than 40 ns. To reduce losses during pulse-skipping mode, a higher inductance value of 220 μH is chosen.

The inductor current rating must be higher than

\[ I_{\text{IN DC}} + \frac{I_P}{2} \]
\[ I_{\text{IN DC}} = 87 \text{ mA} + \frac{(0.4 \times 87 \text{ mA})}{2} \]
\[ I_{\text{IN DC}} = 104 \text{ mA} \]

The VLCF5028T-221MR22-2 from TDK, capable of handling 0.22 A with a small footprint.

**Schottky Diode**

Even with an ideal PCB layout containing short traces to minimize stray inductance and capacitance, the switching node of the boost converter may exhibit ringing up to 30% higher than the output voltage. Therefore, in this design a 40-V rated diode is selected to accommodate such ringing. Also, a diode with a 150°C thermal rating is selected, which is high enough to accommodate power dissipation of approximately:

\[ P_{\text{DIODE}} = I_{OUT} \times V_F \]
\[ P_{\text{DIODE}} = 30 \text{ mA} \times 0.4 \text{ V} \]
\[ P_{\text{DIODE}} = 12 \text{ mW} \]
The "Schottky diode MBR0540T1G" from "ON Semiconductor" is found suitable for the above requirement.

Thermal Resistance – Junction-to-Ambient (θ_{T,J,A}) for MBR0540G = 206°C/W

\[ T_J = 70 + \theta_{T,J,A} \times P_D \text{DIODE} \]

\[ T_J = 70 + 206 \times 12 \text{ mW} \]

\[ T_J = 73^\circ \text{C} \]

(20)

\[ T_J \text{ (Calculated)} < T_{J \text{ MAX}} \text{ of diode (150^\circ \text{C})} \]

Assuming a ceramic output capacitor with negligible ESR and the output ripple specification \( V_{\text{RIPPLE}} = 50 \text{ mVpp} \), the minimum output capacitance is

\[ C_{\text{OUT}} > \frac{(V_{\text{OUT}} - V_{\text{IN}}) \times I_{\text{OUT}}}{V_{\text{OUT}} \times F_S \times V_{\text{RIPPLE}}} \]

\[ C_{\text{OUT}} > \frac{[28 - 12] \times 30 \text{ mA}}{28 \times 1 \text{ MHz} \times 50 \text{ mV}} \]

\[ C_{\text{OUT}} = 3.42 \mu \text{F} \]

(21)

The GRM31CR71H225KA88L 2.2-\( \mu \text{F} \) capacitors from Murat are connected in parallel. Adding a ferrite bead at the output of the supply enhances the noise performance of the system. The boost converter output capacitor, ferrite bead, and the bulk capacitor at the input of the DAC8760 form a low-pass filter, which provides attenuation greater than 80 dB at 1 MHz.

Compensating the Control Loop

\[ G(s) = \frac{1.229}{V_{\text{OUT}}} \times \frac{G_{\text{EA}} \times 6 \text{ M\Omega} \times V_{\text{IN}} \times R_{\text{OUT}}}{V_{\text{OUT}} \times R_{\text{SENSE}} \times 2} \times \left[ \frac{1 + \frac{S}{2 \times \pi \times f_{Z}}}{1 + \frac{S}{2 \times \pi \times f_{RHPZ}}} \right] \times \left[ \frac{1 - \frac{S}{2 \times \pi \times f_{Z}}}{1 + \frac{S}{2 \times \pi \times f_{P2}}} \right] \]

where

\[ f_{P2} = \frac{2}{2 \times \pi \times R_{\text{OUT}} \times C_2} = \frac{2}{2 \times \pi \times 300 \text{ \Omega} \times 2 \times 2.2 \mu \text{F}} = 241.14 \text{ Hz} \]

\[ f_{RHPZ} = \frac{R_{\text{OUT}} \times V_{\text{IN}}^2}{2\pi \times L \times V_{\text{OUT}}} = \frac{300 \text{ \mu H}}{2 \times \pi \times 220 \text{ \mu H} \times \left[ \frac{12}{28} \right]} = 217.03 \text{ k} \times 0.184 = 39.93 \text{ kHz} \]

\[ f_{P1} = \frac{1}{2 \times \pi \times 6 \text{ M\Omega} \times C_3} \]

\[ f_{Z} = \frac{1}{2 \times \pi \times R_{3} \times C_3} \]

(22)

\( G_{\text{EA}} \) is the amplifier trans-conductance 320 \( \mu \text{mho} \) and \( R_{\text{OUT}} = 300 \text{ \Omega} \), which is commonly used in the industrial current AO module. For current mode boost power supplies, the inductor is not part of the control loop, and the output capacitor sets the dominant pole, \( f_{P2} \). If the RHPZ is high enough in frequency simply setting the compensation zero, \( f_{Z} \), equal to the dominant pole, \( f_{P2} \), stabilizes the loop. Assuming \( R_3 = 15 \text{ k\Omega} \) per the data sheet recommendation and \( R_{\text{SENSE}} = 200 \text{ m\Omega} \), its approximate maximum value, setting \( f_{Z} = f_{P2} \) gives \( C_3 = 44 \text{ nF} \), which is replaced by the standard value of 47 nF.
Figure 11 shows the Mathcad™ gain and phase of the power stage, $G_T(s)$, with $s = j \times 2 \times \pi \times f$.

Refer to the TPS61170 datasheet [7] and calculation spreadsheet [8] for device operation, design procedure, and design calculations.

5.3.2 Differential Amplifier and Feedback Network

The OPA2171 is a single-supply, low-noise operational amplifier with the ability to operate on supplies ranging from 2.7 V (±1.35 V) to 36 V (±18 V). The OPA2171 can operate with full rail-to-rail input 100 mV beyond the top rail with a very low-bias current of 8 pA. An extended common-mode input range and low-input bias current with low cost make the OPA2171 suitable for this application.

The low-bias current allows using 1-MΩ resistor in feedback and input circuit, which minimizes the output current error. The feedback for the TPS61170 is from the divider network (R31 and R24). The resistors are chosen such that the feedback voltage is 1.23 V when the drop across the DAC8760 drive FET is 2 V. The feedback voltage is compared with the TPS61170 internal feedback reference voltage of 1.23 V. Regulation is achieved by varying the duty cycle of the PWM signal driving the internal switch of the TPS61170.
At the input of the OPA2171, the high-value resistor network divides the input by 20, so the common mode input range is given by:

Total common-mode input range ($V_R$)
$$V_R = 20 \times (5 \text{ V} - 2 \text{ V})$$
$$V_R = 20 \times 3 \text{ V}$$
$$V_R = 60 \text{ V}$$  \hspace{1cm} (23)

Minimum common-mode input signal ($V_L$)
$$V_L = 20 \times (-0.1)$$
$$V_L = -2 \text{ V}$$  \hspace{1cm} (24)

Maximum common-mode input signal ($V_n$)
$$V_R = V_R - V_L$$
$$V_R = 60 \text{ V} - (-2 \text{ V})$$
$$V_R = 62 \text{ V}$$  \hspace{1cm} (25)

Gain calculation:
$$V_+ = V_1 \left( \frac{R_2}{R_1 + R_2} \right)$$
$$V_{OUT1} = V_1 \left( \frac{R_2}{R_1 + R_2} \right) \times \left( \frac{R_4 + R_F}{R_4} \right)$$
$$V_{OUT2} = V_2 \left( \frac{-R_F}{R_3} \right)$$
$$V_{OUT} = \left[ V_1 \left( \frac{R_2}{R_1 + R_2} \right) \times \left( \frac{R_4 + R_F}{R_4} \right) \right] - V_2 \left( \frac{-R_F}{R_3} \right)$$  \hspace{1cm} (26)

With resistor above combination Gain = 1. Therefore, $V_{OUT} = V_1 - V_2$. 
5.4 Protection Circuit

Figure 13 shows output structure of the AO module.

D9 protect the FET from any reverse current when AOUT is accidentally connected to external voltage source.

D10 and D12 are “ESD clamping diodes,” which clamp the voltage to a safe level (AVDD to GND).

Figure 13. Output Structure of AO Module

- A high-voltage Y-cap (C52) is connected between signal and earth to decouple high-frequency transient noises
- A TVS (D13) is used to filter and suppress any external transients. The R38 is a pulse withstanding resistor, used to limit the current through TVS and clamping diodes
- Schottky barrier diodes D10 and D12 clamps any overvoltage to the positive (AVDD) or the ground
- Diodes D9, D10, and D12 provide protection from reverse biasing
5.4.1 Protection for ESD, EFT, and Surge

The analog current output can be directly connected to the external loads over a long distance; therefore, the output ports are susceptible to voltage surges and EFT pulses. The TVS provides highly effective protection against such discharges. When a high-energy transient appears on the AO, the TVS goes from high to low impedance within a few nanoseconds. The TVS can absorb thousands of watts of surge power and clamp the analog input to a preset voltage, thus protecting DAC and precision components from being damaged by the surge.

The output stage is designed to withstand up to 8-kV ESD, 2-kV EFT, and 1-kV Surge. The output channel is protected by a TVS SMCJ28A. The TVS diode clamps the surge voltage to safer limit. In addition, a Y-cap is placed near to output connector to divert transient energy quickly to protective earth. Layout guidelines are followed to ensure compliance to EMC standards.

**TVS Diode Selection**

Consider the case of 1 kV (CM) @ 8/20-μs surge on input lines and do some calculations because the voltage surge has the highest energy.

Impedance in path,

$$Z_{\text{TOTAL}} = Z_{\text{SURGE \_ GENERATOR}} + Z_{\text{CDN \_ NETWORK}} + R_{\text{SERIES \_ RES}}$$

$$= 2 \Omega + 40 \Omega + 10 \Omega = 52 \Omega$$

(27)

The internal overvoltage protection circuit of the DAC8760 can withstand up to AVDD on the IOUT pin. Therefore, the clamping voltage must be less than 40 V.

The SMCJ28CA rating: $V_{\text{BR}} = 31.10$ V, $V_{\text{CMAX}} = 45.4$ V @ 8/20 μs @ $I_{\text{PP}} = 33.1$ A, $P_{\text{PP}} = 1500$ W and maximum leakage current = 1 μA

![Figure 14. Characteristics of TVS Diode](image)

$$V_C = \frac{I_P}{I_{\text{PP}}} \left[ V_C - V_{\text{BR}} \right] + V_{\text{BR}}$$

$$I_P = \frac{(1000 \text{ V} - V_C)}{Z_{\text{TOTAL}}}$$

$$I_P = \frac{(1000 \text{ V} - V_C)}{52 \Omega}$$

(28)

Put $I_P$ into the equation of $V_C$ and solve the equation from SMBJ28CA datasheet values:

$V_C = 35.75$ V

$P_P = V_C \times I_P = 35.75 \text{ V} \times 18.54 \text{ A}$

$P_P = 700$ W

(29)
The ESD clamping diodes further clamp the overvoltage to safe level (Vboost_Out) and protects the DAC8760 I\textsubscript{OUT} from damage.

- TVS diode and Y-cap are placed close to the J2 output connector.
- Used copper plane to ensure a low-impedance path for high-energy transients.

**Figure 15. ESD, EFT, and Surge Protection**

**Working:**
- R38 is a pulse withstanding resistor, which limits the current through D13.
- D13 clamps the voltage to 35.75 V.
- D12 and D10 further clamps the voltage to safe level (equal to AVDD of DAC).
- D9 remains reverse bias and blocks any incoming high voltage pulse reaching to DAC.
5.4.2 Reverse Voltage

The protection circuit also safeguards the AO module in the event of reverse voltage. The diode D9 is connected in series with analog current output for reverse voltage protection. D9 remains in reverse biased and offers high resistance to reverse current flow and ensures reverse voltage is low enough to prevent damage to the DAC8760.

The D12 clamps the positive polarity voltage to AVDD and D10 clamps the negative polarity voltage to GND level. The current through D12 and D10 is limited by R36 and F1. A positive temperature coefficient resistor, F1, is connected in series with the AO for protection circuit. The F1 offers a very low resistance during normal operation with no impact to the rest of the circuit. When the current exceeds the hold current rating, PPTC fuse temperature and resistance rapidly increases. This high-resistance mode limits the current and protects the clamping diode circuit from damage. When current increases beyond \(I_{\text{TRIP}}\) (50 mA), the fuse disconnects AO from the load side. The fuse resistance returns to its normal value when the current flow returns to the nominal limit, which results in less maintenance for remote locations.

![Figure 16. Reverse Voltage Protection](image)
5.5 Interface

The AO module has the following connectors:
1. J1: 2-pin screw terminal type, 2.54-mm pitch connector for connecting protective earth
2. J2: 4-pin screw terminal type, 2.54-mm pitch connector for AO
3. J3: 50-pin connector for connecting SPI, I2C, and power supply from the host controller
6 Test Setup

6.1 Performance Evaluation Test Setup

The Tiva C Series I/O Controller Platform (TIDA-00123) has the required connectors and the MCU to interface with the AO module and is used for performance testing. The 24-V power input to the module is supplied by the TIDA-00123.

Figure 19. Performance Evaluation Test Setup
The complete signal chain performance can be evaluated using a LabVIEW-based GUI. The GUI on the PC connects to the TIDA-00123 through USB interface. The TIDA-00123 then controls the AO module with adaptive power supply through SPI. The output signal is read by 8½-digit multimeter. The GUI saves the data in Microsoft® Excel® format. The extracted data can be used for evaluation.

The equipment used for the testing is as follows:

- 24-V DC power supply with current limit set to 100 mA
- 8½-digit multimeter (3458A Hewlett Packard® make), configured as DC ammeter and connected in series between AO and load resistor
- Two 6½ digit multimeters (34401 A, Agilent make), configured as DC voltmeter and connected in across AO and DAC internal FET
- 1-k/2-W MFR resistor as a load (fixed load) or power decade resistor box (variable load)

The following functionality is provided in the GUI:

- DAC8760 configuration
- Reads and store the analog data using 8½-digit multimeter
- Analog data can be imported to Microsoft Excel format for performance evaluation

**NOTE:** The test data in Section 7 was measured at room temperature using calibrated lab equipment, unless otherwise specified.
7 Test Results

7.1 Accuracy

This test is conducted by a sweeping output current from 0 to 20 mA, keeping the load resistance constant to 1000 Ω, and a $T_A$ at 25°C.

The following steps were carried out to test accuracy:

1. Connect the test setup as shown in Figure 19.
2. Configure the DAC8760 as a current output using the LabVIEW test utility.
3. Set DAC8760 output range to 0 to 20 mA.
4. Set "Start" and "Stop" value to 0 to 216. For full-range performance testing, set these values as 0 to 65535 with step size '1'.
5. Press the "DAC Linearity" tab in GUI.
6. The test results are stored in Microsoft Excel format.
7. The offset and gain calibration is applied to the output current to measure calibrated error in FSR %.

![Figure 21. Accuracy Plot](image-url)
7.2 **Power Saving**

The test explains the improvement in power saving using the adaptive power supply.

7.2.1 **Boost Converter Efficiency**

The efficiency of boost converter is the key parameter in the design. The losses in the boost converter will directly impact the overall power consumption of the system and hence efficiency of the system. Figure 22 shows the efficiency of the TPS61170-based boost converter used as at different load conditions. The efficiency is > 80% at load current greater than 12 mA.

![Figure 22. Boost Converter Output Current versus Efficiency](image)

7.2.2 **Output Current Sweep Keeping Load Resistance Constant**

This test is conducted by a sweeping output current from 0 to 24 mA, keeping the load resistance constant to 1000 Ω, and a $T_A$ at 25°C.

<table>
<thead>
<tr>
<th>DROP ACROSS FET (V)</th>
<th>OUTPUT VOLTAGE (V)</th>
<th>OUTPUT CURRENT (mA)</th>
<th>FET POWER DISSIPATION (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>12.48</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>9.9347</td>
<td>1.9648</td>
<td>1.9954</td>
<td>19.86483004</td>
</tr>
<tr>
<td>7.6783</td>
<td>3.9258</td>
<td>3.9501</td>
<td>30.67488528</td>
</tr>
<tr>
<td>5.4432</td>
<td>5.8875</td>
<td>5.9263</td>
<td>32.61908362</td>
</tr>
<tr>
<td>3.2246</td>
<td>7.8452</td>
<td>7.9894</td>
<td>25.76265149</td>
</tr>
<tr>
<td>2.0298</td>
<td>9.7992</td>
<td>9.9857</td>
<td>20.2690505</td>
</tr>
<tr>
<td>2.0169</td>
<td>11.7468</td>
<td>11.9816</td>
<td>24.16568904</td>
</tr>
<tr>
<td>1.9294</td>
<td>13.688</td>
<td>13.9802</td>
<td>26.9733978</td>
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<tr>
<td>1.8458</td>
<td>15.622</td>
<td>15.9764</td>
<td>29.48923912</td>
</tr>
<tr>
<td>1.7701</td>
<td>17.548</td>
<td>17.9715</td>
<td>31.81135215</td>
</tr>
<tr>
<td>1.7051</td>
<td>19.467</td>
<td>19.9772</td>
<td>34.06312372</td>
</tr>
<tr>
<td>1.6518</td>
<td>21.346</td>
<td>21.9732</td>
<td>36.29533176</td>
</tr>
<tr>
<td>1.6051</td>
<td>23.27</td>
<td>23.9778</td>
<td>38.48676678</td>
</tr>
</tbody>
</table>
Table 6. APS Disable, Output Current Sweep From 0 to 24 mA

<table>
<thead>
<tr>
<th>DROP ACROSS FET (V)</th>
<th>OUTPUT VOLTAGE (V)</th>
<th>OUTPUT CURRENT (mA)</th>
<th>FET POWER DISSIPATION (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>29.374</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>26.988</td>
<td>1.9523</td>
<td>1.98678</td>
<td>53.61921864</td>
</tr>
<tr>
<td>24.843</td>
<td>3.9135</td>
<td>3.98265</td>
<td>98.94097395</td>
</tr>
<tr>
<td>22.647</td>
<td>5.8687</td>
<td>5.98018</td>
<td>135.4331365</td>
</tr>
<tr>
<td>20.505</td>
<td>7.8301</td>
<td>7.97581</td>
<td>163.5439841</td>
</tr>
<tr>
<td>18.356</td>
<td>9.7852</td>
<td>9.97332</td>
<td>183.0702619</td>
</tr>
<tr>
<td>16.211</td>
<td>11.7341</td>
<td>11.9703</td>
<td>194.0505333</td>
</tr>
<tr>
<td>12.084</td>
<td>15.613</td>
<td>15.9879</td>
<td>193.1977836</td>
</tr>
<tr>
<td>9.972</td>
<td>17.541</td>
<td>17.9951</td>
<td>179.4471372</td>
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<tr>
<td>7.8708</td>
<td>19.462</td>
<td>19.9821</td>
<td>157.2751127</td>
</tr>
<tr>
<td>5.779</td>
<td>21.371</td>
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<td>127.0796321</td>
</tr>
<tr>
<td>3.6958</td>
<td>23.271</td>
<td>23.9862</td>
<td>88.64819796</td>
</tr>
</tbody>
</table>

Figure 23. Output Current versus Power Dissipation in FET (Full Range Current Sweep)
7.2.3 Load Resistance Sweep

This test is conducted by sweeping load resistance from 10 to 1000 Ω, keeping the load current constant to 24 mA, and a $T_A$ at 25°C.

### Table 7. APS Disable, Load Resistor Sweep From 10 to 1000 Ω

<table>
<thead>
<tr>
<th>DROP ACROSS FET (V)</th>
<th>OUTPUT VOLTAGE (V)</th>
<th>OUTPUT CURRENT (mA)</th>
<th>FET POWER DISSIPATION (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>26.432</td>
<td>0.13047</td>
<td>24.0092</td>
<td>634.6111744</td>
</tr>
<tr>
<td>24.061</td>
<td>2.5167</td>
<td>23.9985</td>
<td>577.4279058</td>
</tr>
<tr>
<td>21.662</td>
<td>4.9231</td>
<td>23.9921</td>
<td>519.7168702</td>
</tr>
<tr>
<td>19.284</td>
<td>7.3256</td>
<td>23.986</td>
<td>462.546024</td>
</tr>
<tr>
<td>16.857</td>
<td>9.7548</td>
<td>23.9804</td>
<td>404.2376028</td>
</tr>
<tr>
<td>14.469</td>
<td>12.155</td>
<td>23.9754</td>
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<tr>
<td>12.092</td>
<td>14.538</td>
<td>23.9707</td>
<td>289.8537044</td>
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<tr>
<td>9.703</td>
<td>16.937</td>
<td>23.9706</td>
<td>232.5867318</td>
</tr>
<tr>
<td>7.2942</td>
<td>19.367</td>
<td>23.9753</td>
<td>174.8806333</td>
</tr>
<tr>
<td>4.917</td>
<td>21.768</td>
<td>23.9783</td>
<td>117.9013011</td>
</tr>
<tr>
<td>3.0081</td>
<td>24.193</td>
<td>23.9899</td>
<td>72.16401819</td>
</tr>
</tbody>
</table>

### Table 8. APS Enable, Load Resistor Sweep From 10 to 1000 Ω

<table>
<thead>
<tr>
<th>DROP ACROSS FET (V)</th>
<th>OUTPUT VOLTAGE (V)</th>
<th>OUTPUT CURRENT (mA)</th>
<th>FET POWER DISSIPATION (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>9.1989</td>
<td>0.18553</td>
<td>24.0149</td>
<td>220.9106636</td>
</tr>
<tr>
<td>6.8071</td>
<td>2.5658</td>
<td>24.0033</td>
<td>163.3928634</td>
</tr>
<tr>
<td>4.3886</td>
<td>4.983</td>
<td>23.9973</td>
<td>105.3145508</td>
</tr>
<tr>
<td>1.9907</td>
<td>7.3834</td>
<td>23.993</td>
<td>47.7628651</td>
</tr>
<tr>
<td>1.9903</td>
<td>9.8106</td>
<td>23.9869</td>
<td>47.74112707</td>
</tr>
<tr>
<td>1.8835</td>
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<td>1.8035</td>
<td>14.604</td>
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<td>43.2403553</td>
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<td>1.7369</td>
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<td>1.6811</td>
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<td>1.633</td>
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<tr>
<td>1.6068</td>
<td>24.233</td>
<td>23.976</td>
<td>38.5246368</td>
</tr>
</tbody>
</table>
Figure 24. Output Current versus Power Dissipation in FET (Load Resistor Sweep From 10 to 1000 Ω)

7.3 Output Current Settling Time

The output is stepped from 0 to 20 mA with a 1000-Ω load resistance. A low output resistance can result in a better settling time (see Figure 25).

Figure 25. Settling Time
7.4 Pre-Compliance Testing

The AO module has been designed to meet standard EMC requirements for Industrial PLC application. The following EMC tests have been performed.

Table 9. EMC Tests and Standards

<table>
<thead>
<tr>
<th>TESTS</th>
<th>STANDARDS</th>
</tr>
</thead>
<tbody>
<tr>
<td>ESD</td>
<td>IEC61000-4-2</td>
</tr>
<tr>
<td>EFT</td>
<td>IEC61000-4-4</td>
</tr>
<tr>
<td>Surge</td>
<td>IEC61000-4-5</td>
</tr>
</tbody>
</table>

Table 10. Criteria and Performance as per IEC61131-2

<table>
<thead>
<tr>
<th>CRITERIA</th>
<th>PERFORMANCE (PASS) CRITERIA</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>The analog output module shall continue to operate as intended. The module has no loss of function or performance even during the test.</td>
</tr>
<tr>
<td>B</td>
<td>Temporary degradation of performance is accepted. After the test, the analog output module shall continue to operate as intended without manual intervention.</td>
</tr>
<tr>
<td>C</td>
<td>During the test, a loss of functions is accepted, but not the destruction of hardware or software. After the test, the analog output module shall continue to operate as intended automatically after a manual restart or power off/power on.</td>
</tr>
</tbody>
</table>

The targeted accuracy for criteria A is as follows:

- Voltage Input: ±0.2% full scale at 25°C
- Current Input: ±0.2% full scale at 25°C

The next sections explain the test setup, procedures, and observations.
7.4.1 ESD: IEC61000-4-2

7.4.1.1 Test Level and Expected Performance

The ESD level at I/O connectors and the performance criteria expected are as follows:

**Table 11. ESD Test Levels and Performance Criteria**

<table>
<thead>
<tr>
<th>GENERIC TEST STANDARD</th>
<th>TEST LEVEL</th>
<th>PERFORMANCE</th>
</tr>
</thead>
<tbody>
<tr>
<td>ESDIEC 61000-4-2</td>
<td>4 kV contact discharges – Level 2</td>
<td>Criteria B</td>
</tr>
<tr>
<td></td>
<td>8 kV air discharges – Level 3</td>
<td></td>
</tr>
</tbody>
</table>

7.4.1.2 Setup Description

The ESD is injected to the EUT in two ways: contact discharge or air discharge. The EUT is placed on a horizontal coupling plane (HCP) of 160×80-cm dimensions on top of a wooden table 80 cm high and located above ground reference plane. The EUT and its attached cables were isolated from the HCP by a thin insulating support of 0.5-mm thickness. ESDs were applied using an ESD gun directly (through contact or air discharges) or indirectly (through HCP). The EUT operation was monitored after the test. The EUT is tested in active mode using unshielded 3-m cables on I/O ports.

7.4.1.3 Monitoring Methods

1. Connect the shield pin to the same protective earth as the ESD generator.
2. Connect the battery power to avoid earth ground loop.
3. Power on the EUT. EUT software is configured to generate an output of 4 mA and 20 mA alternately for two seconds each.

The AO channel is checked before and after the test. The ESD test is performed as per test levels mentioned in **Table 12**.

7.4.1.4 Results

**Table 12. ESD Test Results**

<table>
<thead>
<tr>
<th>TEST NO.</th>
<th>TEST MODE</th>
<th>OBSERVATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Air 2 kV</td>
<td>Pass</td>
</tr>
<tr>
<td>2</td>
<td>Air –2 kV</td>
<td>Pass</td>
</tr>
<tr>
<td>3</td>
<td>Air 4 kV</td>
<td>Pass</td>
</tr>
<tr>
<td>4</td>
<td>Air –4 kV</td>
<td>Pass</td>
</tr>
<tr>
<td>5</td>
<td>Air 6 kV</td>
<td>Pass</td>
</tr>
<tr>
<td>6</td>
<td>Air –6 kV</td>
<td>Pass</td>
</tr>
<tr>
<td>7</td>
<td>Air 8 kV</td>
<td>Pass</td>
</tr>
<tr>
<td>8</td>
<td>Air 8 kV</td>
<td>Pass</td>
</tr>
<tr>
<td>9</td>
<td>Contact 1 kV</td>
<td>Pass</td>
</tr>
<tr>
<td>10</td>
<td>Contact –1 kV</td>
<td>Pass</td>
</tr>
<tr>
<td>11</td>
<td>Contact 2 kV</td>
<td>Pass</td>
</tr>
<tr>
<td>12</td>
<td>Contact –2 kV</td>
<td>Pass</td>
</tr>
<tr>
<td>13</td>
<td>Contact 4 kV</td>
<td>Pass</td>
</tr>
<tr>
<td>14</td>
<td>Contact –4 kV</td>
<td>Pass</td>
</tr>
<tr>
<td>15</td>
<td>HCP 2 kV</td>
<td>Pass</td>
</tr>
<tr>
<td>16</td>
<td>HCP –2 kV</td>
<td>Pass</td>
</tr>
<tr>
<td>17</td>
<td>HCP 4 kV</td>
<td>Pass</td>
</tr>
<tr>
<td>18</td>
<td>HCP –4 kV</td>
<td>Pass</td>
</tr>
<tr>
<td>22</td>
<td>HCP –4 kV</td>
<td>Pass</td>
</tr>
</tbody>
</table>
7.4.2 EFT: IEC61000 – 4-4

7.4.2.1 Test Level and Expected Performance

The EFT burst at I/O connectors and the performance criteria expected are as follows:

Table 13. EFT Test Levels and Performance Criteria

<table>
<thead>
<tr>
<th>GENERIC TEST STANDARD</th>
<th>TEST LEVEL</th>
<th>PERFORMANCE (PASS) CRITERIA</th>
</tr>
</thead>
<tbody>
<tr>
<td>EFT/B IEC 61000-4-4</td>
<td>±2 kV at 5 kHz, 100 kHz on signal ports</td>
<td>Criteria A</td>
</tr>
</tbody>
</table>

7.4.2.2 Setup Description

The burst signal is injected on all cables together using a capacitive coupling clamp. EUT is connected to auxiliary sources by unshielded cables. The lengths of the cables are set to 3 m and cables are placed 10 cm above the reference plane. The test is carried out with the EUT placed 10 cm above the reference plane on insulating material, and with the EUT placed on the reference plane.

Figure 26. EFT Test Setup
7.4.2.3 Monitoring Methods

1. Connect the EUT as shown in Figure 26. The shield pin is connected to protective earth same as the EFT generator.
2. Power on the EUT. EUT software is configured to generate an output of 4 mA and 20 mA alternately for two seconds each.

The AO channel is checked before and after the test. The EFT test is performed as per test levels mentioned in Table 14.

7.4.2.4 Results

<table>
<thead>
<tr>
<th>TEST NO.</th>
<th>TEST MODE</th>
<th>OBSERVATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0.5 kV, 5 kHz</td>
<td>Pass</td>
</tr>
<tr>
<td>2</td>
<td>−0.5 kV, 5 kHz</td>
<td>Pass</td>
</tr>
<tr>
<td>3</td>
<td>1 kV, 5 kHz</td>
<td>Pass</td>
</tr>
<tr>
<td>4</td>
<td>−1 kV, 5 kHz</td>
<td>Pass</td>
</tr>
<tr>
<td>5</td>
<td>1.5 kV, 5 kHz</td>
<td>Pass</td>
</tr>
<tr>
<td>6</td>
<td>−1.5 kV, 5 kHz</td>
<td>Pass</td>
</tr>
<tr>
<td>7</td>
<td>2 kV, 5 kHz</td>
<td>Pass</td>
</tr>
<tr>
<td>8</td>
<td>−2 kV, 5 kHz</td>
<td>Pass</td>
</tr>
<tr>
<td>9</td>
<td>0.5 kV, 100 kHz</td>
<td>Pass</td>
</tr>
<tr>
<td>10</td>
<td>−0.5 kV, 100 kHz</td>
<td>Pass</td>
</tr>
<tr>
<td>11</td>
<td>1 kV, 100 kHz</td>
<td>Pass</td>
</tr>
<tr>
<td>12</td>
<td>−1 kV, 100 kHz</td>
<td>Pass</td>
</tr>
<tr>
<td>13</td>
<td>1.5 kV, 100 kHz</td>
<td>Pass</td>
</tr>
<tr>
<td>14</td>
<td>−1.5 kV, 100 kHz</td>
<td>Pass</td>
</tr>
<tr>
<td>15</td>
<td>2 kV, 100 kHz</td>
<td>Pass</td>
</tr>
<tr>
<td>16</td>
<td>−2 kV, 100 kHz</td>
<td>Pass</td>
</tr>
</tbody>
</table>
7.4.3 Surge: IEC61000-4-5

7.4.3.1 Test Level and Expected Performance

The common-mode surge at I/O connectors and the performance criteria expected are as follows:

<table>
<thead>
<tr>
<th>GENERIC TEST STANDARD</th>
<th>TEST LEVEL</th>
<th>PERFORMANCE (PASS) CRITERIA</th>
</tr>
</thead>
<tbody>
<tr>
<td>Surge IEC 61000-4-5</td>
<td>±1 kV CM on signal ports</td>
<td>Criteria B</td>
</tr>
</tbody>
</table>

7.4.3.2 Setup Description

The EUT and AO cable were placed on nonconductive support 10 cm above a reference ground plane. Surge was injected into the AO cable (I/O cable) for testing through a coupling-decoupling network. The EUT operation was monitored before and after the test.
7.4.3.3 Monitoring Methods

1. Connect the EUT as shown in Figure 27. The shield pin is connected to protective earth same as the surge generator.

2. Power on the EUT. EUT software is configure to generate an output of 4 mA and 20 mA alternately for two seconds each.

The AO channel is checked before and after the test. The surge test is performed as per test levels mentioned in Table 16.

7.4.3.4 Results

Table 16. Surge Test Results

<table>
<thead>
<tr>
<th>TEST NO.</th>
<th>TEST MODE</th>
<th>OBSERVATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0.5 kV</td>
<td>Pass</td>
</tr>
<tr>
<td>2</td>
<td>–0.5 kV</td>
<td>Pass</td>
</tr>
<tr>
<td>3</td>
<td>1 kV</td>
<td>Pass</td>
</tr>
<tr>
<td>4</td>
<td>–1 kV</td>
<td>Pass</td>
</tr>
</tbody>
</table>
8 References

1. Texas Instruments, *AN2292 Designing an Isolated Buck (Flybuck) Converter*, Application Note (SNVA674)
2. Texas Instruments, *AN2040 Output Voltage Clamping Using the LM5069 Hot Swap Controller*, Application Note (SNVA430)
5. Texas Instruments, *TPS61170 Design Software for Control Loop Design*, TPS61170 Design Software (ZIP)
7. Texas Instruments, *TPS61170 1.2-A High-Voltage Boost Converter in 2-mm x 2-mm² QFN Package*, Datasheet (SLVS789)
8. Texas Instruments, *TPS61170 Calculation Spreadsheet* (SLVC160)

9 Terminology

**Differential Nonlinearity (DNL) and Integral Nonlinearity (INL)**

DNL is the deviation between two analog values corresponding to adjacent input digital values. Ideally, any two adjacent digital codes correspond to output analog voltages that are exactly one LSB apart. Any deviation from the ideal step width (LSB) is the DNL. DNL errors accumulate to produce a total INL.

DNL and INL values are usually specified using one of the following units: LSB or %FSV.

**Total Unadjusted Error (TUE)**

TUE is measurement error without any gain or offset error compensations. TUE gives an exact measure of the system level inaccuracies. With the right choice of components and proper PCB layout, the need for factory calibration may be avoided, which can save time and costs during mass production.

\[
TUE = \sqrt{(Offset Error)^2 + (Gain Error)^2 + (DNL)^2 + (INL)^2}
\]

(30)
10  Design Files

10.1  Schematics
To download the most recent schematics, see the design files at TIDA-00231.

10.2  Bill of Materials
To download the most recent bill of materials (BOM), see the design files at TIDA-00231.

10.3  PCB Layout Recommendations
The AO module is implemented in a four-layer PCB. For optimal performance of this design, standard PCB layout guidelines were followed, including proper decoupling close to all integrated circuits and adequate power and ground connections with large copper pours. Additional considerations were made for providing robust EMC/EMI immunity. All protection elements were placed as close as possible to the output connector to provide a controlled return path for transient currents. To allow optimum current flow, wide, low-impedance, low-inductance traces were used along the output signal path and protection elements. Wherever possible, copper pours were used in place of traces. Stitching the planes provides an effective return path around the PCB and helps reduce the impact of radiated emissions.

To achieve high performance, follow these layout guidelines:
1. Route all signals, assuming there is a split ground plane for analog and digital. Furthermore, it is better to split the ground initially during the layout. Route all analog and digital traces so that the traces see the respective ground all along the second layer. Then, short both grounds to form a common ground plane.
2. Return the DAC ground pins to the ground plane through multiple vias (PTH).
3. Ensure that protection elements such as TVS diodes, capacitors are placed as close as possible to the connectors to ensure that return current from high-energy transients does not damage sensitive devices. Further, use large and wide traces to ensure a low-impedance path for high-energy transients.
4. Place the decoupling capacitors close to the supply pin of respective IC pins.
5. Use multiple vias for power and ground for decoupling caps.
6. Route the current sense resistor as a Kelvin sense connection.
7. For signal integrity in SPI lines, place the termination resistors near to the source.
8. Each AVDD/AVSS should have decoupling capacitors placed close to the respective pins.
9. Place the reference capacitor close to the voltage reference input pin.
10. Connect the thermal PAD of DAC8760 to the lowest potential in the system. In this design, it is connected to ground potential.
Isolation Barrier

TPS61170 datasheet recommended placement guidelines are followed for this design

Wide protective Earth plane: Provides low-impedence path to divert high-energy transients away from I/O terminals through TVS diode and Y-CAP

DAC thermal pad is connected to GND to enhance thermal performance

TVS protection diodes placed close to board connector

**Figure 28. PCB Layout Guidelines**

10.3.1 **Layer Plots**

To download the most recent layer plots, see the design files at TIDA-00231.

**NOTE:** All artwork is viewed from the top side.

10.4 **Altium Project**

To download the most recent Altium project files, see the design files at TIDA-00231.

10.5 **Gerber Files**

To download the most recent Gerber files, see the design files at TIDA-00231.

10.6 **Assembly Drawings**

To download the most recent assembly drawings, see the design files at TIDA-00231.

10.7 **Software Files**

To download the most recent software files, see the design files at TIDA-00231.
About the Author

AMOL GADKARI is a systems engineer at Texas Instruments India where he is responsible for developing reference design solutions for the industrial segment. Amol has eight years of experience in mixed signal board design, analog circuit designs, and EMC-protection circuit design. He can be reached at a-gadkari@ti.com.
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