Design Considerations
TIDA-00389 Automotive ADAS Power Design
Optimized for Xilinx® Zynq® 7010 SoC

Power Supplies

- This design consists of six power rails to power the Xilinx® Zynq® 7010 SoC, a boost converter for powering the CAN transceiver, and a DDR termination regulator. This design uses a combination of a multi-rail IC along with LDOs, and a boost to generate these rails.

- All power supplies are designed to operate above the AM band with switching frequencies >2MHz from a single +3.3V or +5V input voltage.

- The estimated power dissipation of the LDO's used is shown below:

	Power (W) at VIN = 3.3V	Power (W) at VIN = 5V
VCCAUX	0.317	0.672
VCCO_1.8V	0.188	0.4
VCCO_2.5V	0.123	0.385

- Common output voltages were combined to minimize the number of regulators for this design. Additional filtering may be required depending on application.

- Jumper J8 is provided to disable the boost converter in the case the input voltage is 5V.

- All passives selected operate under automotive grade temperatures.

- 1% tolerance resistors are chosen to set all the FB resistive dividers for better accuracy.

- All ceramic capacitors are chosen to have a voltage rating >2x the maximum input voltage applied to avoid DC bias effects.

Layout

- Use short, wide traces between the power components and for power connections to the DC-DC converter circuits.

- Route noise sensitive traces, such as the voltage feedback path, away from noisy traces between the power components.

- The path between the input capacitors and the IC must be minimized.

- The voltage feedback trace must remain close to the buck circuit.

Power Sequencing

The LM3880 power sequencer was used to provide power up and down sequencing for all of the Xilinx® Zynq® 7010 PS and PL power supply rails. For reference, the sequencing requirements from the Xilinx® Zynq® 7010 datasheet are shown below:

PS Power-On/Off Power Supply Sequencing

The recommended power-on sequence is VCCPINT, VCCPAUX, and VCCPLL together, then the PS VCCO supplies (VCCO_MIO0, VCCO_MIO1, and VCCO_DDR) to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If VCCPAUX, VCCPLL, and the PS VCCO supplies (VCCO_MIO0, VCCO_MIO1, and VCCO_DDR) have the same recommended voltage levels, then they can be powered by the same supply and ramped simultaneously. Xilinx recommends powering VCCPLL with the same supply as VCCPAUX, with an optional ferrite bead filter.

For VCCO_MIO0 and VCCO_MIO1 voltages of 3.3V:

• The voltage difference between VCCO_MIO0 /VCCO_MIO1 and VCCPAUX must not exceed 2.625V for longer than
TVCCO2VCCAUX for each power-on/off cycle to maintain device reliability levels.
• The TVCCO2VCCAUX time can be allocated in any percentage between the power-on and power-off ramps.

PL Power-On/Off Power Supply Sequencing

The recommended power-on sequence for the PL is VCCINT, VCCBRAM, VCCAUX, and VCCO to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If VCCINT and VCCBRAM have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously. If VCCAUX and VCCO have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously.

For VCCO voltages of 3.3V in HR I/O banks and configuration bank 0:

• The voltage difference between VCCO and VCCAUX must not exceed 2.625V for longer than TVCCO2VCCAUX for each
power-on/off cycle to maintain device reliability levels.
• The TVCCO2VCCAUX time can be allocated in any percentage between the power-on and power-off ramps.

PS—PL Power Sequencing

The PS and PL power supplies are fully independent. PS power supplies (VCCPINT, VCCPAUX, VCCPLL, VCCO_DDR, V_{CCO_MIO0}, and V_{CCO_MIO1}) can be powered before or after any PL power supplies. The PS and PL power regions are isolated to prevent damage.

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