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1) Power Tree Block Diagram

USB 5V power

5V VCC pins in Two GPIO Headers

2-pin Power Header
Input Power Range: 3.6V - 5.7V

5V

LDO LP5900SD-2.5
Up to 150mA

2.5V

LDO LP38500SD-ADJ
Up to 1.5A

3.3V

LDO LP38500SD-ADJ
Up to 1.5A

1.2V

EP4CE22 VCCINT

SDRAM VDD, VDDQ
MAX II EPM240 VCCINT, VCCID
EP4CE22 VCCIO

GPIO 3.3V power
EP2C8T144I8, 24LC256B, ADXL345

24LC256B

RT2438BL VCC(5V)

5V

GPIO 5V power

R90x757
2) Board Photos

Top View

- USB Type mini-AB Port
- 2Kb 12C EEPROM
- 4 Dip Switches
- 2-pin External Power Header
- Digital Accelerometer
- 50Mhz Clock Oscillator
- FPGA Serial Configuration Device (EPCS)
- 8 Green LEDs
- 32 MB SDRAM
- 40-pin GPIO Header
- 2 Push-buttons
- Altera Cyclone IV EP4CE22F17C8N FPGA
- 26-pin Header
- A/D Converter
- 40-pin GPIO Header
DE0-Nano Power-up Sequence

3) Power-up Sequence
4) Output Voltage Ripple

The images below shows the output voltage ripple when load is fully applied.

LP38500SD-ADJ: VIN = 3.3V, VOUT = 1.2V, IOUT = 0.9A Output Ripple Voltage
LP38500SD-ADJ: VIN = 5V, VOUT = 3.3V, IOUT = 1.35A Output Ripple Voltage
5) Load Regulation

The images below show the output load regulation. The input voltages are 3.3V and 5V for 1.2V and 3.3V outputs, respectively.
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