

Design Considerations

TIDA-00390 Automotive ADAS Power Design Optimized for Xilinx Zynq 7020 SoC

Power Supplies

- This design consists of five power rails to power the Xilinx Zynq 7020 SoC, a boost converter for powering the CAN transceiver, and a DDR termination regulator. This design uses discrete ICs along with LDOs, and a boost to generate these rails.
- All power supplies are designed to operate above the AM band with switching frequencies >2MHz from a single +3.3V or +5V input voltage.
- The estimated power dissipation of the LDO's used is shown below:

	Power (W) at VIN = 3.3V	Power (W) at VIN = 5V
VCCO_1.8V	0.071	0.150
VCCO_2.5V	0.182	0.567

- Common output voltages were combined to minimize the number of regulators for this design. Additional filtering may be required depending on application.
- Jumper J8 is provided to disable the boost converter in the case the input voltage is 5V.
- All passives selected operate under automotive grade temperatures.
- 1% tolerance resistors are chosen to set all the FB resistive dividers for better accuracy.
- All ceramic capacitors are chosen to have a voltage rating >2x the maximum input voltage applied to avoid DC bias effects.

Layout

- Use short, wide traces between the power components and for power connections to the DC-DC converter circuits.
- Route noise sensitive traces, such as the voltage feedback path, away from noisy traces between the power components.
- The path between the input capacitors and the IC must be minimized.
- The voltage feedback trace must remain close to the buck circuit.

Power Sequencing

The LM3880 power sequencer was used to provide power up and down sequencing for all of the Xilinx® Zynq® 7020 PS and PL power supply rails. For reference, the sequencing requirements from the Xilinx® Zynq® 7020 datasheet are shown below:

PS Power-On/Off Power Supply Sequencing

The recommended power-on sequence is VCCPINT, VCCPAUX, and VCCPLL together, then the PS VCCO supplies (VCCO_MIO0, VCCO_MIO1, and VCCO_DDR) to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If VCCPAUX, VCCPLL, and the PS VCCO supplies (VCCO_MIO0, VCCO_MIO1, and VCCO_DDR) have the same recommended voltage levels, then they can be powered by the same supply and ramped simultaneously. Xilinx recommends powering VCCPLL with the same supply as VCCPAUX, with an optional ferrite bead filter.

For VCCO_MIO0 and VCCO_MIO1 voltages of 3.3V:

- The voltage difference between VCCO_MIO0 /VCCO_MIO1 and VCCPAUX must not exceed 2.625V for longer than TVCCO2VCCAUX for each power-on/off cycle to maintain device reliability levels.
- The TVCCO2VCCAUX time can be allocated in any percentage between the power-on and power-off ramps.

PL Power-On/Off Power Supply Sequencing

The recommended power-on sequence for the PL is VCCINT, VCCBRAM, VCCAUX, and VCCO to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If VCCINT and VCCBRAM have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously. If VCCAUX and VCCO have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously.

For VCCO voltages of 3.3V in HR I/O banks and configuration bank 0:

- The voltage difference between VCCO and VCCAUX must not exceed 2.625V for longer than TVCCO2VCCAUX for each power-on/off cycle to maintain device reliability levels.
- The TVCCO2VCCAUX time can be allocated in any percentage between the power-on and power-off ramps.

PS—PL Power Sequencing

The PS and PL power supplies are fully independent. PS power supplies (VCCPINT, VCCPAUX, VCCPLL, VCCO_DDR, VCCO_MIO0, and VCCO_MIO1) can be powered before or after any PL power supplies. The PS and PL power regions are isolated to prevent damage.

IMPORTANT NOTICE FOR TI REFERENCE DESIGNS

Texas Instruments Incorporated ("TI") reference designs are solely intended to assist designers ("Buyers") who are developing systems that incorporate TI semiconductor products (also referred to herein as "components"). Buyer understands and agrees that Buyer remains responsible for using its independent analysis, evaluation and judgment in designing Buyer's systems and products.

TI reference designs have been created using standard laboratory conditions and engineering practices. **TI has not conducted any testing other than that specifically described in the published documentation for a particular reference design.** TI may make corrections, enhancements, improvements and other changes to its reference designs.

Buyers are authorized to use TI reference designs with the TI component(s) identified in each particular reference design and to modify the reference design in the development of their end products. HOWEVER, NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY THIRD PARTY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT, IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI REFERENCE DESIGNS ARE PROVIDED "AS IS". TI MAKES NO WARRANTIES OR REPRESENTATIONS WITH REGARD TO THE REFERENCE DESIGNS OR USE OF THE REFERENCE DESIGNS, EXPRESS, IMPLIED OR STATUTORY, INCLUDING ACCURACY OR COMPLETENESS. TI DISCLAIMS ANY WARRANTY OF TITLE AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, QUIET ENJOYMENT, QUIET POSSESSION, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS WITH REGARD TO TI REFERENCE DESIGNS OR USE THEREOF. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY BUYERS AGAINST ANY THIRD PARTY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON A COMBINATION OF COMPONENTS PROVIDED IN A TI REFERENCE DESIGN. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, SPECIAL, INCIDENTAL, CONSEQUENTIAL OR INDIRECT DAMAGES, HOWEVER CAUSED, ON ANY THEORY OF LIABILITY AND WHETHER OR NOT TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES, ARISING IN ANY WAY OUT OF TI REFERENCE DESIGNS OR BUYER'S USE OF TI REFERENCE DESIGNS.

TI reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques for TI components are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

Reproduction of significant portions of TI information in TI data books, data sheets or reference designs is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards that anticipate dangerous failures, monitor failures and their consequences, lessen the likelihood of dangerous failures and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in Buyer's safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed an agreement specifically governing such use.

Only those TI components that TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components that have **not** been so designated is solely at Buyer's risk, and Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.