

# TI Designs: High Speed Synchronizing Multiple JESD204B Analog to Digital Converters for Emitter Position Location



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## Circuit Description

A common technique to estimate the position of emitters uses the amplitude and phase shift data of a signal derived from an array of spatially distributed sensors [1]. For such systems, it is important to guarantee a deterministic phase relationship between the sensors to minimize errors in the actual measured data. This application design will discuss how multiple Analog to Digital Converters (ADCs) with a JESD204B interface can be synchronized so that the sampled data from the ADCs are phase aligned. The synchronization concepts will be demonstrated with two Giga-sample ADCs (ADC12J4000 in bypass mode) sampling at 3.072 GSPS but the concepts can be expanded to more than two ADCs.

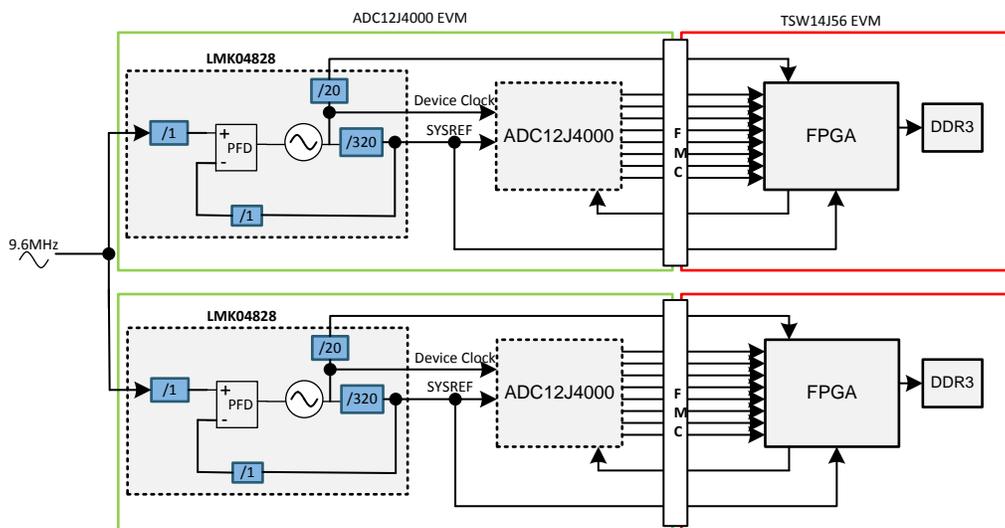
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[LMK04828](#)  
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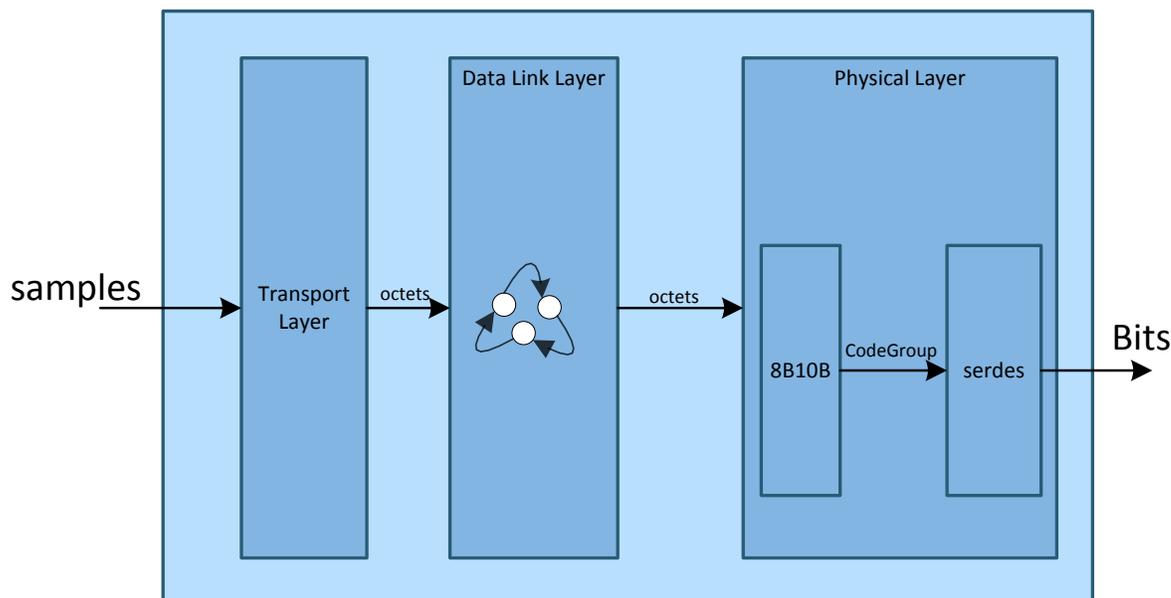


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## 1 JESD204B Interface

As the throughput of data converters increase because of increasing channel count and sample rates, conventional LVDS and CMOS interface technologies become inefficient to deliver (or receive) the payload data to digital signal processors (FPGA or ASIC). The inefficiencies exist in the power consumption and board area used by LVDS or CMOS interfaces. A JESD204B interface solves this by using multi-gigabit transceiver technology to interface between a data converter and an FPGA or ASIC [2].



**Figure 1: Simplified JESD204B Interface**

Figure 1 shows the various blocks of a simplified JESD204B interface between an ADC and FPGA. The various layers that make up the interface include transport layer, data link layer and physical layer. The sampled and digitized data from the ADC is first converted into groups of 8 bits (or octets) inside the transport layer. The data link layer inserts special characters in the stream of octets from the transport layer under special conditions and rules [2]. Inside the physical layer, octets from the data link layer are encoded into 10 bits (or code groups) and serialized for transmission to FPGA/ASIC. After receiving the transmitted bit stream, all the above sequences are reversed in the FPGA/ASIC to extract the samples from the transmitted bit stream.

### 1.1 Theory of Synchronization Across a JESD204B link

A major advantage of JESD204B that also simplifies the synchronization of multiple devices is the requirement that all clocks must be generated internally from a common external reference (or device clock). This is illustrated in Figure 2. Consequently, two main requirements need to be met to successfully synchronize multiple JESD204B devices:

- 1) Provide a common device clock to all the data converters and FPGAs. This is critical since all other clocks-sampling clock, frame clock, character clock, bit clock- are generated from this common source. Also ensure that the distribution of the device clock to all devices is well matched to guarantee a deterministic phase relationship.
- 2) Provide a synchronized timing reference to all the devices. This timing reference is used to align the phase of the clock dividers and multipliers used to generate all of the internal clocks. This timing reference can be provided through the sysref input (in subclass 1 devices) or through the sync input (in subclass 2 devices)

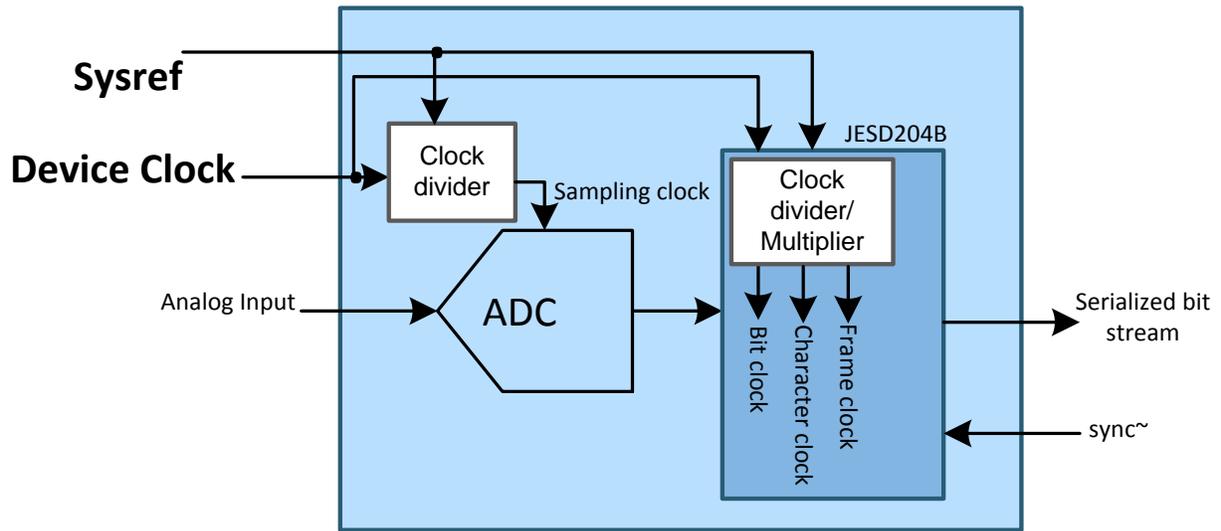
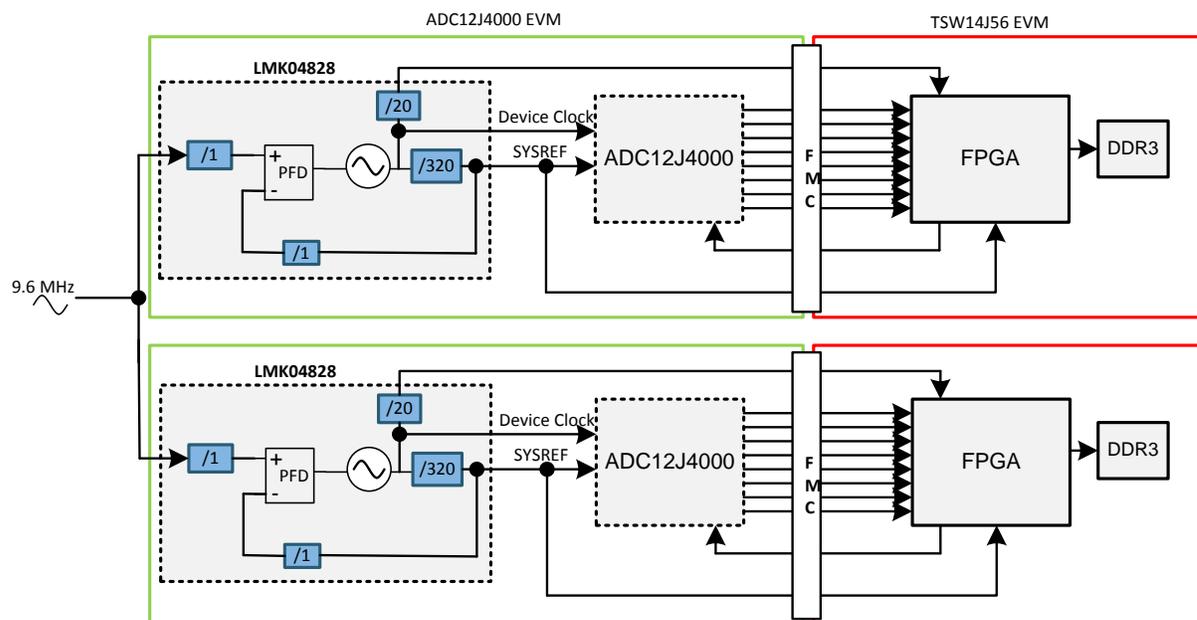


Figure 2: Clock generation in a JESD204B device

## 2 How to synchronize multiple ADCs across JESD204B link

Two ADC12J4000 and two TSW14J56 will be synchronized to illustrate the JESD204B synchronization concepts. The ADC12J4000 is a Giga-sampling ADC (capable of sample rates up to 4 GSPS) with a JESD204B subclass 1 interface. The TSW14J56 is an FPGA-based data capture and pattern generation board with a JESD204B interface. A block diagram of the setup is shown in Figure 3. Data from each ADC12J4000 will be captured and stored in external DDR3 memory on the TSW14J56 EVM. A software generated trigger will be used to align the start of data capture by the two TSW14J56 EVMs.



**Figure 3: Block diagram of synchronized 2x ADC12J4000 and 2x TSW14J56**

### 2.1 Synchronized device clock and sysref generation

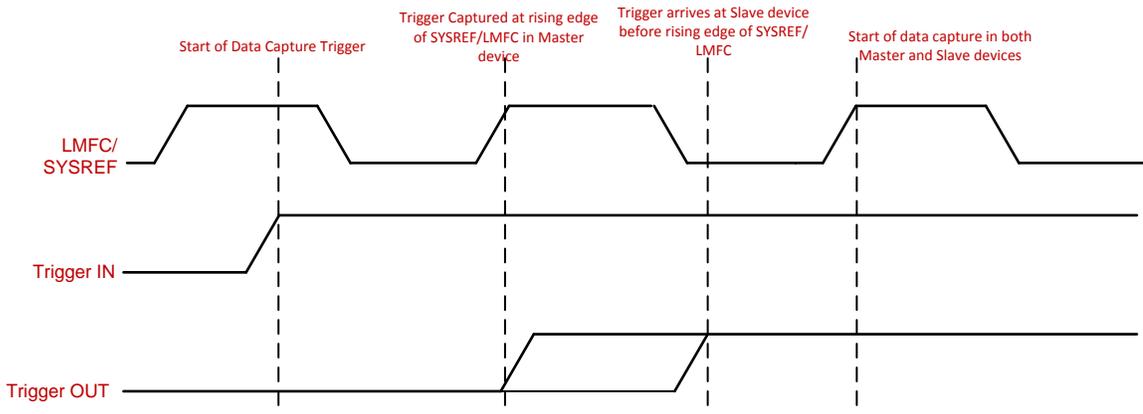
Each ADC12J4000 EVM has an LMK04828 clock chip that is used to provide source synchronous device clock and SYSREF to the ADCs and FPGAs as shown in Figure 3. In order to phase align the device clock and SYSREF going to each ADC12J4000 and TSW14J56, the LMK04828 clock outputs are phased locked (using the 2nd PLL of LMK04828) to a common 9.6 MHz reference as illustrated in Figure 3.

### 2.2 Synchronizing data capture into external DDR3 memory

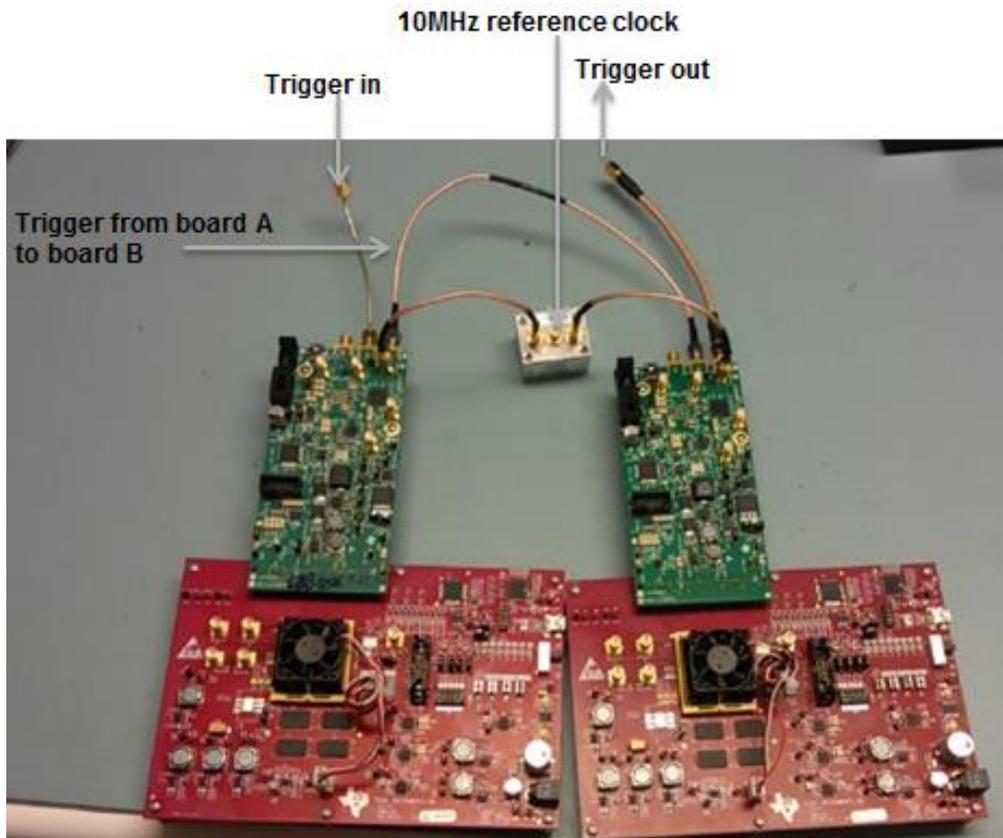
An important aspect of the setup is the ability to synchronize the capture of data from each ADC into the external DDR3 memory on each TSW14J56 EVM. This is achieved by aligning the start of data capture into the external memory to an external trigger signal. As shown in Figure 4, an external trigger (or software generated trigger) is provided to the Master TSW14J56 and it is sampled at the rising edge of the SYREF clock (or Local Multi-Frame Clock) to generate a "Trigger Out" signal. This "Trigger Out" signal is subsequently routed internally in the Master device and externally to each of the connected slave devices to enable data capture. The start of data capture into the DDR3 memory (in both master and slave devices) occurs at a SYREF/LMFC rising edge when the "Trigger OUT" signal is high.

**NOTE:**

Because there are not enough SMA connectors on the TSW14J56 EVM (revision B), the SMA connectors (TMST+ and TMST-) on the ADC12J4000 EVM are used to daisy chain the trigger signal from the master TSW14J56 EVM to the slave TSW14J56 EVM. To enable the trigger signal to get to the FPGA, install R18 and R21 on the ADC12J4000 EVM. For this setup, the ADC12J4000 is configured to use single-ended sync instead of differential sync.



**Figure 4: Trigger generation timing diagram**



**Figure 5: Setup of ADC12J4000 EVM and TSW14J56 EVM**

### 3 Setup

The following steps outline how to successfully setup and synchronize two ADC12J4000 EVMs and two TSW14J56 EVMs. The ADC12J4000 will be configured in bypass mode and at a sample rate of 3.072 GSPS (sample clock is sourced from LMK04828 clock chip).

#### 3.1 Required ADC12J4000 EVM Modifications

The default configuration of the ADC12J4000 EVM must be modified as follows:

- a) Install R18 and R21 on the ADC12J4000 EVM. This will be used to propagate the trigger signal from the maser to the slave EVM
- b) To enable the 9.6 MHz reference clock to the OSCIN\* input pin of the LMK04828, install C85 and C86
- c) Install capacitors to enable the ADC DEVCLK+ and ADC DEVCLK- nets from the LMK04828 to be used as the sampling clock to the ADC12J4000. Remove C32 and C33

For all component locations, refer to ADC12J4000 EVM schematic [3]

#### 3.2 Required Software

The following software interfaces are required to control the setup:

- a) Synchronization: This software interface is shown in figure 6 and is the main user interface that is used to control the setup. It can be used to perform the following functions:

- a. Create a communication channel between PC and TSW14J56 EVMs. 

- b. Download firmware to TSW14J56 EVMs 

- c. Load firmware configuration settings to the TSW14J56 EVMs 

- d. Read and display captured data from DDR3 memory of TSW14J56 EVMs 

- e. Save captured data in .csv file format 

- f. Plot eye diagram of the captured data 

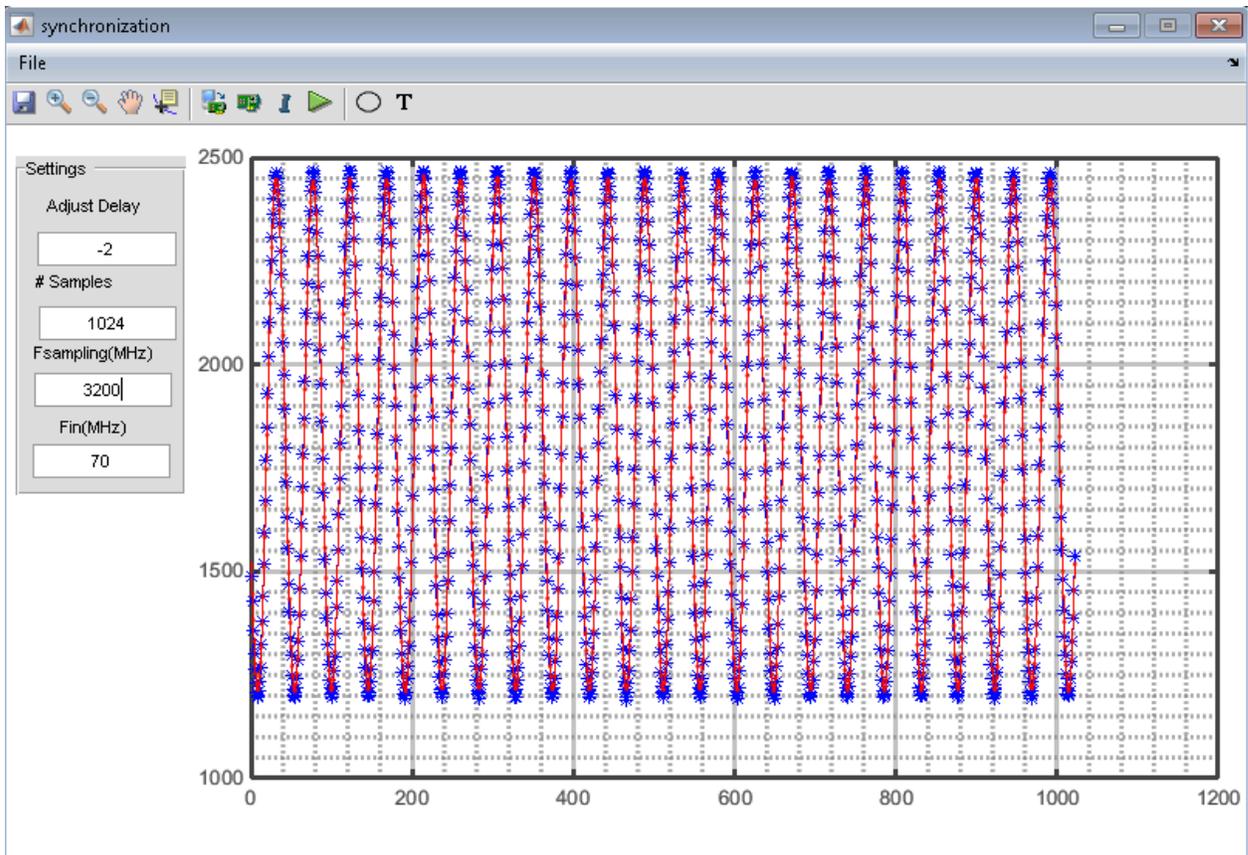
- b) ADC12J4000 EVM GUI

This is used to configure the ADC12J4000 and can be downloaded from Texas Instruments website together with a user's guide

- c) High Speed Data Converter PRO software (HSDC-PRO)

It is important to install HSDC-PRO software so that the relevant FTDI USB drivers required by the main user interface for controlling the setup (synchronization.exe) will be installed on the PC.

The HSDC-PRO software is also recommended for frequency domain analysis of the captured data. The time domain samples of the captured data from the ADC12J4000 can be saved in a .csv file format and imported to HSDC-PRO software for frequency domain analysis. More information on importing data into HSDC-PRO is available in [4].



**Figure 6: Main user Interface to control ADC12J4000 and TSW14J56 synchronization**

### 3.3 Setup Procedure

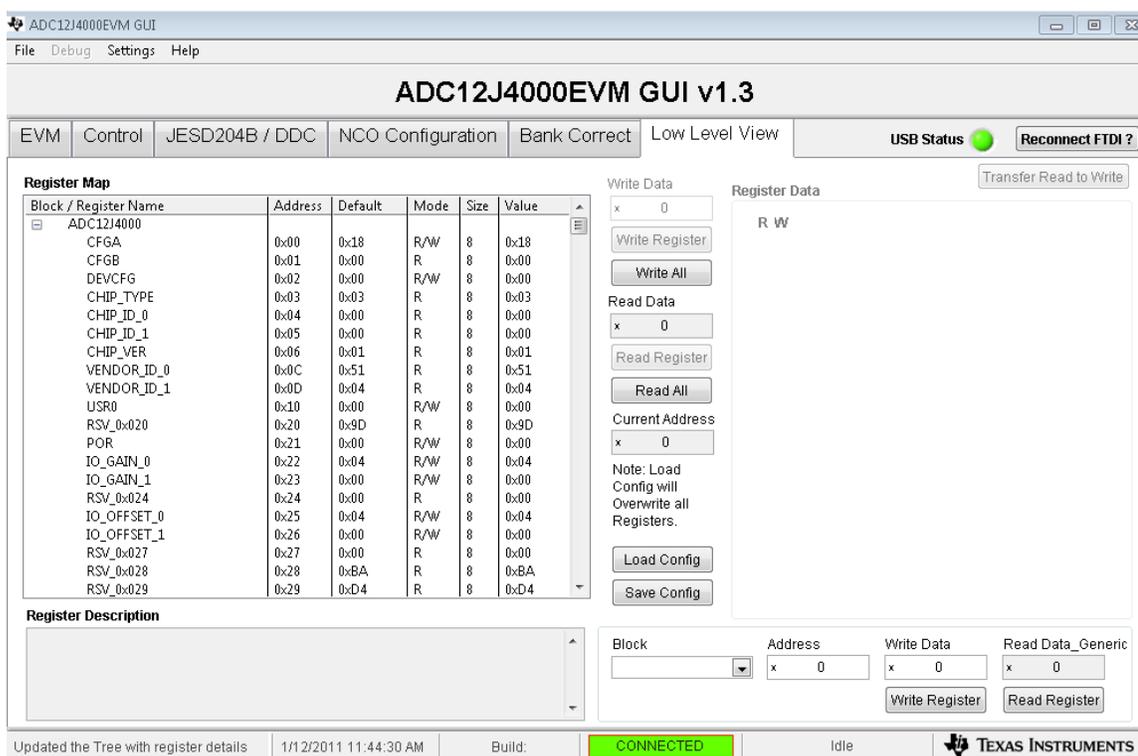
- 1) Connect the ADC12J4000 EVMs (REVB and up) and TSW14J56 EVMs together as shown in Figure 5
- 2) Provide 9.6 MHz reference clock to SMA connector 'LMKCLK' on each ADC12J4000 EVM as shown in Figure 5. Note: The LMK04828 on-chip PLL is configured to multiply the reference clock by 320 to generate the device clock (3.072 GHz) to ADC12J4000.
- 3) Connect an SMA cable between the two ADC12J4000 EVMs from the SMA connector TMST+ of the master to the SMA connector TMST- of the slave device. Note: Either of the EVMs can be designated as the Master. Note the serial number of the TSW14J56 EVM selected as the master.
- 4) Plug 5V power supply into the ADC12J4000 and TSW14J56 and power on the EVMs
- 5) Connect 2 USB cables to PC and to each of the TSW14J56 EVMs
- 6) Connect one USB cable to either of the ADC12J4000 EVMs and configure the EVM as follows;
  - a) Start the ADC12J4000 EVM Software programming interface. Once started ensure that the USB status LED on the GUI front panel is lit green. Click on the Reconnect FTDI button repeatedly if this LED is unlit. Refer to the ADC12J4000 EVM Users Guide on how to troubleshoot USB connectivity issues
  - b) Click on the Low Level View Tab, Load Config button and browse to the configuration file *ADC12J4000\_bypass\_SE\_SYNC.cfg*. Load this file. This file sets up the ADC12J4000 in bypass mode with single ended SYNC and K=8.

- c) Click on the Low Level View Tab, Load Config button and browse to the configuration file *LMK04828\_PLL2\_0delay\_FBMUX\_SYSREF.cfg*. Load this file. This file sets up the LMK04828 to use PLL2 in 0-delay mode with the feedback path through the SYSREF divider. Refer to figure 3 for PLL2 divider settings.

**NOTE:**

**After loading this configuration file, LED Status2 on the ADC12J4000 EVM must be lit green to indicate that PLL2 is locked to the 9.6 MHz reference clock provided in step 2**

- 7) Disconnect the USB cable from the ADC12J4000 EVM that was connected previously in step 6 and connect to the other ADC12J4000 EVM. Repeat step 6 to configure this ADC and the LMK04828 clock chip. Again, look for green LED **Status2** to light up after successfully configuring this EVM



**Figure 7: User Interface for ADC12J4000 showing the low level page**

- 8) Double click on the executable *synchronization.exe* to start the graphic user interface to control the setup. This user interface is shown in Figure 6. To use the user interface;

- a) Click on the connect  icon to open a communication channel between the PC and the TSW14J56 EVMs.

**NOTE:**

**A pop up menu lists the serial numbers of all connected TSW14J56 EVMs and allows the user to select the serial number of the Master TSW14J56 EVM.**

- b) Click on the Push Firmware  icon to load the firmware image. If Firmware has already been downloaded in a previous step, then there is no need to download again.

**NOTE:**

After successful firmware download to TSW14J56 EVM, LEDs D2 and D4 should BLINK, LED D8 should be ON and LEDs D6 and D7 should be OFF. Re-download firmware if the status of any of the LEDs mentioned above on the TSW14J56 EVM is different.

- c) Click on the Initialize  icon to load firmware configuration settings.

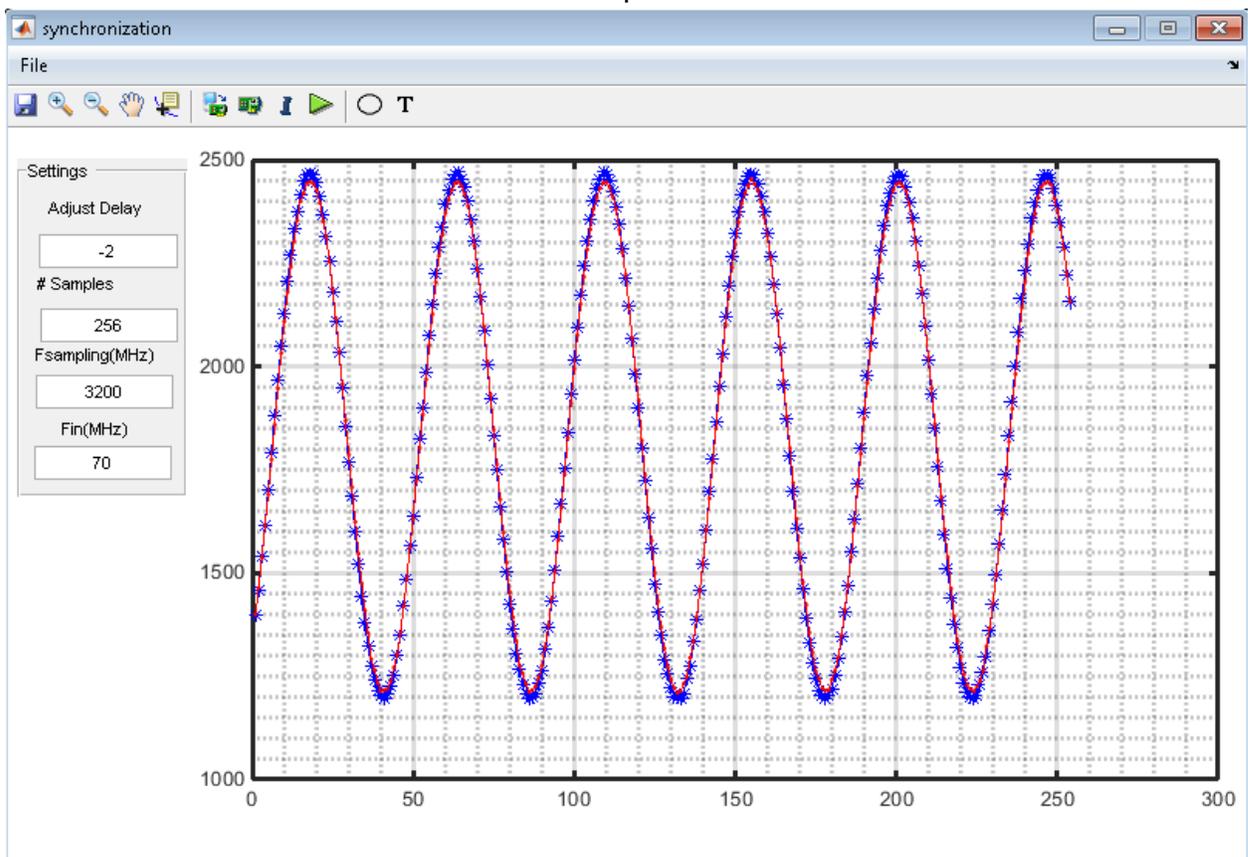
**NOTE:**

After successful initialization, LED D3 on both TSW14J56 EVMs must turn OFF.

- d) Click on the Get Data  icon to initiate a software trigger from the master EVM to slave EVM and to read data captured into DDR3 memory back to PC.

#### 4 Results

Figure 8 shows 6 cycles of a 70 MHz sinusoid sampled at 3.072 GSPS by both ADC12J4000 EVMs. Note that samples from the slave (red plot) had to be delayed by 2 samples relative to the master (blue plot). This initial delay adjustment may vary from setup to setup but is fixed for any particular setup.



**Figure 8: Time-Domain output of synchronized ADC12J4000 showing six cycles of 70 MHz sinusoid**

To estimate the amount of phase variation between the two synchronized ADCs, one-half cycle of the sinusoid from each ADC12J4000 is overlaid on top of each other to obtain the eye diagram shown in figure 9. The eye diagram shows the cumulative effect of sampling clock jitter, aperture delay and analog path delay on the data sampled by each of the ADCs. This eye diagram is displayed by clicking on the icon



From figure 9, the maximum possible phase variation between the two ADCs can be estimated as 80% of one sampling clock period or 250 ps.

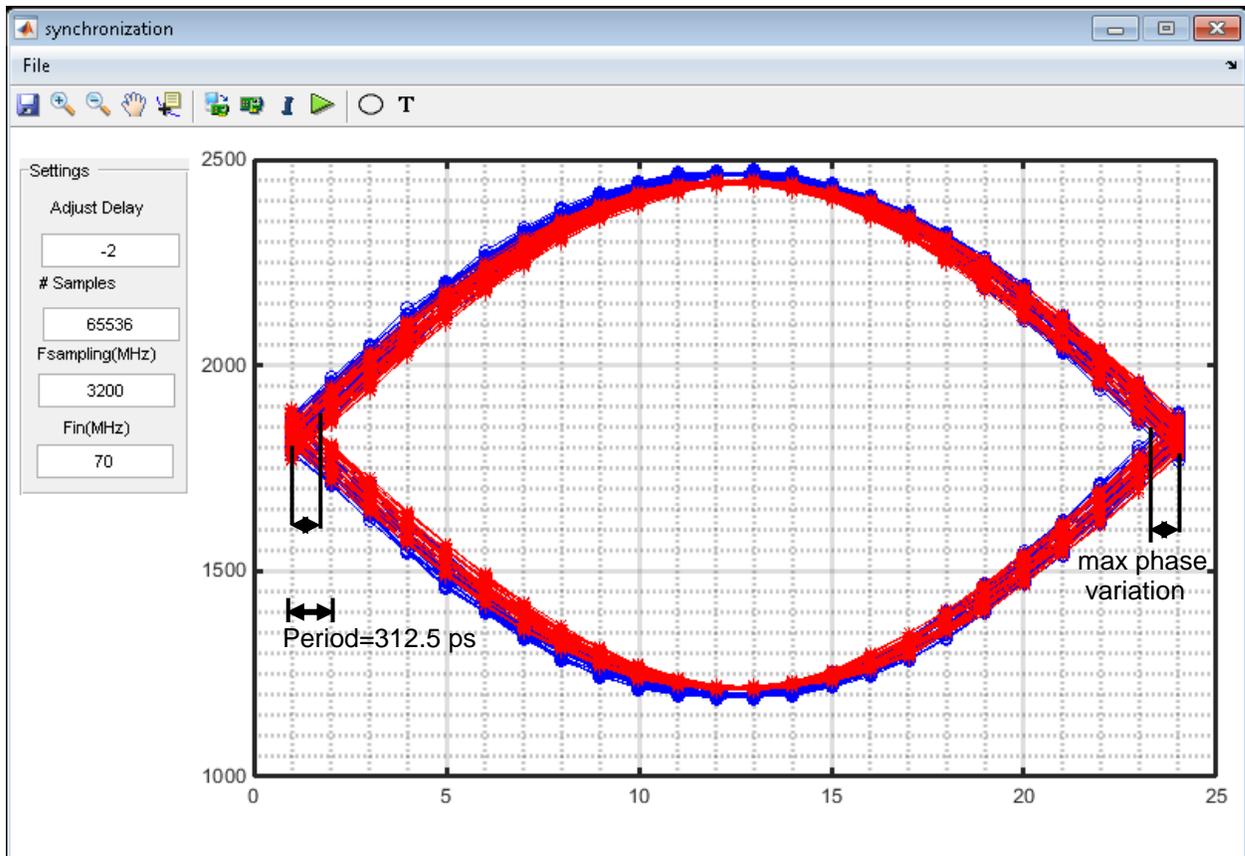


Figure 9: Eye diagram output of synchronized ADC12J4000 showing 1434 cycles of 70 MHz sinusoid

## 5 References

1. *Ralph O Schmidt, "Multiple Emitter Location and Signal Parameter Estimation. IEEE Transactions on Antennas and Propagation, Volume 34, Issue 3, March 1986.*
2. *JESD204B Interface Standard, Available: <http://www.jedec.org>*
3. *ADC12J4000 Evaluation Module (SLAC649)*
4. *High Speed Data Converter Pro GUI (SLWU087B)*

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