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**Parallel Load Switches for Higher Output Current & Reduced ON-Resistance Design Guide**

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**Design Resources**

- **TIDA-00513** Tool Folder Containing Design Files
- **TIDA-00514** Design Folder
- **TPS22966** Product Folder
- **TPS22959** Product Folder
- **TPS22966EVM-007** Product Folder

**Design Features**

- Increased Maximum Output Current
- Reduced Total ON-Resistance ($R_{ON}$)
- Faster Output Rise Time
- Lower Power Dissipation
- Reduced Quick Output Discharge (QOD) Resistance

**Featured Applications**

- Servers
- Enterprise Computing
- Industrial Systems
- High Current Voltage Rails

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![Diagram of TPS22959](image)

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TIDU859—March 2015

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Parallel Load Switches for Higher Output Current & Reduced ON-Resistance Design Guide

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1 System Description

Users can expand the functionality of existing load switches by placing multiple channels in a parallel configuration. This TI Design demonstrates two examples of paralleling load switches.

1.1 Dual TPS22966

The first example uses both channels of the dual-channel TPS22966 for a total output current of 10 A.

![Figure 1. Dual TPS22966 Block Diagram](image)

1.1.1 Key Specifications

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SPECIFICATION</th>
<th>DETAILS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum Continuous Output Current</td>
<td>10 A</td>
<td>See Section 4.1</td>
</tr>
<tr>
<td>Typical ON Resistance</td>
<td>8 mΩ</td>
<td>See Section 7.1</td>
</tr>
<tr>
<td>Rise Time at 5 V</td>
<td>262 us</td>
<td>See Section 7.2</td>
</tr>
</tbody>
</table>
1.2 **Triple TPS22959**

The second uses three TPS22959 in parallel for a total output current of 30 A.

![Triple TPS22959 Block Diagram](image)

**Figure 2. Triple TPS22966 Block Diagram**

### 1.2.1 Key Specifications

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SPECIFICATION</th>
<th>DETAILS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum Continuous Output Current</td>
<td>30 A</td>
<td>See Section 4.1</td>
</tr>
<tr>
<td>Typical ON Resistance</td>
<td>1.5 mΩ</td>
<td>See Section 8.1</td>
</tr>
<tr>
<td>Rise Time at 5 V</td>
<td>2.4 ms</td>
<td>See Section 8.2</td>
</tr>
</tbody>
</table>
The block diagrams for the two parallel load switch circuits are shown in Figure 3 and Figure 4.

**Figure 3. TPS22966 Functional Block Diagram**
3 Highlighted Products

3.1 TPS22966

- Integrated Dual-Channel Load Switch
- Input Voltage Range: 0.8 V to 5.5 V
- ON-Resistance
  - $R_{ON} = 16 \, \text{mΩ} \text{ at } V_{IN} = 5 \, \text{V (V_{BIAS} = 5 \, \text{V})}$
  - $R_{ON} = 16 \, \text{mΩ} \text{ at } V_{IN} = 3.6 \, \text{V (V_{BIAS} = 5 \, \text{V})}$
  - $R_{ON} = 16 \, \text{mΩ} \text{ at } V_{IN} = 1.8 \, \text{V (V_{BIAS} = 5 \, \text{V})}$
- 6-A Maximum Continuous Switch Current per Channel
- Low Control Input Threshold Enables Use of 1.2 V or Higher GPIO
- Configurable Rise Time
- Quick Output Discharge (QOD)
- SON 14-Pin Package With Thermal Pad
3.2 **TPS22959**

- Integrated Single Channel Load Switch
- $V_{\text{BIAS}}$ Voltage Range: 2.5 V to 5.5 V
- $V_{\text{IN}}$ Voltage Range: 0.8 V to 5.5 V
- Ultra Low $R_{\text{ON}}$ Resistance
  - $R_{\text{ON}} = 4.4 \, \text{m}\Omega$ at $V_{\text{IN}} = 5 \, \text{V}$ ($V_{\text{BIAS}} = 5 \, \text{V}$)
- 15 A Maximum Continuous Switch Current
- Low Quiescent Current (20 $\mu$A for $V_{\text{BIAS}} = 5 \, \text{V}$)
- Low Shutdown Current (1 $\mu$A for $V_{\text{BIAS}} = 5 \, \text{V}$)
- Low Control Input Threshold Enables Use of 1.2 V or Higher GPIO
- Quick Output Discharge (QOD)
- SON 8-Terminal Package with Thermal Pad

4 **System Design Theory**

This section will discuss how placing multiple load switch channels in parallel will affect functionality.

4.1 **Increased Maximum Output Current**

When multiple load switch channels are placed in parallel, the maximum output current increases for two reasons:

1. The total ON Resistance is lower reducing the amount of $V = IR$ voltage drop.
2. The power dissipation will be more distributed leading to better thermal performance.

4.2 **Reduced Total ON-Resistance ($R_{\text{ON}}$)**

Placing multiple load switch channels in parallel will reduce the typical and maximum ON Resistance proportionately to the number of channels in parallel. For example, two channels will halve the ON Resistance, and three channels will result in one third. This event is critical in systems with tight tolerances on the voltage rails.

4.3 **Faster Output Rise Time**

When a single-load switch channel is turned on, the inrush current is limited by a controlled slew rate. When multiple channels are in parallel, the total inrush will increase, allowing for a faster output rise time.

4.4 **Reduced Quick Output Discharge (QOD) Resistance**

For load switches that connect a quick output discharge resistance to the output when disabled, the total QOD resistance will be reduced because multiple QOD resistors will be in parallel. This lower QOD resistance will reduce the output fall time, leading to a faster system power down sequencing.
5 Getting Started Hardware

This section will provide an overview of PCB hardware.

5.1 Dual TPS22966 Connections and Test Points

Table 3 shows a summary of the connections and test points for the dual TPS22966:

<table>
<thead>
<tr>
<th>CONNECTION</th>
<th>NAME</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>J21</td>
<td>V_IN</td>
<td>DC Input to V_IN</td>
</tr>
<tr>
<td>J22</td>
<td>V_OUT</td>
<td>Load Connection for V_OUT</td>
</tr>
<tr>
<td>JP22</td>
<td>V_BIAS</td>
<td>Power</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Connects V_BIAS to V_IN</td>
</tr>
<tr>
<td>JP21</td>
<td>ON Control</td>
<td>Connects ON pin to V_IN or GND</td>
</tr>
<tr>
<td>TP21</td>
<td>V_IN Sense</td>
<td>Sense Connection to V_IN</td>
</tr>
<tr>
<td>TP26</td>
<td>V_OUT Sense</td>
<td>Sense Connection to V_OUT</td>
</tr>
<tr>
<td>TP24</td>
<td>V_BIAS</td>
<td>V_BIAS Connection</td>
</tr>
<tr>
<td>TP23</td>
<td>ON</td>
<td>Enable Connection</td>
</tr>
<tr>
<td>TP22, TP27, TP28, TP29</td>
<td>GND</td>
<td>Connection to Board Ground</td>
</tr>
</tbody>
</table>

5.2 Triple TPS22959 Connections and Test Points

Table 4 shows a summary of the connections and test points for the triple TPS22959:

<table>
<thead>
<tr>
<th>CONNECTION</th>
<th>NAME</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>J31</td>
<td>V_IN</td>
<td>DC Input to V_IN</td>
</tr>
<tr>
<td>J32</td>
<td>V_OUT</td>
<td>Load Connection for V_OUT</td>
</tr>
<tr>
<td>JP31</td>
<td>V_BIAS</td>
<td>Power</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Connects V_BIAS to V_IN</td>
</tr>
<tr>
<td>JP32</td>
<td>ON Control</td>
<td>Connects ON pin to V_IN or GND</td>
</tr>
<tr>
<td>TP31</td>
<td>V_IN Sense</td>
<td>Sense Connection to V_IN</td>
</tr>
<tr>
<td>TP35</td>
<td>V_OUT Sense</td>
<td>Sense Connection to V_OUT</td>
</tr>
<tr>
<td>TP33</td>
<td>V_BIAS</td>
<td>V_BIAS Connection</td>
</tr>
<tr>
<td>TP34</td>
<td>ON</td>
<td>Enable Connection</td>
</tr>
<tr>
<td>TP32, TP36, TP37, TP38</td>
<td>GND</td>
<td>Connection to Board Ground</td>
</tr>
</tbody>
</table>
6 Test Setup

Figure 5 and Figure 6 show how to collect ON Resistance and turn on measurements for the dual TPS22966 circuit. A similar setup can be used for the triple TPS22959 circuit.
7 Dual TPS22966 Test Data

This section will cover the test data from the dual TPS22966 circuit.

7.1 ON Resistance vs. Load Current

Table 5 provides a summary of the ON Resistance measured at various loads:

<table>
<thead>
<tr>
<th>LOAD CURRENT</th>
<th>V\text{IN} = V\text{BIAS} = 5 \text{ V}</th>
<th>V\text{IN} = V\text{BIAS} = 3.3 \text{ V}</th>
</tr>
</thead>
<tbody>
<tr>
<td>200 mA</td>
<td>7.8 mΩ</td>
<td>8.7 mΩ</td>
</tr>
<tr>
<td>1 A</td>
<td>7.8 mΩ</td>
<td>8.7 mΩ</td>
</tr>
<tr>
<td>5 A</td>
<td>7.9 mΩ</td>
<td>8.8 mΩ</td>
</tr>
<tr>
<td>10 A</td>
<td>8.6 mΩ</td>
<td>9.7 mΩ</td>
</tr>
</tbody>
</table>

7.2 Turn On Waveforms

![Figure 7. Dual TPS22966 Turn On Waveform with V\text{IN} = V\text{BIAS} = 3.3 \text{ V}](image-url)
8 Triple TPS22959 Test Data

This section will cover the test data from the triple TPS22959 circuit.

8.1 ON Resistance vs. Load Current

Table 6 provides a summary of the ON Resistance measured at various loads:

<table>
<thead>
<tr>
<th>LOAD CURRENT</th>
<th>$V_{IN} = V_{BIAS} = 5, \text{V}$</th>
<th>$V_{IN} = V_{BIAS} = 3.3, \text{V}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>200 mA</td>
<td>1.4 mΩ</td>
<td>1.4 mΩ</td>
</tr>
<tr>
<td>1 A</td>
<td>1.4 mΩ</td>
<td>1.4 mΩ</td>
</tr>
<tr>
<td>5 A</td>
<td>1.4 mΩ</td>
<td>1.4 mΩ</td>
</tr>
<tr>
<td>10 A</td>
<td>1.4 mΩ</td>
<td>1.4 mΩ</td>
</tr>
<tr>
<td>15 A</td>
<td>1.5 mΩ</td>
<td>1.5 mΩ</td>
</tr>
<tr>
<td>30 A</td>
<td>1.6 mΩ</td>
<td>1.7 mΩ</td>
</tr>
</tbody>
</table>
8.2 Turn On Waveforms

Figure 9. Triple TPS22959 Turn On Waveform with $V_{IN} = V_{BIAS} = 3.3$ V

Figure 10. Triple TPS22959 Turn On Waveform with $V_{IN} = V_{BIAS} = 5$ V
9 Design Files

9.1 Schematics

To download the Schematics, see the design files at TIDA-00513.

Figure 11. Dual TPS22966 Schematic

Figure 12. Triple TPS22959 Schematic
9.2 **Bill of Materials**
To download the bill of materials (BOM), see the design files at [TIDA-00513](#).

9.3 **Layout Recommendations**
For best performance, all traces should be as short as possible. To be most effective, the input and output capacitors should be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for $V_{IN}$, $V_{OUT}$, and GND helps minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance. The CT trace should be as short as possible to avoid parasitic capacitance.

9.4 **Layer Plots**
To download the layer plots, see the design files at [TIDA-00513](#).

9.5 **Altium Project**
To download the Altium project files, see the design files at [TIDA-00513](#).

9.6 **Layout Guidelines**
To download the Layout Guidelines, see the design files at [TIDA-00513](#).

9.7 **Gerber Files**
To download the Gerber files, see the design files at [TIDA-00513](#).

9.8 **Software Files**
To download the software files, see the design files at [TIDA-00513](#).

10 **References**
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