Art Kay

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AC Coupled, Single-Supply, Inverting and Non-inverting Amplifier Reference Design

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Circuit Description

This design amplifies an ac signal, and shifts the output signal so that it is centered at one half the power supply voltage. Note that the input signal has zero dc offset so it swings above and below ground. The key benefit of this circuit is that it accepts signals which swing below ground even though the amplifier does not have a negative power supply.

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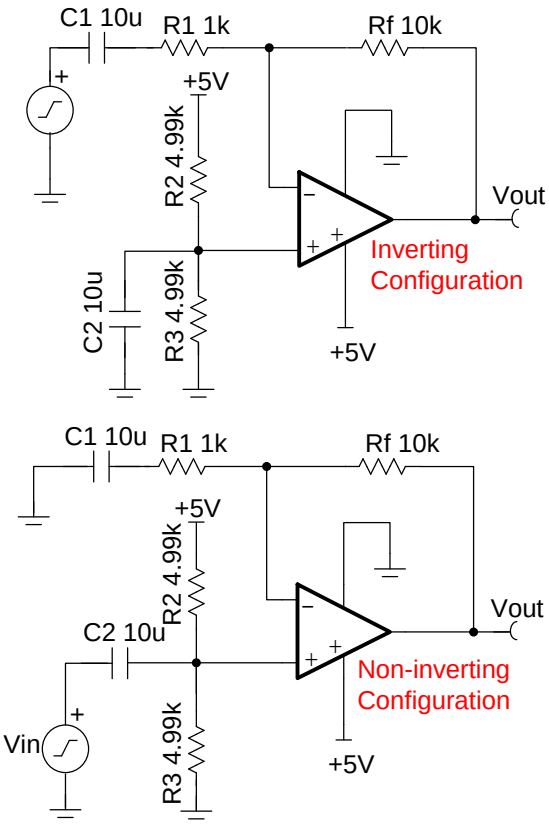

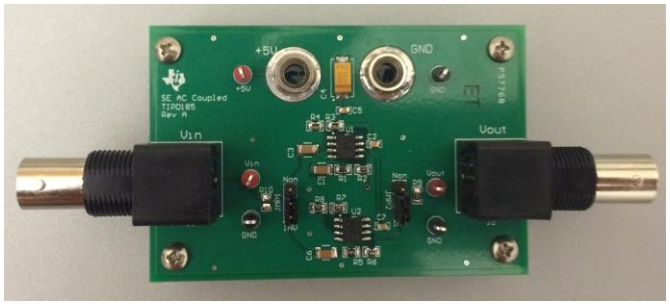

1 Design Summary

The design requirements are as follows:

- Supply Voltage: 5 V
- Input: 480mVpp
- Output: 4.8Vpp

The design goals and performance are summarized in Table 1. Figure 1 depicts the measured transfer function of the design.

Table 1. Comparison of Design Goals, Simulation, and Measured Performance

	Goal	Calculated	Simulated	Measured
f_L	16Hz	16Hz	16Hz	16Hz
f_H	500kHz	500kHz	500kHz	500kHz
Total Noise	100µVrms	74 µVrms	85 µVrms	-na-

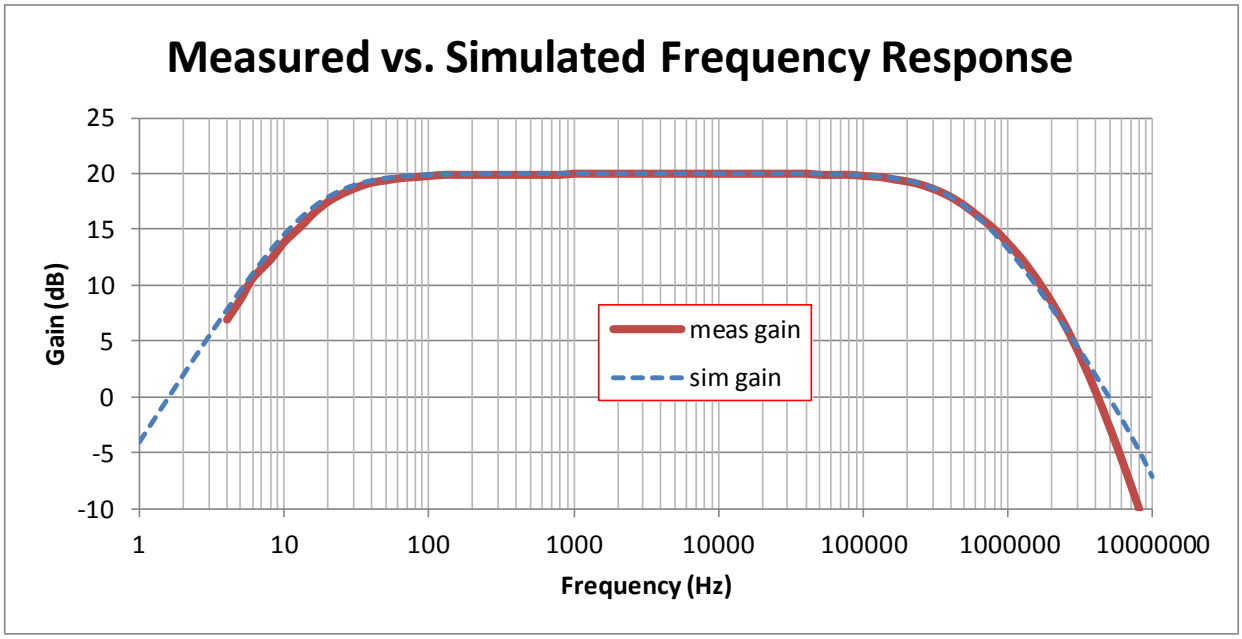

Figure 1: Measured Transfer Function

2 Theory of Operation

Figure 2 shows the schematic of the inverting single supply ac coupled circuit. This TI Design does not cover the details of the non-inverting configuration, because the analysis is identical except that the input signal is applied to the non-inverting input. Nevertheless, measured results for the non-inverting case are provided in Appendix B.

As shown in Figure 2, the input swings below ground and the output is shifted so it is centered at 2.5V. The output is ideally suited for an A/D converter input. The R_2-R_3 voltage divider sets the dc average output voltage. Normally this is set to one half of the supply voltage so that a sinusoidal output can achieve the maximum peak to peak range

The input signal is ac coupled through capacitor C1. The gain of the circuit is set by Rf and R1. In this example the gain is 10V/V, but other gain values can be achieved by changing the ratio. The capacitor C2 is selected to minimize the noise introduced from the resistors R2 and R3. The bandwidth and transient operation of the circuit is determined by the input RC networks. Details on this will be covered in later sections.

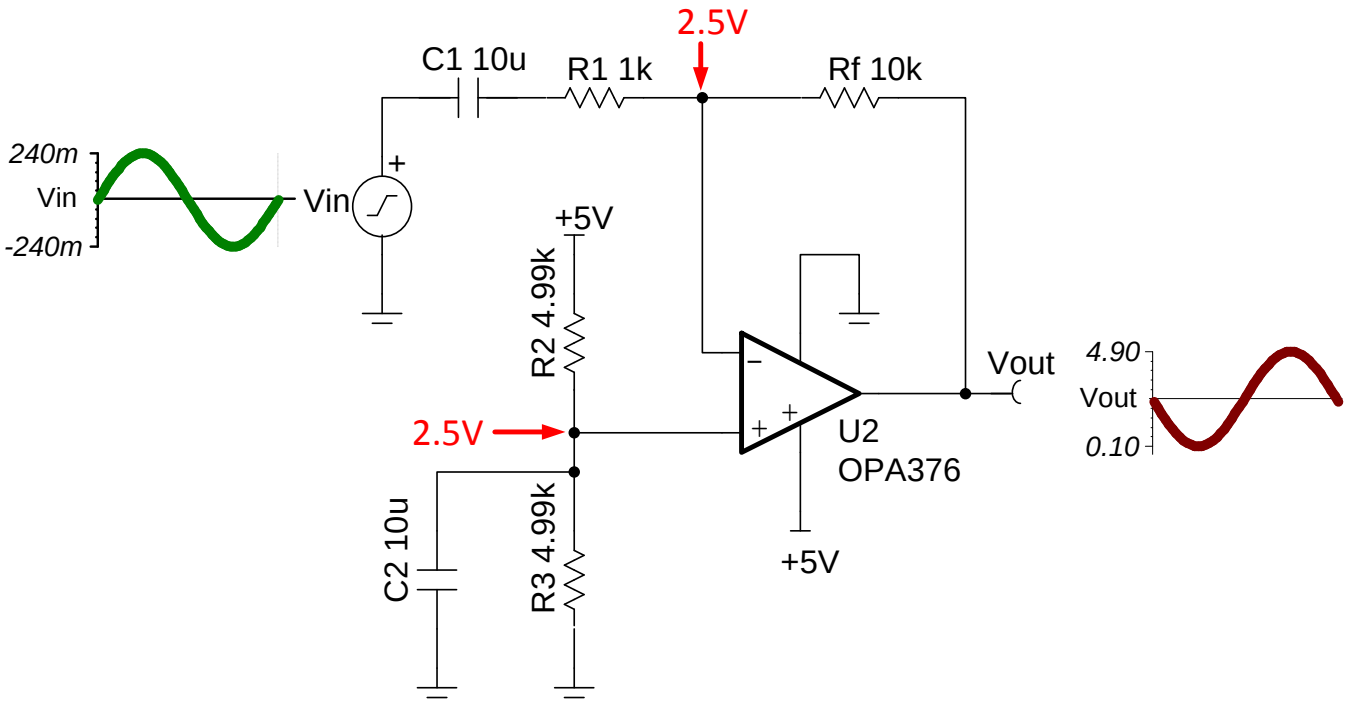

Figure 2: Single Supply ac Coupled Amplifier

2.1 Voltage Gain

The flat band ac voltage gain for this circuit is calculated assuming that the input capacitor C1 is shorted. Note that this is an inverting amplifier, so any output signal will be 180° out of phase with the input.

$$G_{ac} = -\frac{R_F}{R_1} = -\frac{10k\Omega}{1k\Omega} = -10V/V \quad (1)$$

2.2 Setting ac Response – Cutoff Frequencies

The input RC network and the voltage divider R_1C_1 set the lower cutoff frequency for the circuit. Equation (**2**) gives the general relationship for the lower cutoff frequency. In this example the cutoff is set to 16Hz. For most applications it is desirable to set f_L as low as possible. Increasing R_1 or C_1 will decrease this frequency further, but this will also increase the transient startup for this circuit. Furthermore, choosing a large value for R_1 will increase noise.

$$f_{L1} = \frac{1}{2\pi R_1 C_1} = \frac{1}{2\pi(1k\Omega)(10\mu F)} = 16Hz \quad (2)$$

The cutoff frequency of the R_2 R_3 voltage divider has an impact on the circuit's noise. Ideally this cutoff frequency should be set as low as possible to minimize noise. From a noise perspective R_2 and R_3 are in parallel (see Equation (**3**)). In this example, the cutoff frequency is set to 6.4Hz (see Equation (**4**)). The effects this cutoff frequency has on the noise calculations are shown in Section 2.6.

$$R_{n\_div} = \frac{R_2 R_3}{R_2 + R_4} = \frac{(4.99k\Omega)(4.99k\Omega)}{4.99k\Omega + 4.99k\Omega} = 2.495k\Omega \quad (3)$$

$$f_{div} = \frac{1}{2\pi R_{n\_div} C_2} = \frac{1}{2\pi(2.495k\Omega)(10\mu F)} = 6.4Hz \quad (4)$$

The amplifier's upper cutoff frequency is set by the amplifier noise gain and gain bandwidth of the amplifier. In this example, the upper cutoff frequency is 500kHz (see Equations (**5**) (**6**)).

$$G_N = \frac{R_F}{R_1} + 1 = \frac{10k\Omega}{1k\Omega} + 1 = 11 \quad (5)$$

$$f_H = \frac{GBW}{G_N} = \frac{5.5MHz}{11} = 500kHz \quad (6)$$

2.3 Total Current Consumption

This circuit has three main sources of current: quiescent current, voltage divider current, and feedback network current. Note that in this example the feedback current is an ac peak current, so the total current is the maximum instantaneous current that this circuit draws from the supply.

OPA376 Data Sheet

$$I_Q = 950\mu A \text{ dc max} \quad (7)$$

$$I_{DIV} = \frac{V_S}{R_2 + R_3} = \frac{5V}{4.99k\Omega + 4.99k\Omega} = 500\mu A \text{ dc} \quad (8)$$

$$I_{Out\_pk} = \frac{V_{OUT\_MAX}}{R_F + R_1} = \frac{5V}{10k\Omega + 1k\Omega} = 450\mu A \text{pk ac} \quad (9)$$

Total Max Instantaneous

$$I_{total} = I_Q + I_{DIV} + I_{Out\_pk} = 950\mu A + 500\mu A + 450\mu A \text{pk} = 1.89mA \quad (10)$$

2.4 Transient Response

The capacitors C1 and C2 need to fully charge for the circuit to function properly. The definition of fully charged can vary depending on the accuracy required for the circuit. If we assume a 12 bit system the time required to fully charge the input capacitors is given below.

$$\tau_1 = R_1 C_1 = (1k\Omega)(10\mu F) = 0.01s \quad (11)$$

For 12 bit settling

$$T_1 = \ln(2^N)\tau_1 = \ln(2^{12})\,(0.01s) = 0.083s \quad (12)$$

$$\tau_2 = R_2 C_2 = (2.5k\Omega)(10\mu F) = 0.025s \quad (13)$$

For 12 bit settling

$$T_2 = \ln(2^N)\tau_1 = \ln(2^{12})\,(0.025s) = 0.208s \quad (14)$$

2.5 Output Swing

Always keep in mind that the output cannot swing all the way to the power supply rails. Look at both the output swing limitation and the A_{OL} test condition to determine the linear output range. In this case, the amplifier can swing linearly to 50mV from the power supply rail.

OPA376 Output Swing from Rail
RL=10kΩ over temperature

$$40mV \text{ From Rail} \quad (15)$$

OPA376 A_{OL} Condition
RL=10kΩ over temperature

$$50mV < V_O < (V+) - 50mV \quad (16)$$

2.6 Total Noise

Factors affecting output noise:

1. Current noise – In this example current noise is not significant because CMOS devices do not have high current noise (i_n = 2fA/rtHz). Also the impedances connected to the device are relatively low (in kilo-ohm range).
2. Resistor noise from divider – In this example the resistor noise from the divider will be negligible because it is mostly filtered out by C_2 (6.4Hz).

3. Flicker Noise (i.e. 1/f noise) – In this example, the bandwidth is relatively high compared to the 1/f noise corner, so 1/f does not contribute significantly to the total rms noise.

4. Resistor noise from Feedback Network – This can be a significant source of noise. In this case the resistance of the feedback network was selected to minimize noise. Figure 3 displays a convenient way to translate resistor values to spectral density.

$$R_{eq} = \frac{R_f R_1}{R_2 + R_4} = \frac{(10k\Omega)(1k\Omega)}{10k\Omega + 1k\Omega} = 9.09k\Omega \quad (17)$$

$$e_{nr} = \sqrt{4kTR} = \sqrt{4(1.38 \cdot 10^{-23})(298K)(9.09k\Omega)} = 3.86\,nV/\sqrt{Hz} \quad (18)$$

OPA376 Data Sheet

$$e_{n\_opa} = 7.5\,nV/\sqrt{Hz} \quad (19)$$

Total

$$e_{ntotal} = \sqrt{{e_{nr}}^2 + {e_{n\_opa}}^2} \quad (20)$$

Total

$$e_{ntotal} = \sqrt{(3.86\,nV/\sqrt{Hz})^2 + (7.5\,nV/\sqrt{Hz})^2} = 8.4\,nV/\sqrt{Hz} \quad (21)$$

Total rms noise out

$$E_{n\_out\_RMS} = e_{ntotal} \cdot \sqrt{BW_n} \cdot G_N \quad (22)$$

Total rms noise out

$$E_{n\_out\_RMS} = \left(8.4\,nV/\sqrt{Hz}\right) \cdot \sqrt{500kHz \cdot 1.57} \cdot (10\,V/V) = 74.4\mu Vrms \quad (23)$$

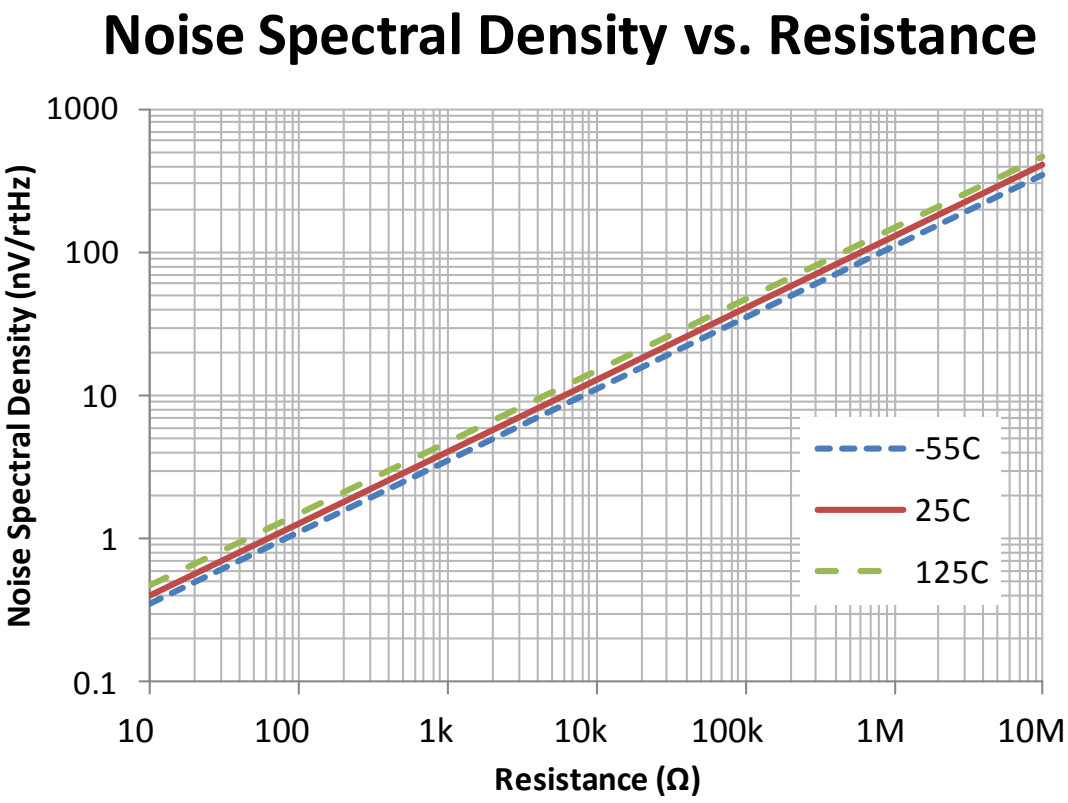

Figure 3: Resistor to Noise Spectral Density Curve

3 Component Selection

3.1 Amplifier

The OPA376 was selected for this design because it has relatively wide bandwidth, low noise, and a rail-to-rail output. Input offset voltage and other dc parameters are not critical in this application as it is ac coupled. This is a very general application and many different amplifiers are suitable for this application.

3.2 Passive Components

This design uses 1% thin film resistors and X7R ceramic capacitors. Special low distortion capacitors are not required for C1 and C2 as the ac voltage across the capacitors is very low during normal operation (i.e. the capacitor is an effective short at these frequencies).

4 Simulation

4.1 Transfer Function

The simulated and measured response vs frequency is shown in Figure 4. As mentioned in Section 2.1, the lower cutoff frequency is set by input coupling capacitor C1 and input resistor R1. The upper cutoff frequency is set by the amplifier's gain bandwidth product. The simulation and measurement results for both the upper and lower cutoff frequencies match well.

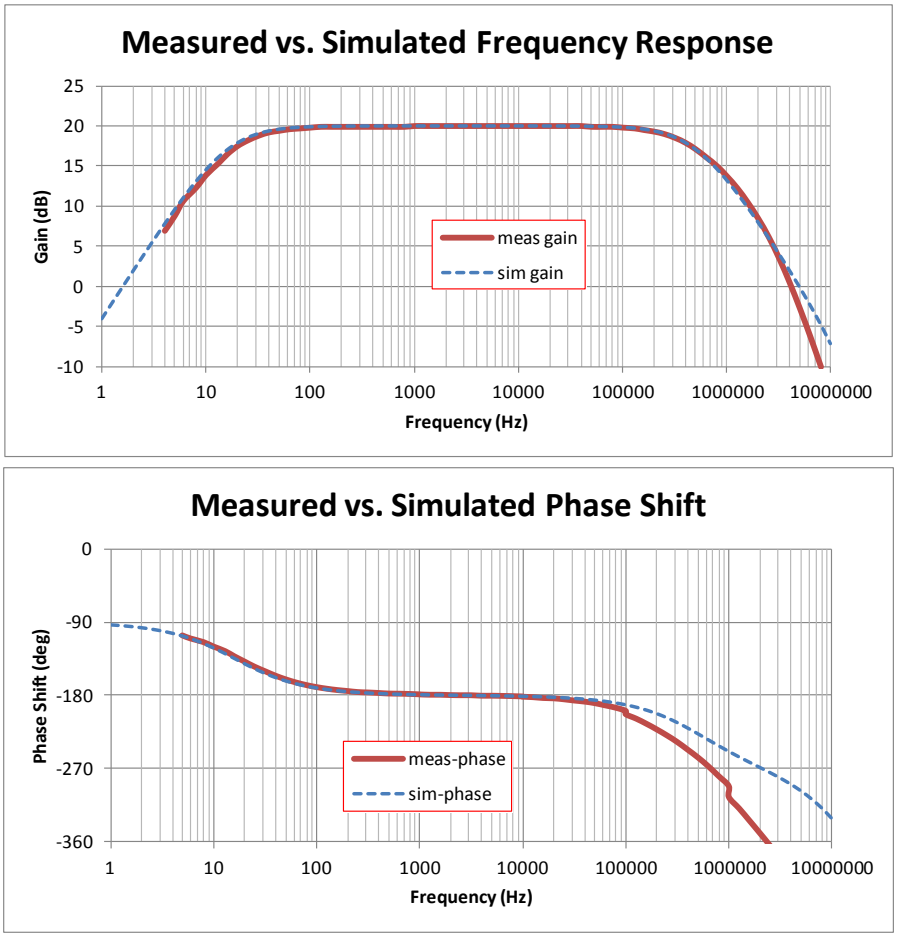

Figure 4: Frequency response for OPA376 ac coupled amplifier

4.2 Transient – Startup

The simulation below shows the startup condition with the input source set to zero volts. Notice that the input voltage divider capacitor (Vdiv) is fully charged in about 150ms. Also, the input coupling capacitor C1 is charging. See Equation (14) for more detail.

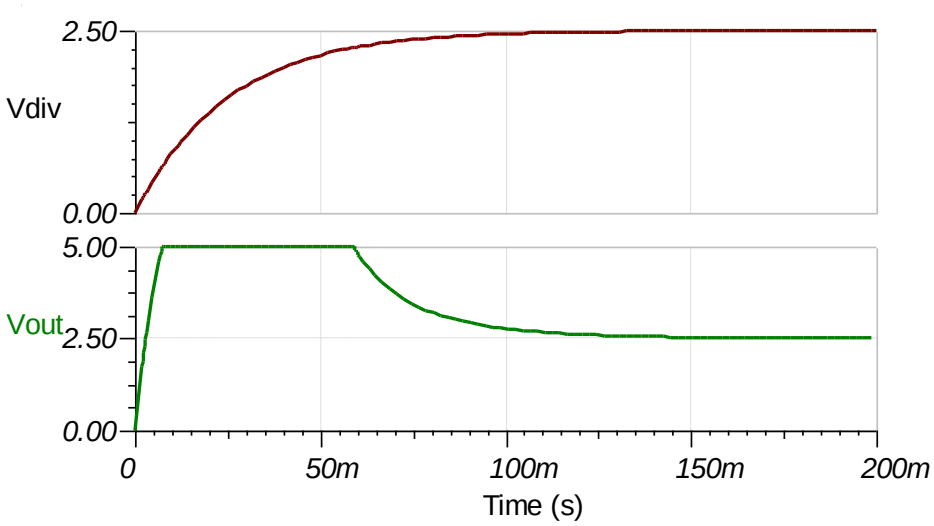

Figure 5: Startup Transient Output Voltage and voltage divider output.

4.3 Transient – Steady State

The simulation below shows the steady state response for a 240mVpk 1kHz signal.

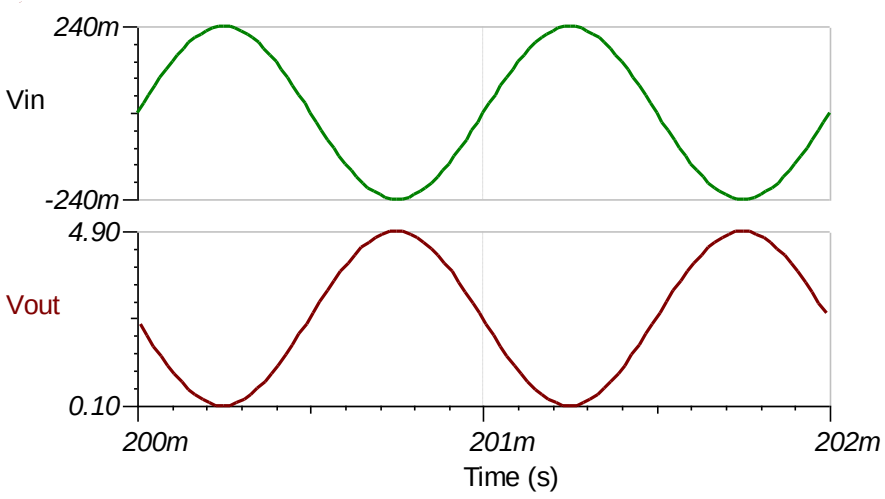

Figure 6: Steady State Transient to a 240mV 1kHz Input Signal

4.4 Noise

The noise spectral density is shown in Figure 7 and the total integrated noise is shown in Figure 8. The simulated results compare well to the hand calculations (see Equation (23)).

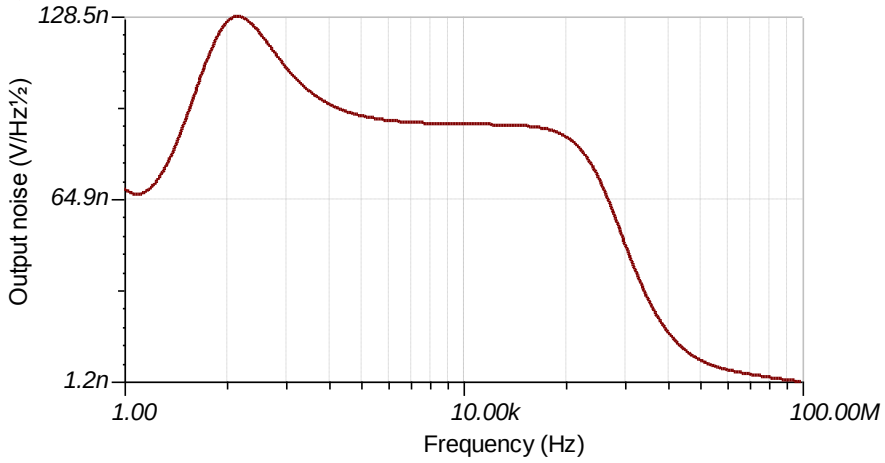

Figure 7: Output Noise Spectral Density Simulation

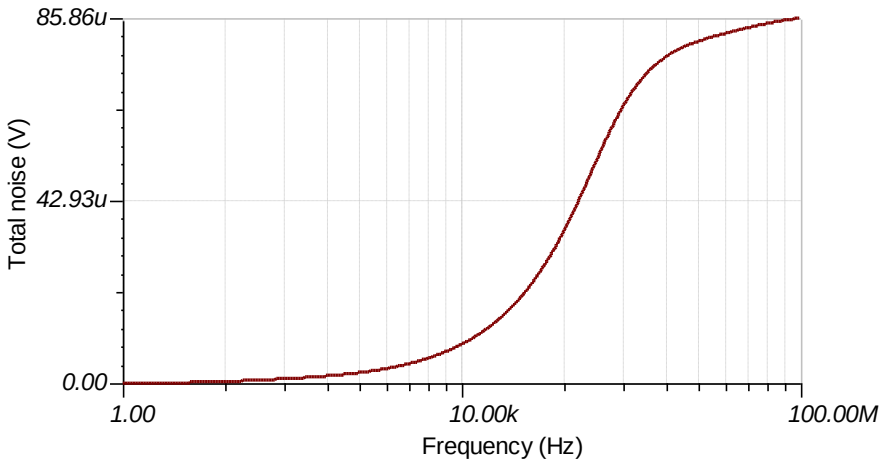

Figure 8: Output Total rms Noise Simulation

5 PCB Design

Note that this PCB includes both the inverting and non-inverting ac coupled amplifier. The PCB schematic and bill of materials can be found in Appendix A.

5.1 PCB Layout

Normal PCB layout precautions were in this layout (i.e. short traces, solid ground connections, minimized vias, close decoupling capacitors).

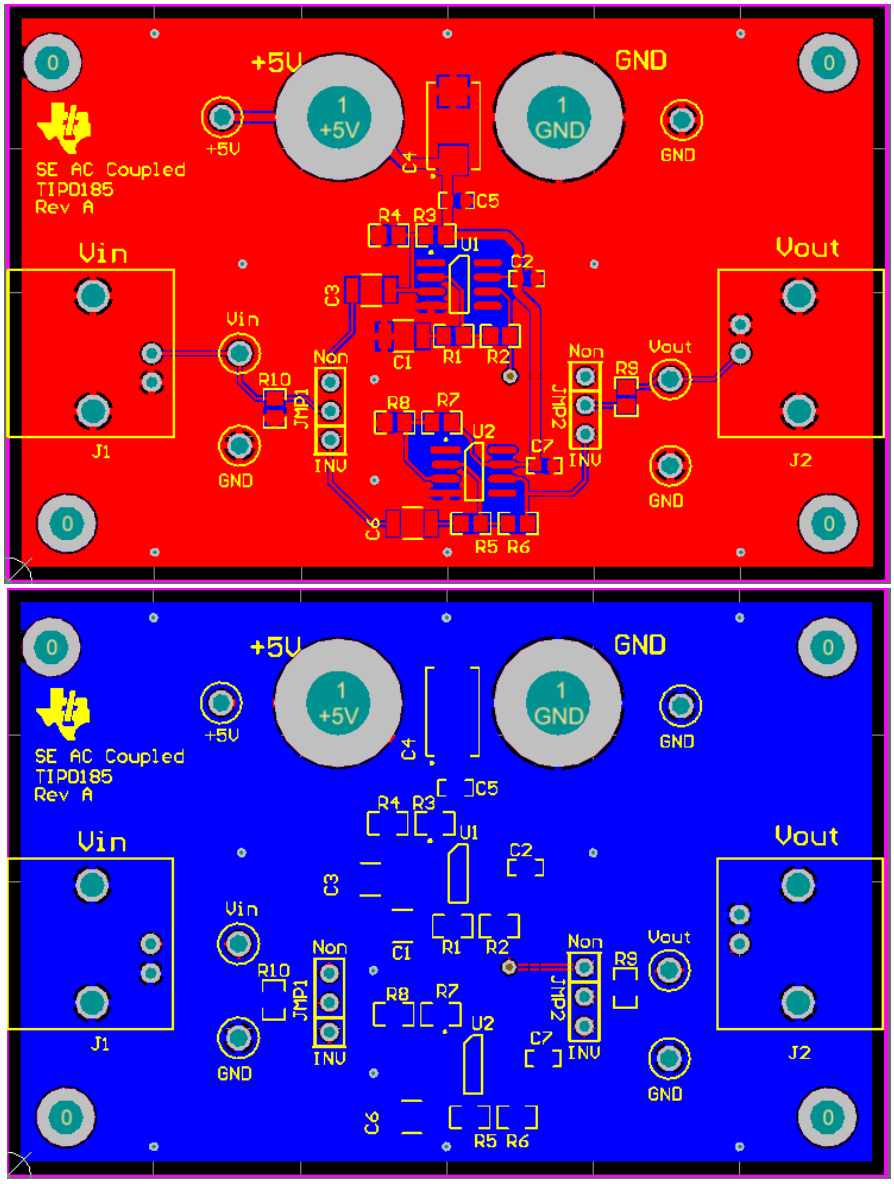

Figure 9: PCB Layout (Top - Red, Bottom - Blue)

6 Verification & Measured Performance

6.1 Transfer Function

The measured and simulated ac transfer functions are compared to each other in Section 4.1. The measured results compare well with the simulations.

6.2 Transient – Steady State

Figure 10 shows the steady state response to a 1kHz, 240mVpk sinusoidal waveform. The input signal multiplies by the gain produces output of 2.4Vpk signal on an 2.5V dc voltage. Thus, the output signal ranges from 0.1V to 4.9V. Section 2.5 explains that the output swing is linear to within 50mV of either supply rail, so the output is linear.

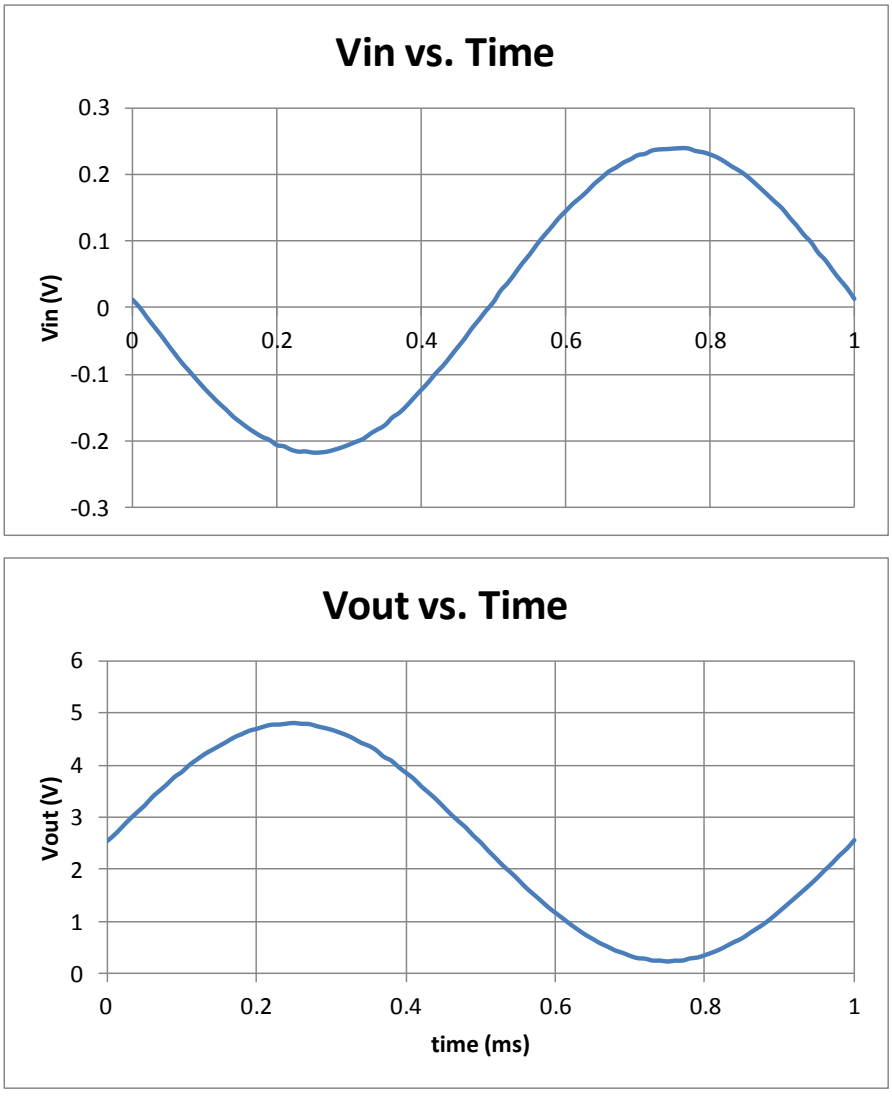

Figure 10: Transient Response to a 1kHz, 240mVpk input signal

7 Modifications

Depending on your design goal you may choose different values.

Design Goal	Modification	Trade off
Minimal Noise	Choose low noise amplifier Reduce feedback resistances	Lower noise amplifier costs more Lower feedback resistors draw more current. Lower feedback resistors will require larger input capacitance to achieve same lower cutoff frequency.
Lower low cutoff frequency	Increase R1 x C1	This will increase transient start up time.
Upper cutoff frequency	Increase gain bandwidth	Wider bandwidth devices normally draw more current. Wider bandwidth designs result in higher total integrated noise
Non-inverting Configuration	Use the circuit in Figure 11	The input impedance for the two configurations is different. Zin(inverting) = R1 Zin(non-inverting) =R3 || R4 The inverting configuration has a 180deg phase shift.

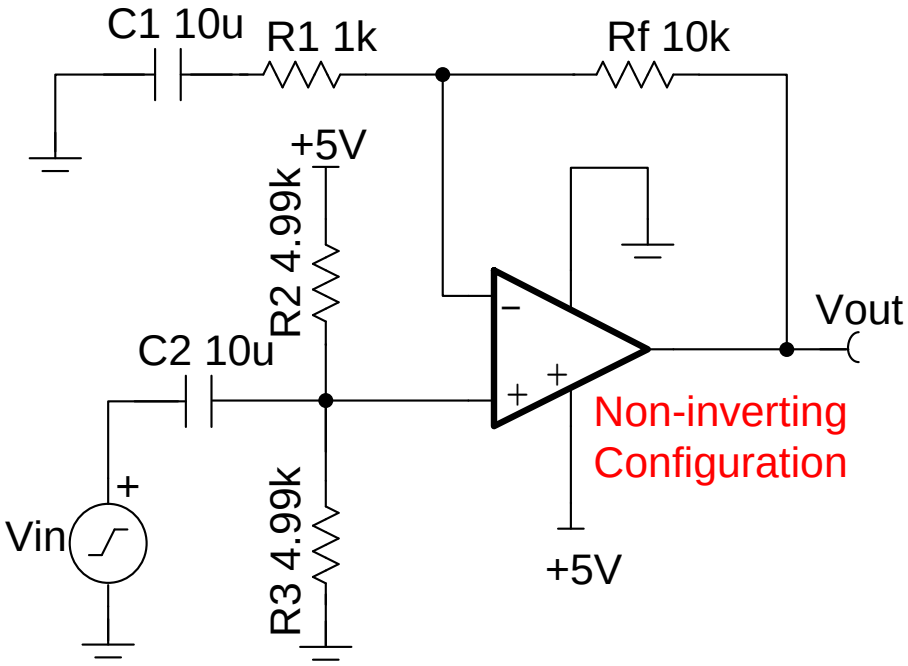

Figure 11: Non-inverting configuration ac coupled single supply amplifier

8 About the Author

Arthur Kay is an applications engineering manager at TI where he specializes in the support of amplifiers, references, and mixed signal devices. Arthur focuses a good deal on industrial applications such as bridge sensor signal conditioning. Arthur has published a book and an article series on amplifier noise. Arthur received his M.S.E.E. from Georgia Institute of Technology, and B.S.E.E. from Cleveland State University.

Appendix A.

A.1 Electrical Schematic

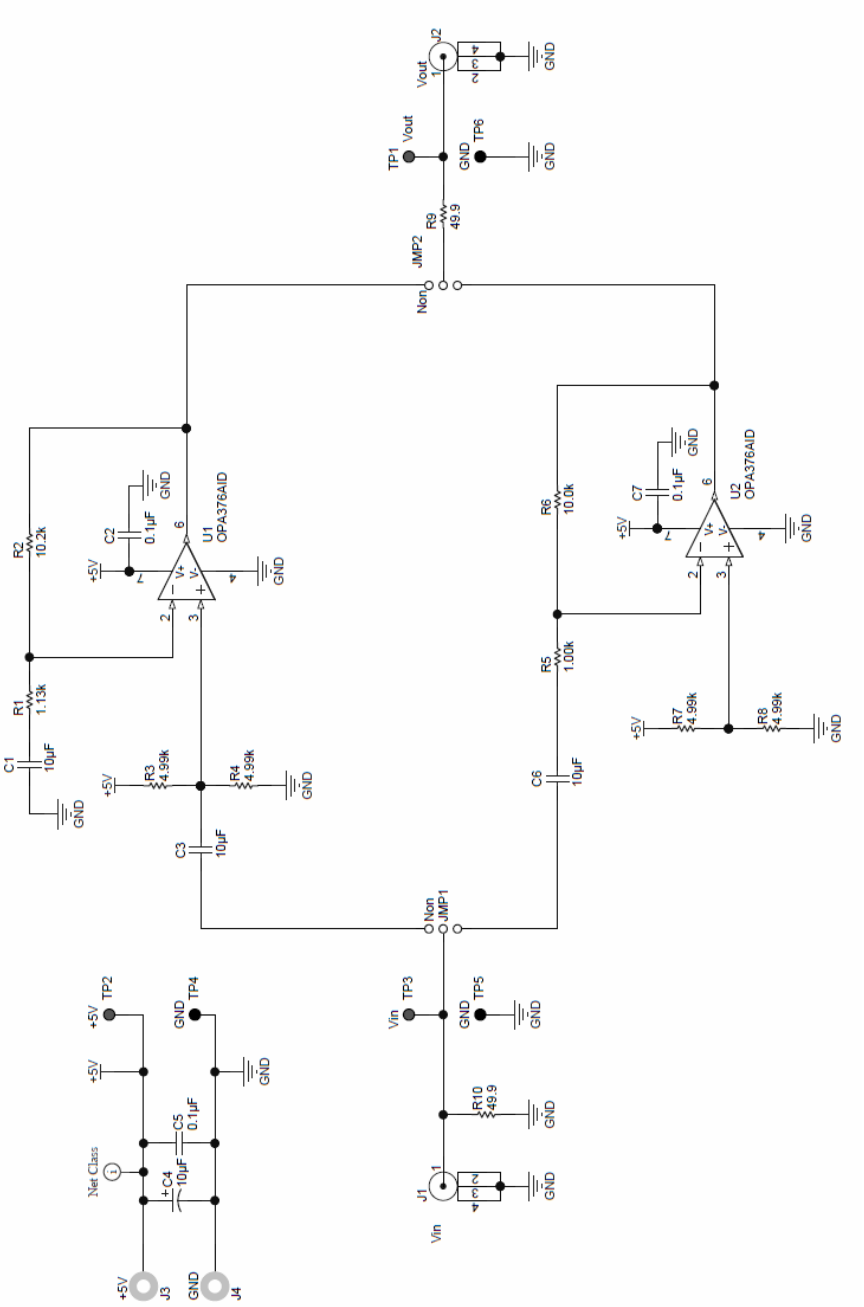

Figure A-1: Electrical Schematic

A.2 Bill of Materials

Qty	Designator	Description	Manufacture	Part Number	Supplier Part Number
3	C1, C3, C6	CAP, CERM, 10 µF, 25 V, +/- 10%, X7R, 1210	AVX Corporation	12103C106KAT2A	478-5728-1-ND
3	C2, C5, C7	CAP, CERM, 0.1 µF, 25 V, +/- 10%, X5R, 0603	AVX Corporation	06033D104KAT2A	478-1244-1-ND
1	C4	CAP, TA, 10 µF, 50 V, +/- 10%, 0.8 ohm, SMD	Vishay Sprague	293D106X9050E2TE3	718-1022-1-ND
1	J1, J2	CONN BNC JACK R/A 50 OHM PCB	TE Connectivity	1-1634612-0	A97555-ND
1	J3, J4	JACK NON-INSULATED .218",Banana Jack	Keystone Electronics	575-4	575-4K-ND
2	JMP1, JMP2	SHUNT LP W/HANDLE 2 POS 30AU	TE Connectivity	JUMP3	A26242-ND
2	JMP1, JMP2	CONN HEADER 50POS .100" SGL GOLD	Samtec Inc	JUMP3	SAM1029-50-ND
1	R1	RES SMD 1.13K OHM 1% 1/8W 0805	Vishay Dale	CRCW08051K13FKEA	541-1.13KCCT-ND
1	R2	RES SMD 10.2K OHM 1% 1/8W 0805	Vishay Dale	CRCW080510K2FKEA	541-10.2KCCT-ND
5	R3, R4, R6, R7, R8	RES, 10.0 k, 1%, 0.125 W, 0805	Vishay Dale	CRCW080510K0FKEA	541-10.0KCCT-ND
1	R5	RES, 1.00 k, 1%, 0.125 W, 0805	Vishay Dale	CRCW08051K00FKEA	541-1.00KCCT-ND
2	R9, R10	RES, 49.9, 1%, 0.125 W, 0805	Vishay Dale	CRCW080549R9FKEA	541-49.9CCT-ND
3	TP1, TP2, TP3	Test Point, TH, Compact, Red	Keystone Electronics	5005	5005K-ND
3	TP4, TP5, TP6	Test Point, TH, Compact, Black	Keystone Electronics	5006	5006K-ND
2	U1, U2	IC OPAMP GP 5.5MHZ RRO 8SOIC	Texas Instruments	OPA376AID	296-22190-5-ND
4		STANDOFF HEX 4-40THR ALUM 1L"	Keystone Electronics	2205	2205K-ND
4		MACHINE SCREW PAN PHILLIPS 4-40	B&F Fastener Supply	PMSSS 440 0025 PH	H703-ND

Appendix B.

B.1 Measured Results for Non-inverting Circuit

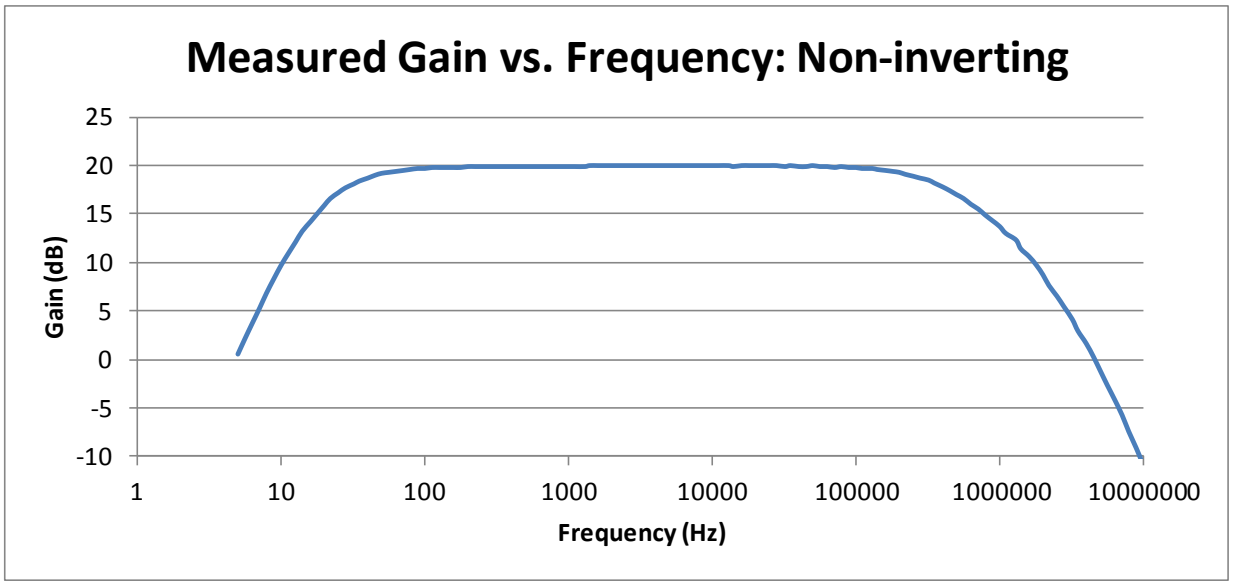

Figure 12: Measured Gain for Non-inverting Circuit

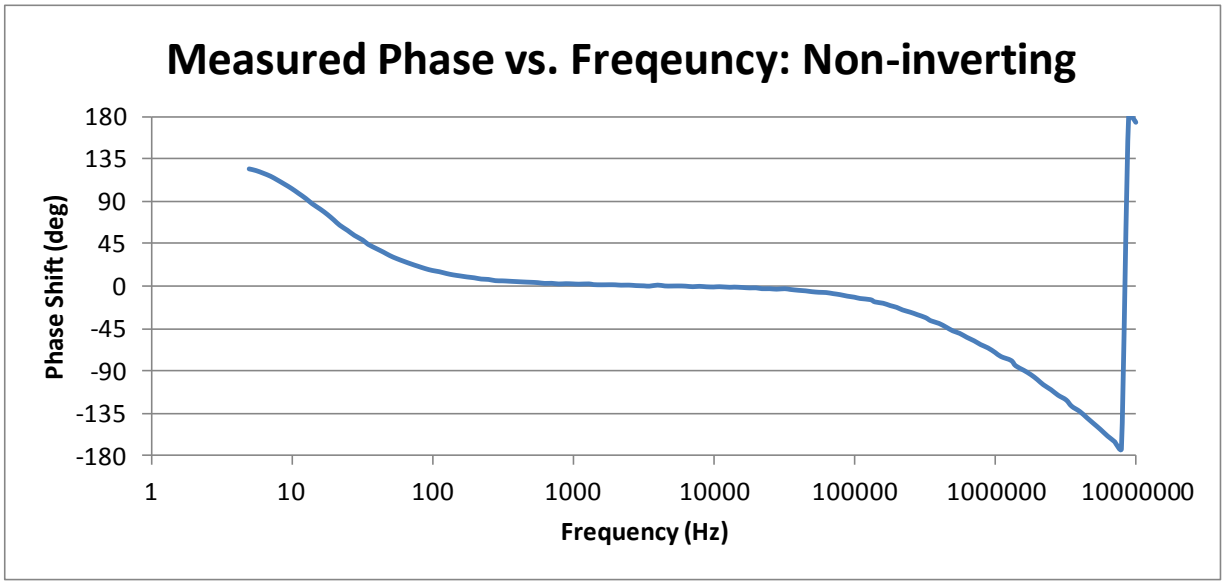

Figure 13: Measured Phase Shift for Non-inverting Circuit

B.2 Measured Results for Non-inverting Circuit

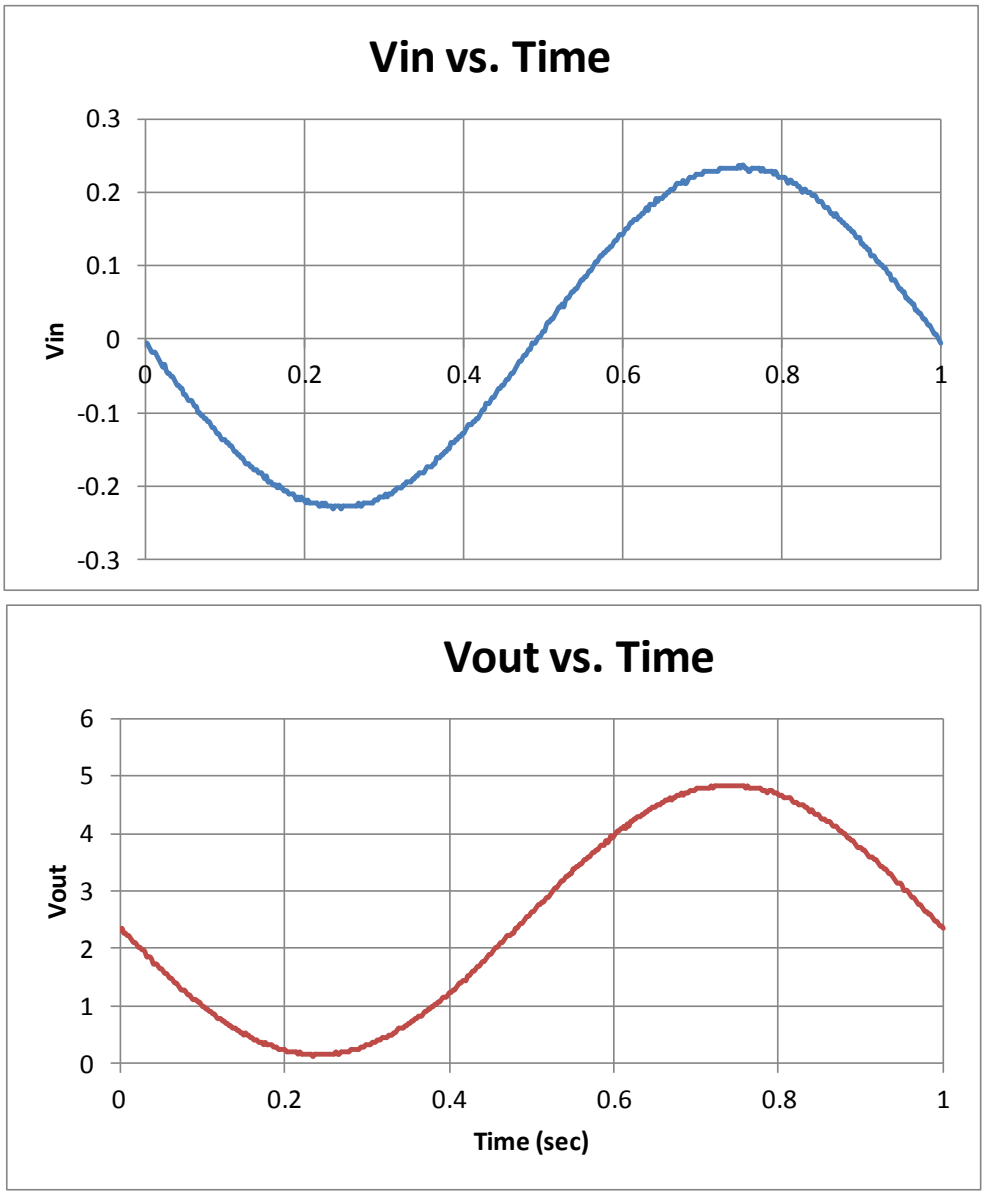

Figure 14: Non inverting transient response

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