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Power Sequencing for the 66AK2E0x and AM5K2E0x Using the UCD9090 Design Guide

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Design Resources

- K2EVM
- 66AK2E05
- 66AK2E02
- AM5K2E04
- AM5K2E02
- UCD9090

Design Features

- Sequences 10 Individual Power Supplies

Featured Applications

- Compatible With Any KeyStone or KeyStone II Design

Circuit Description

The UCD9090 10-Channel Sequencer and System Health Monitor can sequence power-supply rails for the 66AK2E0x and AM5K2E0x SoCs. The UCD9090 also monitors the voltage levels of the power supplies. If a power supply fails, the remaining power supplies can be shut down.

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1 Design Summary

The 66AK2E0x and AM5K2E0x SoCs require that the supply voltages be sequenced for initialization. For details on the voltages and the sequence order, see 66AK2E0x Multicore DSP+ARM KeyStone II System-on-Chip (SoC) (SPRS865D) and AM5K2E0x Multicore ARM KeyStone II System-on-Chip (SoC) (SPRS864D). The UCD9090 device sequences and monitors up to 10 power supplies. This design shows sequencing control using the UCD9090 device. For the full power tree for the XEVMK2EX design, see Figure 1.

Figure 1. Power Tree for the XEVMK2EX Design
1.1 Introduction to the UCD9090

The UCD9090 device can monitor and enable up to 10 power supplies in a programmed sequence. The device includes 10 analog inputs connected to ADCs that monitor the voltage levels of power supply. The analog inputs provide 12 bits of accuracy from 0 to 2.5 V. The device has twenty-one GPIOs which are programable as inputs or outputs. These GPIOs can perform stem-level functions such as external interrupts, power-good, resets, or rail enables. When configured as a rail enable, you can sequence GPIOs up or down and program them as active-high, active-low, or open-drain. The sequencing engine can generate a user-defined sequence of rail enables. You can use the Fusion Digital Power Designer software to program the conditions for the sequence and store that configuration into the internal flash memory.

2 Block Diagram

![Block Diagram](image-url)

Figure 2. Block Diagram
# Implementation

The UCD9090 device sequences and monitors the power outputs of the XEVMK2EX design. If an output fails, the UCD9090 disables the power supplies in the programmed sequence. For a list of the power supplies for the XEVMK2EX design, see Table 1.

## Table 1. XEVMK2EX Power Supplies Controlled by the UCD9090

<table>
<thead>
<tr>
<th>Sequence</th>
<th>Power Supply</th>
<th>Voltage</th>
<th>Rail Enable</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>TPS65400</td>
<td>3.3 V</td>
<td>VCC3V3_AUX_EN</td>
<td>Local system 3.3 V isolated from K2E</td>
</tr>
<tr>
<td>2</td>
<td>TPS544C25</td>
<td>Core AVS</td>
<td>CVDD_EN</td>
<td>K2E core AVS power supply</td>
</tr>
<tr>
<td>3</td>
<td>TPS65400</td>
<td>1.0 V</td>
<td>CVDD1_EN</td>
<td>K2E 1.0-V fixed core supply (0.95 V in EVM design)</td>
</tr>
<tr>
<td>4</td>
<td>TPS65400</td>
<td>1.8 V</td>
<td>VCC1V8_EN</td>
<td>K2E 1.8-V I/O voltage supply</td>
</tr>
<tr>
<td>5</td>
<td>TPS54620</td>
<td>1.5 V</td>
<td>VCC1V5_EN</td>
<td>K2E 1.5-V DDR3 I/O voltage supply</td>
</tr>
<tr>
<td>6</td>
<td>TPS51200</td>
<td>0.75 V</td>
<td>VTT_EN</td>
<td>K2E 0.75-V DDR3 VTT I/O voltage supply</td>
</tr>
<tr>
<td>7</td>
<td>TPS65400</td>
<td>0.85 V</td>
<td>VCC0V85_EN</td>
<td>K2E 0.85-V Serdes low-voltage supply</td>
</tr>
<tr>
<td>8</td>
<td>TPS22913B</td>
<td>3.3 V</td>
<td>VCC3V3_EN</td>
<td>SoC side 3.3-V supply (Not connected to K2E directly)</td>
</tr>
<tr>
<td>9</td>
<td>TPS54620</td>
<td>5.0 V</td>
<td>VCC5_EN</td>
<td>K2E USB 5.0-V supply</td>
</tr>
<tr>
<td>10</td>
<td>TPS22913B</td>
<td>5.0 V</td>
<td>USB_VBUS_EN</td>
<td>K2E VBUS pin voltage isolator</td>
</tr>
</tbody>
</table>

For more information on each of these devices, see the respective product folders at [www.TI.com](http://www.TI.com).
2.2 Voltage Monitoring

The UCD9090 device monitors the voltage levels for the power supplies on the XEVMK2EX design. The internal ADC inputs are limited to 2.5 V. To accommodate this limit, a voltage divider connects the 3.3-V and 5-V supply inputs. For the voltage monitor inputs, see Figure 3.

![Figure 3. Voltage Monitor Inputs](image-url)
Each monitor input generates a power-good signal for that rail. The power-good signals can then sequence and define the GPIO logic in the UCD9090 device. The power-good condition for each monitor input is defined in the Vout Config tab of the Fusion Digital Power Designer software. For an overview of the voltage monitor definition, see Figure 4.

**Figure 4. Voltage Monitor Definition**

### 2.3 Rail Enables

The UCD9090 device provides the 10 rail-enable signals to the power supplies on the XEVMK2EX design. For the voltage rail enables, see Figure 5.

**Figure 5. Voltage Rail Enables**
The Pin Assignment tab of the Fusion Digital Power Designer software assigns the rail-enable signals and selects the signal type. For the voltage rail enable selection, see Figure 6.

Figure 6. Voltage Rail-Enable Selection
In the power sequence for the XEVMK2EX design, the Vout Config tab of the Fusion Digital Power Designer software defines the rail enable for each power supply. The EVM uses a time-based sequence for the power supplies initiated by a control input from the BMC processor. When the processor enables the sequence, the rail enables are activated as defined in Figure 7. You can use the turn-on timing setting to set the delay for the rail and to specify the turn-off delay for a sequenced shutdown. For an overview of the definition of the voltage rail-enable sequence, see Figure 7.
When the power sequence completes, the K2E SoC requires all voltage rails be present. If a voltage rail fails during operation, the UCD9090 device shuts down the rest of the rails. If the power supply fails, the fault shutdown slave window defines which additional power supplies are disabled. For an overview of the fault shutdown condition of the voltage rail-enable sequence, see Figure 8.

Figure 8. Voltage Rail-Enable Fault Shutdown Condition
2.4 **BMC Processor Control Signals**

The XEVMK2EX design uses the BMC processor to control the state of the K2E, including initiating the sequencing of the power supplies. The processor provides two control inputs and two monitor outputs. We intended the MAIN\_POWER\_START input to enable the VCC3V3\_AUX supply and the SOC\_POWER\_START input to initiate the sequence of the rest of the rails. The released version of the configuration does not use the MAIN\_POWER\_START input. When the SOC\_POWER\_START is set at the beginning of the sequence, the UCD9090 enables the VCC3V3\_AUX supply. For the BMC sequencing control signals, see Figure 9.

To configure the power supply sequence, do the following:
1. Use the window in the Vout Config tab to select the on and off dependencies for the GPI sequence.
2. Use the Pin Assignment tab to define the pins for GPI and GPO (see Figure 10).
3. Select Configure, listed under Actions, to define the GPO (a window with two conditions to be assigned to an OR function opens [see Figure 11]).
4. Select the login function that controls the GPO (see Figure 12).

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**Figure 9. BMC Sequencing Control Signals**
Figure 10. GPI and GPO Pin Assignment
Figure 11. GPO Pin Configuration

Figure 12. GPO Pin Output Criteria
Configuration of the UCD9090

Use the Fusion Digital Power Designer software and the PMB interface to generate the register values and to program the UCD9090 device. The Fusion Digital Power Designer software uses the TI USB-TO-GPIO USB Interface Adapter EVM to connect a PC running the Fusion software to the XEVMK2EX design. Only the PMBUS_DAT, PMBUS_CLK and GND signal must be connected to program the UCD9090 device. When you have configured the UCD9090, click Write to Hardware on the tab labeled Configure to store the configuration to the UCD9090 device.

![USB Interface Adapter Pod](image1.png)

Figure 13. USB Interface Adapter Pod
Configuration of the UCD9090

Figure 14. USB Pod to PMBus Header Connection

PMBus Head

Figure 14. USB Pod to PMBus Header Connection
3.1 Configuration File

You can use the Fusion Digital Power Designer to open an XML file as a project. The XML configuration file for the EVMK2E is in the product folder for this design. When you open the configuration file with the software, it displays the Vout Config tab. This tab shows the power supply rail enable and the sequence order.

4 PCB Design

You can find the PCB, schematic, and bill of materials in the product folder for this design. For details on the placement and layout of the PCB, refer to 10-Rail Power Supply Sequencer and Monitor with ACPI Support (SLVSA30A). This design was implemented as part of the XEVMK2EX design. The PCB file includes all parts associated with the 66AK2E0x EVM device.

5 Modifications

The XEVMK2EX design includes a few power supplies that are not used by the K2E SoC. The XEVMK2EX design includes the board monitor controller (BMC) that acts as a master to set the boot mode and initiate the power supply sequence for the K2E SoC. These power supplies are unnecessary for customer designs and can be removed. The UCD9090 device includes other features unused by the XEVMK2EX design. For more information on capabilities that might be useful in your design, see 10-Rail Power Supply Sequencer and Monitor with ACPI Support (SLVSA30A).

5.1 Power Supply Removal

In the XEVMK2EX design, the VCC3V3_AUX and the VDD3V3 voltages are not used by the K2E SoC. Your design may not require these supplies.

5.2 BMC Initialization

The current design requires the external control of the BMC to initiate the sequence using the SOC_POWER_START input. You can modify the programming of the UCD9090 device to initiate the sequence when power is available to the device. You can include monitor input for the source voltage used by the SoC power supplies and change the sequence to initiate when the source voltage power good condition exists. The supplies shut downs if one of the voltage rails fails. You can use the SOC_POWER_GOOD signal as a test point or drive an LED to indicate when the supplies are stable.

6 References

- UCD9090 10-Rail Power Supply Sequencer and Monitor with ACPI Support (SLVSA30)
- 66AK2E05, 66AK2E02 Multicore DSP+ARM KeyStone II System-on-Chip (SoC) (SPRS865)
- AM5K2E04, AM5K2E02 Multicore ARM KeyStone II System-on-Chip (SoC) (SPRS864)
About the Author

WILLIAM TABOADA is an application engineer at TI, where he supports the KeyStone I and KeyStone II multicore processor families. William brings to this role his extensive experience designing processor based systems utilizing DDR3 memory architecture and high-speed serial interfaces. William earned a Bachelor of Science (BS) from Lehigh University and a Master of Science (MS) from The George Washington University.
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