**TI Designs**

TI Designs are analog solutions created by TI’s analog experts. Reference designs offer the theory, component selection, and simulation of useful circuits. Circuit modifications that help to meet alternate design goals are also discussed.

**Circuit Description**

This Reference-Design is to power the USB port that aims to support Quick Charge 2.0 from Lithium-ion battery or a voltage supply between 2.7 V and 4.4 V. The Reference-Design includes a boost converter TPS61088 to boost the input voltage up to 12 V, a 12-V E-fuse TPS2592AA with 2-A to 3.7-A adjustable current limit for short circuit protection and a QC2.0 interface IC CHY100 to adjust output voltage according to the Quick Charge 2.0 standard. This Reference-Design can support 5V&3A, 9V&2A and 12V&1.5A output power.
Contents

1 Introduction ........................................................................................................................................ 4

2 Design Description ......................................................................................................................... 4
  2.1 Boost Converter Solution ......................................................................................................... 5
    2.1.1 Frequency, Inductor and capacitor selection ................................................................. 5
    2.1.2 Compensation Capacitor and Resistor ............................................................................. 6
    2.1.3 Output Voltage Setting ..................................................................................................... 6
  2.2 E-fuse and Interface .................................................................................................................... 6

3 A method to Enter QC2.0 .............................................................................................................. 6

4 Test Result ........................................................................................................................................ 7
  4.1 Efficiency ................................................................................................................................. 7
  4.2 Thermal Performance .............................................................................................................. 8
  4.3 VBUS Voltage Transition ....................................................................................................... 9
  4.4 Load Transient ........................................................................................................................ 11
  4.5 Short Circuit Protection ......................................................................................................... 12
  4.6 Mobile phone Charging ......................................................................................................... 12

5 Schematic, Bill of Materials and PCB Layout ............................................................................. 14
  5.1 Schematic ............................................................................................................................... 14
  5.2 Bill of Materials ....................................................................................................................... 15
  5.3 PCB Layout ............................................................................................................................. 16
List of Figure

Figure 1: Block Diagram of the Reference-Design ...................................... 4
Figure 2 TPS61088 Boost Converter Schematic ........................................ 5
Figure 3 Interface-Circuit to Enter Quick Charge 2.0 .................................. 7
Figure 4 Efficiency of the Reference Design .............................................. 8
Figure 5 Thermal Performance at V_{\text{IN}}=3.6\text{V} .................................................... 9
Figure 6 V_{\text{BUS}} Transits from 5\text{V} to 9\text{V} at V_{\text{IN}}=3.6\text{V} ...................... 10
Figure 7 V_{\text{BUS}} Transits from 9\text{V} to 12\text{V} at V_{\text{IN}}=3.6\text{V} ......................... 10
Figure 8 V_{\text{BUS}} Transits from 5\text{V} to 12\text{V} at V_{\text{IN}}=3.6\text{V} ......................... 10
Figure 9 Falling-Time at V_{\text{IN}}=3.6\text{V}&I_{\text{OUT}}=0\text{A} ........................................... 11
Figure 10 Load Transient Waveform ......................................................... 12
Figure 11 Short Circuit Protection ............................................................. 12
Figure 12 Setup to Charge a Mobile Phone ................................................. 13
Figure 13 Waveform of Charging a Mobile Phone ........................................ 13
Figure 14 PMP9773 Schematic ................................................................. 14
Figure 15 PMP9773 Top Overlay, Top Layer and Top Paste ........................... 16
Figure 16 PMP9773 Bottom Overlay and Bottom Layer .............................. 16

List of Table

Table 1 Performance Specification Summary .............................................. 4
Table 2 PMP9775 Output Effective Capacitance and Ripple ....................... 6
Table 3 Quick Charge 2.0 Lookup Table ..................................................... 7
Table 4 Temperature-Rise at V_{\text{BUS}}=9\text{V} ....................................................... 9
Table 5 Over/undershoot of Load Transient ............................................... 12
Table 6 PMP9773 Bill of Material .............................................................. 15
1 Introduction

The Reference-Design (RD) builds a power circuit for USB port that supports Quick Charge 2.0 (QC2.0) class A. The input and output capability of this design is shown in Table 1. By using a charger interface IC, the output voltage $V_{BUS}$ can be one of the three voltages, 5V, 9V or 12V, based on the signal on D+ and D- pin of the USB port. The maximum output power of the RD is 18W.

<table>
<thead>
<tr>
<th>specification</th>
<th>Test Condition</th>
<th>Min</th>
<th>typical</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage</td>
<td></td>
<td>2.7</td>
<td>4.4</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Output Voltage</td>
<td>Output Current lower than the maximum value</td>
<td>5.0</td>
<td>V</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>9.0</td>
<td>V</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>12.0</td>
<td>V</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Output Current</td>
<td>$V_{BUS} = 5V$</td>
<td>0</td>
<td>3</td>
<td>2</td>
<td>A</td>
</tr>
<tr>
<td></td>
<td>$V_{BUS} = 9V$</td>
<td>0</td>
<td>2</td>
<td>1.5</td>
<td>A</td>
</tr>
<tr>
<td></td>
<td>$V_{BUS} = 12V$</td>
<td>0</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

The following chapters describe the operation principle, schematic, PCB layout, output characteristics and thermal performance of the RD.

2 Design Description

The RD’s block diagram is shown in Figure 1. The primary input power is Lithium-ion battery, the voltage of which is from 3 V to 4.35 V. According the QC2.0 standard class A, the voltage for the USB power output is 5 V, 9 V or 12 V. So the TPS61088 is used to boost the low input voltage to the target voltage.

The TPS2592AA is a 12-V e-Fuse with adjustable 2-A to 3.7-A current limit. It is to protect the battery and the TPS61088 in case of short circuit happening in the USB output port.

![Block Diagram of the Reference-Design](image)

**Figure 1: Block Diagram of the Reference-Design**

The Charger interface IC communicates with the portable device being charged to identify if the portable device supports QC2.0. If yes, it changes the boost converter’s output voltage by changing the feedback resistor according to the requirement of the portable device. If not, the boost converter keeps the default output voltage of 5 V.
2.1 Boost Converter Solution

The schematic of the boost converter solution based on the TPS61088 is shown in Figure 2. The detail operating principle, pin functions and electrical characteristics of the TPS61088 are described in its datasheet (SLVSCM8A).

![Figure 2 TPS61088 Boost Converter Schematic](image)

2.1.1 Frequency, Inductor and capacitor selection

The switching frequency of a boost converter impacts its inductor value, input and output capacitor value and the efficiency. High frequency benefits small inductor and capacitor value, and also small solution size, but is adverse to efficiency; while low frequency benefits high efficiency but causes large solution size. The switching frequency of the TPS61088 is set by a resistor between its SW pin and FSW pin. The frequency at this design is set to approximate 500 KHz.

The average input current of a boost converter is defined by equation (1), where \( \eta \) is the efficiency and \( V_{OUT} \) is the output voltage of the boost converter (the output voltage of the RD is represented by \( V_{BUS} \)). Given \( V_{IN}=3V \), \( \eta=0.9 \), \( V_{OUT}=9V \), \( I_{OUT}=2A \), the average input current \( I_{AVE}=6.7A \).

\[
I_{AVE} = \frac{V_{OUT} \cdot I_{OUT}}{V_{IN} \cdot \eta} \quad (1)
\]

The inductor value is determined by the current ripple, normally 20% to 40% of the average input current. Then inductor value can be calculated by equation (2), where \( I_{PP} \) is the peak to peak current ripple, \( f_s \) is 500 KHz.

\[
L = \frac{1}{I_{PP} \cdot \left( \frac{1}{V_{OUT} - V_{IN}} + \frac{1}{V_{IN}} \right) \cdot f_s} \quad (2)
\]

A 1.5-\( \mu \)H inductor is selected in the RD considering the efficiency of the RD and package of the inductor.

Low-ESR ceramic capacitor is used for this high switching frequency boost converter. So the output voltage ripple is primarily determined by the equation (3), in which \( C_{OUT} \) is the effective capacitance.
Three 22-µF, 0805 package capacitors in parallel are used in the RD. The effective capacitance of ceramic capacitor is largely impacted by its bias voltage. The total effective capacitance and output ripple at $V_{IN}=3.6V$ based on equation (3) are shown in Table 2.

Table 2 PMP9775 Output Effective Capacitance and Ripple

<table>
<thead>
<tr>
<th>$V_{OUT}$</th>
<th>5 V</th>
<th>9 V</th>
<th>12 V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Effective Cap.</td>
<td>33 µF</td>
<td>16.5 µF</td>
<td>13.2 µF</td>
</tr>
<tr>
<td>$V_{RIP}$</td>
<td>51 mV</td>
<td>145 mV</td>
<td>159 mV</td>
</tr>
</tbody>
</table>

2.1.2 Compensation Capacitor and Resistor

The converter must be stable under 5 V, 9 V and 12 V with the same compensation capacitor and resistor, which are C2 and R1 in Figure 2. The C2 and R1 are designed based on 5-V output condition, because the right hand panel zero of the boost converter is smallest at 5-V condition. Refer to the TPS61088 datasheet for the detail about the small signal model.

In real board, the stability and phase margin of the converter can be estimated using the load transient waveform, as described in the page 5, 6 of the application-note “Optimizing Transient Response of Internally Compensated dc-dc Converters With Feedforward Capacitor” (SLVA289).

2.1.3 Output Voltage Setting

The output voltage of the boost converter is set by the interface IC through changing the TPS61088 feedback resistor. As shown in Figure 2, when R8 and R9 are opened, the $V_{OUT}$ can be calculated by equation (4). The RD output $V_{BUS}$ is approximately equal to $V_{OUT}$ when the e-fuse is enabled.

$$V_{OUT} = \frac{R5 + R6}{R6} \cdot V_{REF} \approx 5V$$

When R8 is shorted to GND and R9 keeps opened, the output voltage can be calculated by equation (5)

$$V_{OUT} = \frac{R5 \cdot (R6 + R8) + R6 \cdot R8}{R6 \cdot R8} \cdot V_{REF} \approx 9V$$

When R8 and R9 are both shorted to GND, the output voltage can be calculated by the equation (6)

$$V_{OUT} = \frac{R5 \cdot (R6 \cdot R8 + R8 \cdot R9 + R6 \cdot R9) + R6 \cdot R8 \cdot R9}{R6 \cdot R8 \cdot R9} \cdot V_{REF} \approx 12V$$

2.2 E-fuse and Interface

The external components for the E-fuse TPS2592AA and the interface control IC CHY100 are easy to design following the suggestion in their datasheets.

3 A method to Enter QC2.0

According the description in the CHY100 datasheet, the processes to enter QC2.0 are:

- Apply a voltage between 0.325 V and 2 V to D+ for at least 1.25 seconds
- Discharge the D- voltage below 0.325 V for at least 1ms while keep the D+ voltage above 0.325 V
- Apply the voltage levels in Table 3 to set the output voltage. (must keep the D+ voltage above 0.325 V)
Table 3 Quick Charge 2.0 Lookup Table

<table>
<thead>
<tr>
<th>D+</th>
<th>D-</th>
<th>Output Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.325 V – 2 V</td>
<td>0.325 V – 2 V</td>
<td>12 V</td>
</tr>
<tr>
<td>&gt;2 V</td>
<td>0.325 V – 2 V</td>
<td>9 V</td>
</tr>
<tr>
<td>0.325 V – 2 V</td>
<td>GND</td>
<td>5 V(default)</td>
</tr>
</tbody>
</table>

Figure 3(a) shows an interface-circuit that can help the RD to enter QC2.0 for evaluation. Following lists the steps to connect the interface-circuit to the reference-design and the D+/D- voltage, and the $V_{BUS}$ voltage in each step is shown in Figure 3(b):

S1 Connect a power-supply between 2.7 V and 4.4 V to the RD, and connect a 3V power-supply to the interface-circuit (the $V_{BUS}$ ramps up to approx. 5V after this step).

S2 Close the Jumper J1, connect V1 to the D+ pin and keep the D- floating, then wait at least 2 seconds. Two actions happen during this 2 seconds:
- The D+ and D- voltage equal to 1.5V for 1.25 seconds. (because the D+ and D- pins connect together inside the CHY100)
- Then the D+ keeps at 1.5V and the D- voltage decrease to zero. (because the D+ and D- pins disconnect and a resistor inside the CHY100 discharges the D-)

S3 Open the J1, and then connect the D- to V2. The $V_{BUS}$ jumps to 9V. (because the D+ voltage is above 3V and the D- voltage is between 2V and 0.325V)

S4 While keep the D- connection with V2, close the Jumper J1. The $V_{BUS}$ jumps to 12V. (because the D+ and D- voltage are between 2V and 0.325V)

S5 Disconnect the D+ with V1. $V_{BUS}$ jumps to 5V (Because the RD quits the QC2.0 and $V_{BUS}$ goes to the default value 5V. start from S1 when needing to enter QC2.0 again)

Figure 3 An Interface-Circuit to Enter Quick Charge 2.0

4 Test Result

4.1 Efficiency

Figure 4 shows the efficiency of the RD at $V_{BUS}$ = 5 V, 9 V and 12 V from 0.1A to full load (Refer the TPS61088 datasheet for more efficiency data of the TPS61088). The efficiency does not just depend on the IC, but also depends on the inductor and the PCB layout. A small DCR inductor and PCB power tracks with small resistance can help to improve the efficiency.
4.2 Thermal Performance

Figure 5 shows the thermal performance at full output power condition when \( V_{\text{IN}} = 3.6 \) V. The ambient temperature \( T_A \) is 23°C and highest temperature point is at the inductor or TPS61088. The worst case happens at \( V_{\text{BUS}} = 12 \) V because of lowest efficiency.
Table 4 summarize the temperature-rise at $V_{BUS}=9V$ and $T_A=23^\circ C$.

<table>
<thead>
<tr>
<th>Different Input Voltage Conditions</th>
<th>$V_{IN}=3V$</th>
<th>$V_{IN}=3.3V$</th>
<th>$V_{IN}=3.6V$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{OUT}=2A$</td>
<td>59.6°C</td>
<td>51.8°C</td>
<td>46.1°C</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Different Output Current Conditions</th>
<th>$V_{IN}=3.6V$</th>
<th>$I_{OUT}=1A$</th>
<th>$I_{OUT}=1.5A$</th>
<th>$I_{OUT}=2A$</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>24.2°C</td>
<td>33.5°C</td>
<td>46.1°C</td>
<td></td>
</tr>
</tbody>
</table>

### 4.3 $V_{BUS}$ Voltage Transition

The voltage’s rising up waveforms from 5V to 9V, 9V to 12V and 5V to 12V are shown in Figure 6, Figure 7, and Figure 8 respectively. The waveforms are measured by changing the D+ and D- voltage level.

There is output voltage overshoot at no load condition. The worst case is 5V to 12V, at which the output voltage could reach 13.2V for a short period. It is caused by the fast transition of $V_{BUS}$ and the power save mode enabled. Make sure the device powered by the circuit can tolerate the voltage overshoot, or apply some load during the transition, or disable the power save mode of the TPS61088 by shorting its MODE pin to ground.
The falling-time from 9 V to 5 V, 12 V to 9 V and 12 V to 5 V at no load condition are shown in Figure 9, the longest falling-time happens at 12-V to 5-V transition which lasts about 120 ms.
4.4 Load Transient

The load transient waveform at 5-V, 9-V and 12-V output voltage are shown in Figure 10 (a), (b) and (c) respectively. The test condition is 25% to 75% to 25% of full load with current slew rate of 0.5A/μs. The load transient waveforms indicate that the designed circuit is stable at the three output voltage condition with enough phase margins.
The overshoot and undershoot of the load transient are summarized in Table 5. More output capacitors can help to reduce the overshoot and undershoot but result in high cost.

<table>
<thead>
<tr>
<th>$V_{BUS}$</th>
<th>5 V</th>
<th>9 V</th>
<th>12 V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Overshoot</td>
<td>550 mV</td>
<td>1 V</td>
<td>1.2 V</td>
</tr>
<tr>
<td>undershoot</td>
<td>650 mV</td>
<td>1 V</td>
<td>1.2 V</td>
</tr>
</tbody>
</table>

### 4.5 Short Circuit Protection

The short circuit protection waveform is shown in Figure 11, where $V_{BST}$ is the output voltage of the boost converter. When the $V_{BUS}$ is short to ground, the E-fuse protects the TPS61088 from damage during the short circuit. The output voltage recovers when the short circuit is removed.

### 4.6 Mobile phone Charging

The setup to charge a mobile phone that supports Quick Charger 2.0 is shown in Figure 12. A cable with a micro-B type male connector is used to link the mobile phone (Samsung Note 4) and the RD. A current probe and a voltage probe are to measure the output current and voltage respectively. The EN pins of the TPS61088 and the TPS2592AA are connected together.
Figure 12 Setup to Charge a Mobile Phone

Figure 13 shows the waveforms of output voltage and current after enabling the RD:

- Firstly, the circuit ramps up to 5V;
- Then, the \( V_{\text{BUS}} \) keeps at 5V for approx. 1.6s. The mobile phone needs this period to enter QC2.0;
- And then the \( V_{\text{BUS}} \) jumps to 9V. No overshoot happens at \( V_{\text{BUS}} \). The load current is not constant because the phone is active.
- Finally the phone is inactive (screen turns off), the charge-power keeps at 9V&1.5A.

Figure 13 Waveform of Charging a Mobile Phone
5 Schematic, Bill of Materials and PCB Layout

5.1 Schematic

Figure 14 shows the schematic of the RD.
### 5.2 Bill of Materials

The bill of materials in the reference design is shown in Table 6.

<table>
<thead>
<tr>
<th>Designator</th>
<th>Quantity</th>
<th>Value</th>
<th>Description</th>
<th>Package</th>
<th>Part Number</th>
<th>Manufacturer</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1</td>
<td>1</td>
<td>22uF</td>
<td>CAP, CERM, 22 µF, 10 V, +/-20%, X5R, 0603</td>
<td>0603</td>
<td>GRM188R61A226ME15D</td>
<td>MuRata</td>
</tr>
<tr>
<td>C2</td>
<td>1</td>
<td>0.01uF</td>
<td>CAP, CERM, 0.01 µF, 50 V, +/-10%, X7R, 0402</td>
<td>0402</td>
<td>GRM155R71H103KA88D</td>
<td>MuRata</td>
</tr>
<tr>
<td>C3</td>
<td>1</td>
<td>2.2uF</td>
<td>CAP, CERM, 2.2 µF, 25 V, +/-10%, X5R, 0402</td>
<td>0402</td>
<td>GRM155R61E225KE11D</td>
<td>MuRata</td>
</tr>
<tr>
<td>C4</td>
<td>1</td>
<td>0.047uF</td>
<td>CAP, CERM, 0.047uF, 10V, +/-10%, X5R, 0402</td>
<td>0402</td>
<td>GRM155R61A473KA01D</td>
<td>MuRata</td>
</tr>
<tr>
<td>C5</td>
<td>1</td>
<td>0.1uF</td>
<td>CAP, CERM, 0.1uF, 16V, +/-10%, X5R, 0402</td>
<td>0402</td>
<td>GRM155R61C104KA88D</td>
<td>MuRata</td>
</tr>
<tr>
<td>C6, C12</td>
<td>2</td>
<td>1uF</td>
<td>CAP, CERM, 1 µF, 25 V, +/-10%, X5R, 0603</td>
<td>0603</td>
<td>GRM188R61E105KA12D</td>
<td>MuRata</td>
</tr>
<tr>
<td>C7, C8, C9</td>
<td>3</td>
<td>22uF</td>
<td>CAP, CERM, 22 µF, 25 V, +/-20%, X5R, 0805</td>
<td>0805</td>
<td>GRM21BR61E226ME44</td>
<td>MuRata</td>
</tr>
<tr>
<td>C10</td>
<td>1</td>
<td>0.22uF</td>
<td>CAP, CERM, 0.22 µF, 10 V, +/-10%, X5R, 0402</td>
<td>0402</td>
<td>GRM155R61A224KE19D</td>
<td>MuRata</td>
</tr>
<tr>
<td>C11</td>
<td>1</td>
<td>100pF</td>
<td>CAP, CERM, 100 pF, 50 V, +/-5%, C0G/NP0, 0402</td>
<td>0402</td>
<td>GRM1535C1H101JDD5D</td>
<td>MuRata</td>
</tr>
<tr>
<td>L1</td>
<td>1</td>
<td>1.5uH</td>
<td>Inductor, Shielded Drum Core, Superflux, 1.5 µH, 11 A, 0.0078 ohm, SMD</td>
<td>WE-HC4</td>
<td>744311150</td>
<td>Wurth Elektronik eiSos</td>
</tr>
<tr>
<td>R1</td>
<td>1</td>
<td>4.7k</td>
<td>RES, 4.7 k, 5%, 0.063 W, 0402</td>
<td>0402</td>
<td>CRCW04024K70JNED</td>
<td>Vishay-Dale</td>
</tr>
<tr>
<td>R2, R11</td>
<td>2</td>
<td>1.00Meg</td>
<td>RES, 1.00 M, 1%, 0.063 W, 0402</td>
<td>0402</td>
<td>CRCW04021M00FKED</td>
<td>Vishay-Dale</td>
</tr>
<tr>
<td>R3, R13</td>
<td>2</td>
<td>100k</td>
<td>RES, 100 kohm, 1%, 0.063W, 0402</td>
<td>0402</td>
<td>CRCW0402100FKFED</td>
<td>Vishay-Dale</td>
</tr>
<tr>
<td>R5</td>
<td>1</td>
<td>316k</td>
<td>RES, 316 k, 1%, 0.063 W, 0402</td>
<td>0402</td>
<td>CRCW0402316FKFED</td>
<td>Vishay-Dale</td>
</tr>
<tr>
<td>R6</td>
<td>1</td>
<td>100k</td>
<td>RES, 100 k, 1%, 0.063 W, 0402</td>
<td>0402</td>
<td>CRCW0402100FKFED</td>
<td>Vishay-Dale</td>
</tr>
<tr>
<td>R7</td>
<td>1</td>
<td>332k</td>
<td>RES, 332 k, 1%, 0.063 W, 0402</td>
<td>0402</td>
<td>CRCW0402332FKFED</td>
<td>Vishay-Dale</td>
</tr>
<tr>
<td>R8</td>
<td>1</td>
<td>95.3k</td>
<td>RES, 95.3 k, 1%, 0.063 W, 0402</td>
<td>0402</td>
<td>CRCW040295K3FKED</td>
<td>Vishay-Dale</td>
</tr>
<tr>
<td>R9, R12</td>
<td>2</td>
<td>127k</td>
<td>RES, 127 k, 1%, 0.063 W, 0402</td>
<td>0402</td>
<td>CRCW0402127FKFED</td>
<td>Vishay-Dale</td>
</tr>
<tr>
<td>R10</td>
<td>1</td>
<td>3.01k</td>
<td>RES, 3.01 k, 1%, 0.063 W, 0402</td>
<td>0402</td>
<td>CRCW0402301FKFED</td>
<td>Vishay-Dale</td>
</tr>
<tr>
<td>R14</td>
<td>1</td>
<td>390k</td>
<td>RES, 390 k, 5%, 0.063 W, 0402</td>
<td>0402</td>
<td>CRCW0402390JKJNED</td>
<td>Vishay-Dale</td>
</tr>
<tr>
<td>U1</td>
<td>1</td>
<td>13.2V Output, Synchronous Boost Converter with 10-A Switch, RHL0020A</td>
<td>RHL0020A</td>
<td>TPS61088RHLR</td>
<td>Texas Instruments</td>
<td></td>
</tr>
<tr>
<td>U2</td>
<td>1</td>
<td>12V eFuse with Integrated Blocking FET Driver, Auto Retry, DRC0010J</td>
<td>DRC0010J</td>
<td>TPS2592AADRC</td>
<td>Texas Instruments</td>
<td></td>
</tr>
<tr>
<td>U3</td>
<td>1</td>
<td>CHY100</td>
<td></td>
<td></td>
<td>Power Integrations</td>
<td></td>
</tr>
</tbody>
</table>
5.3 PCB Layout

Figure 15 and Figure 16 show the layout of the reference design. The bulk output capacitor is far away from the TPS61088, so a small package output capacitor C6 is placed near the IC and connected with short track to reduce the voltage spike at SW pin. The copper for the thermal pad of the TPS61088 should be as large as possible to reduce the temperature-rise caused by the power loss.

![Figure 15 PMP9773 Top Overlay, Top Layer and Top Paste](image)

![Figure 16 PMP9773 Bottom Overlay and Bottom Layer](image)
IMPORTANT NOTICE FOR TI REFERENCE DESIGNS

Texas Instruments Incorporated (“TI”) reference designs are solely intended to assist designers (“Buyers”) who are developing systems that incorporate TI semiconductor products (also referred to herein as “components”). Buyer understands and agrees that Buyer remains responsible for using its independent analysis, evaluation and judgment in designing Buyer’s systems and products.

TI reference designs have been created using standard laboratory conditions and engineering practices. TI has not conducted any testing other than that specifically described in the published documentation for a particular reference design. TI may make corrections, enhancements, improvements and other changes to its reference designs.

Buyers are authorized to use TI reference designs with the TI component(s) identified in each particular reference design and to modify the reference design in the development of their end products. HOWEVER, NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY THIRD PARTY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT, IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI REFERENCE DESIGNS ARE PROVIDED “AS IS”, TI MAKES NO WARRANTIES OR REPRESENTATIONS WITH REGARD TO THE REFERENCE DESIGNS OR USE OF THE REFERENCE DESIGNS, EXPRESS, IMPLIED OR STATUTORY, INCLUDING ACCURACY OR COMPLETENESS. TI DISCLAIMS ANY WARRANTY OF TITLE AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, QUIET ENJOYMENT, QUIET POSSESSION, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS WITH REGARD TO TI REFERENCE DESIGNS OR USE THEREOF. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY BUYERS AGAINST ANY THIRD PARTY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON A COMBINATION OF COMPONENTS PROVIDED IN A TI REFERENCE DESIGN. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, SPECIAL, INCIDENTAL, CONSEQUENTIAL OR INDIRECT DAMAGES, HOWEVER CAUSED, ON ANY THEORY OF LIABILITY AND WHETHER OR NOT TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES, ARISING IN ANY WAY OUT OF TI REFERENCE DESIGNS OR BUYER’S USE OF TI REFERENCE DESIGNS.

TI reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques for TI components are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

Reproduction of significant portions of TI information in TI data books, data sheets or reference designs is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards that anticipate dangerous failures, monitor failures and their consequences, lessen the likelihood of dangerous failures and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in Buyer’s safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed an agreement specifically governing such use.

Only those TI components that TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components that have not been so designated is solely at Buyer’s risk, and Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2015, Texas Instruments Incorporated