TI Designs – Precision: Verified Design
Instrumentation Amplifier with DC Rejection Reference Design

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Design Resources
Design Archive
TINA-TI™
INA128
OPA188

Circuit Description
This design is an ac coupled instrumentation amplifier. More specifically, the circuit amplifies ac differential input signals and rejects dc differential and common mode signals. The input is dc coupled, so it achieves effective ac coupling by shifting the instrumentation amplifier reference voltage to cancel output offset.

Art Kay

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Design Summary

The design requirements are as follows:

- Supply Voltage: ±15 V
- Input: small ac input with large dc offset (0 to 1Vpk with -10V to +10V dc offset).
- Output ac coupled

The design goals and performance are summarized in Table 1. Figure 1 depicts the measured and simulated ac transfer characteristic of the design.

### Table 1. Comparison of Design Goals, Simulation, and Measured Performance

<table>
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<tr>
<th>Goal</th>
<th>Calculated</th>
<th>Simulated</th>
<th>Measured</th>
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<tr>
<td>$f_L$</td>
<td>16Hz</td>
<td>16Hz</td>
<td>16Hz</td>
</tr>
<tr>
<td>$f_H$</td>
<td>1MHz</td>
<td>1.3MHz</td>
<td>1.12MHz</td>
</tr>
</tbody>
</table>

Figure 1: Simulated and Measured Transfer Function
1 Theory of Operation

Figure 2 shows the schematic of the instrumentation amplifier with dc rejection. This TI Design behaves very similar to any ac coupled circuit in that the dc signal is rejected and the ac signal is passed. The ac transfer characteristic even looks the same as other ac coupled circuits as it has a lower cutoff frequency and a pass band. The main difference is that this circuit does not use large coupling capacitors on the input to ac couple the signal. Rather, the input is dc coupled and the output dc average is eliminated by integrating the output and subtracting the dc average using the reference pin. In section 6.1 we will cover some advantages of this method of ac coupling as compared to the capacitive input coupling method.

Notice in Figure 2 that the integrator (U2) is an inverting integrator. Also, remember that the integral of a sinusoidal wave is zero where as the integral of a dc constant is a ramp function. This circuit will cause the output of U2 to servo to a dc constant voltage that will cancel the output dc offset voltage on this circuit. You can think of the integrator as a low pass filter that translates the instrumentation amplifier into a high pass by canceling the dc and low frequency components on the circuit’s output (see reference 2).

Figure 2: Single Supply ac Coupled Amplifier
1.1 Setting ac Response – Cutoff Frequencies

The input RC network $R_8$ and $C_{10}$ set the lower cutoff frequency for the circuit. Equation (1) gives the general relationship for the lower cutoff frequency. In this example the cutoff is set to 16Hz. For most applications it is desirable to set $f_L$ as low as possible. Increasing $R_8$ or $C_{10}$ will decrease this frequency further, but this will also increase the transient startup for this circuit.

$$f_L = \frac{1}{2\pi R_8 C_{10}} \frac{1}{2\pi (100k\Omega)(100nF)} = 16\text{Hz} \quad (1)$$

The upper cutoff frequency is set by the bandwidth of the instrumentation amplifier (U1). The data sheet for the INA128 specification table provides bandwidth information for different closed loop gains (in this case $f_H = 1.3\text{MHz}$). Figure 3 shows the position of the upper and lower cutoff frequency on the frequency response curve.

$$f_H = 1.3\text{MHz} \quad (2)$$

![Figure 3: Lower and upper cutoff frequency shown on ac transfer characteristic](image)
2 Component Selection

2.1 Op Amp and Instrumentation Amplifier

The OPA188 was selected for its dc precision. Any offset on the OPA188 will directly appear as an error source on the output. The INA128 was selected for its excellent gain accuracy, low gain drift, low noise, and common mode rejection. This device also has very good dc accuracy, but that is not required in this application as the circuit is ac coupled.

2.2 Passive Components

This design uses 1% thin film resistors and X7R ceramic capacitors. Special low distortion capacitors (C0G) are not practical as a large capacitance value is normally needed for \( C_{10} \). It is recommended to choose a best voltage coefficient possible for this capacitor type to minimize shifting \( C_{10} \) versus dc voltage. Shifting of \( C_{10} \) will cause shifting of the lower cutoff frequency. Note that for a fixed voltage level, capacitors with higher voltage ratings are generally less sensitive to changes in dc voltage. For example, for a 10Vdc applied voltage, a capacitor with a 50V rating is less sensitive than a capacitor with a 25V rating. For this reason, \( C_{10} \) was selected with a 50V rating. Also, a "soft termination" type capacitor was used as this is less sensitive to microphonics (variations in capacitance due to vibration).
3 Simulation

3.1 Transfer Function

The simulated and measured response vs frequency is shown in Figure 4. As mentioned in section 1.1, the lower cutoff frequency is set by input coupling capacitor C10 and input resistor R8. The upper cutoff frequency is set by the instrumentation amplifiers bandwidth limitation. The simulation and measurement results for both the upper and lower cutoff frequencies match well.

![Measured vs. Simulated Freq. Response](image)

Figure 4: Frequency response for INA118 and OPA188 dc rejection circuit
3.2 Transient – Startup

The simulation below shows the startup condition with the input source set to 1Vpk @1kHz +10Vdc. Notice that the output of the integrator ramps to cancel the dc offset on the ac signal. After the initial startup transient, the output will track the ac signal and reject the dc offset.

![Startup transient diagram]

**Figure 5: Startup Transient Integrator Ramping to Cancel Output Offset**

3.3 Transient – Steady State

The simulation below shows the steady state response for 1Vpk @ 1kHz +10Vdc signal.

![Steady state transient diagram]

**Figure 6: Steady State Transient to 1Vpk+10Vdc 1kHz Input Signal**
4 PCB Design

Note that this PCB includes both the inverting and non-inverting ac coupled amplifier. The PCB schematic and bill of materials can be found in the Appendix.

4.1 PCB Layout

Normal PCB layout precautions were in this layout (i.e. short traces, solid ground connections, minimized vias, close decoupling capacitors).

![PCB Layout](image)

Figure 7: PCB Layout (Top - Red, Bottom - Blue)
5 Verification & Measured Performance

5.1 Transfer Function

The measured and simulated ac transfer function is compared to each other in section 3.1. The measured results compare well with the simulations.

5.2 Transient – Steady State

Figure 8 shows the steady state response to a 1Vpk @ 1kHz +10Vdc sinusoidal waveform. The input is multiplied by a gain of one and the dc offset is eliminated. Thus, the output signal is 1Vpk @ 1kHz ac signal with no offset.

Figure 8: Transient Response to a 1Vpk 1kHz + 10Vdc Input Signal
6 Modifications

Depending on your design goal you may choose different values.

<table>
<thead>
<tr>
<th>Design Goal</th>
<th>Modification</th>
<th>Trade off</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lower low cutoff frequency</td>
<td>Increase R1 x C1</td>
<td>This will increase transient start up time.</td>
</tr>
<tr>
<td>Upper cutoff frequency</td>
<td>Choose an instrumentation amplifier with wider bandwidth</td>
<td>Wider bandwidth devices normally draw more current.</td>
</tr>
<tr>
<td>Gain</td>
<td>Select a value of the gain setting resistor (R4 on the schematic in Appendix A.1). Gain = 50kΩ ( \frac{1}{R_4} + 1 )</td>
<td>The amount of dc offset that be corrected is impacted by the gain. Large gain, means that less dc offset correction is achievable. As a good estimate for dc correction, the dc correction range by the gain for higher gains.</td>
</tr>
</tbody>
</table>

Gain | dc correction range |
---|---------------------|
1V/V | ±10Vdc |
10V/V | ±1Vdc |
100V/V | ±0.1Vdc |
1000V/V | ±0.01Vdc |
6.1 Alternative Implementation – Some Tradeoffs

Another ac coupled instrumentation amplifier implementation is shown in Figure 9. This circuit only requires two input coupling capacitors and two input resistors (1µF and 1MΩ in this example). Because of its simplicity, one may initially choose this implementation; however, it has a significant disadvantage over the approach covered in this TI Design. The key disadvantage to circuit shown in Figure 9 is that it translates common mode signals into differential signals. Note that the input capacitors have a tolerance between 1% and 10%, so the mismatch can be significant. This mismatch will effectively translate low frequency common mode signals into low frequency differential signals. One example where this can be especially problematic is ECG signals. In this case the common mode noise (e.g. 60Hz power line pick-up) is in the same frequency range as the measured signal. In this example it is very important that the low frequency common mode signal is rejected. The circuit from this TI Design (Figure 2) has a dc coupled input so that it does not translate common mode signals to differential signals. The circuit shown in Figure 9, on the other hand, will translate common mode noise to differential noise.

![Figure 9: ac Coupled with Input Capacitors Error Source - Common Mode to Differential Translation](image-url)

Capacitor mismatch translates common mode to differential

+15V

-15V

1µF

1µF

1MΩ

1MΩ

Rg

Rg

Vout

INA128

Vcm

Ref

Figure 9: ac Coupled with Input Capacitors Error Source - Common Mode to Differential Translation
7 About the Author

Arthur Kay is an applications engineering manager at TI where he specializes in the support of amplifiers, references, and mixed signal devices. Arthur focuses a good deal on industrial applications such as bridge sensor signal conditioning. Arthur has published a book and an article series on amplifier noise. Arthur received his M.S.E.E. from Georgia Institute of Technology, and B.S.E.E. from Cleveland State University.

8 Acknowledgements & References


Appendix A.

A.1 Electrical Schematic

Figure A-1: Electrical Schematic

Note: the schematic allows for many options that are not used in this TI Design. In some cases components may not be installed, or may have a value different than what is shown in the schematic. Refer, to the bill of material for component values.
## A.2 Bill of Materials

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<th>Designator</th>
<th>Description</th>
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<td>INA118U</td>
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<td>B&amp;F Fastener Supply</td>
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