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Load Switches for Power MUXing and Reverse Current Blocking Design Guide

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Design Resources

TIDA-00514  Tool Folder Containing Design Files
TPS22959  Product Folder
CSD13381F4  Product Folder
TPS22959EVM-079  Product Folder

Design Features

• Control Power Multiplexing (MUX) With A Single GPIO Control Signal
• Optimized RC Circuit Ensures Make-Before-Break Logic For A Seamless Switch Over
• Configure Single-Switch Direction For Various Levels Of Reverse Current Blocking
• Includes Back-to-Back Switch Configuration For Bi-Directional Current Blocking

Featured Applications

• Servers
• Enterprise Computing
• Medical
• Telecom Systems
• Industrial Systems
• High Current Voltage Rails

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1 System Description

The functionality of existing load switches can be expanded by using them in the reverse configuration to block reverse current. This TI design demonstrates two examples of using load switches in the reverse configuration.

1.1 Forward vs. Reverse Switch Configuration

Typically, a load switch is used to control current only in the forward direction from a power supply to a load. This is because a single MOSFET can only block current in one direction due to the intrinsic body diode. However, some applications require blocking current in the reverse direction. In this case, a load switch can be used in the reverse direction for an ideal diode function. Table 1 summarizes the differences between the forward and reverse configuration.

<table>
<thead>
<tr>
<th>FEATURES:</th>
<th>FEATURES:</th>
</tr>
</thead>
<tbody>
<tr>
<td>Blocks forward current when disabled</td>
<td>Blocks reverse current when disabled</td>
</tr>
<tr>
<td>Very low ON resistance when enabled</td>
<td>Very low ON resistance when enabled</td>
</tr>
<tr>
<td>Does not block reverse current</td>
<td>Does not block forward current</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>APPLICATIONS:</th>
<th>APPLICATIONS:</th>
</tr>
</thead>
<tbody>
<tr>
<td>Shutdown load for power savings</td>
<td>Reverse current blocking</td>
</tr>
<tr>
<td>Power sequencing</td>
<td>Power MUXing</td>
</tr>
<tr>
<td>Inrush current control</td>
<td></td>
</tr>
</tbody>
</table>

1.2 Make-Before-Break 2:1 Power Multiplexer (MUX)

The first circuit featured in this design is a make-before-break 2:1 power MUX using two TPS22959 in the reverse configuration. The make-before-break logic ensures a seamless transition between the two power supplies by turning on the second switch before the first switch is turned off. This configuration can only be used in applications where the main and standby voltages are the same in order to prevent reverse current flow when both switches are on.
1.2.1 Key Specifications

Table 2. Key Specifications

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SPECIFICATION</th>
<th>DETAILS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum continuous output current</td>
<td>15 A</td>
<td>Maximum continuous current rating of TPS22959</td>
</tr>
<tr>
<td>Typical ON resistance</td>
<td>4.4 mΩ</td>
<td>See Section 4.2</td>
</tr>
<tr>
<td>Switch over time</td>
<td>&lt;20 ms</td>
<td>See Section 7.1 and Section 7.2</td>
</tr>
</tbody>
</table>
1.2.2 Alternate Configurations

Resistors R41, R47, and R48 can configure the main and standby switches into the forward or reverse direction. Each resistor represents a different case, and only one should be installed at a time. None of these resistors are needed in the final design, and the chosen resistor can be replaced by a wide PCB trace to further reduce power dissipation and voltage drop. This design guide highlights the case where both switches are in the reverse configuration (R48 installed) for reverse current blocking on both power supplies. In cases where one supply is always available or reverse current is not a concern, the forward configuration may be preferred.

Table 3. Alternate Power MUX Switch Configurations

<table>
<thead>
<tr>
<th>INSTALL</th>
<th>MAIN POWER SWITCH (U41)</th>
<th>STANDBY POWER SWITCH (U42)</th>
<th>LOAD CONNECTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>R48</td>
<td>Reverse Configuration</td>
<td>Reverse Configuration</td>
<td>Connectors J42</td>
</tr>
<tr>
<td></td>
<td>Input Connector J41</td>
<td>Input Connector J43</td>
<td>and J44</td>
</tr>
<tr>
<td>R47</td>
<td>Reverse Configuration</td>
<td>Forward Configuration</td>
<td>Connectors J42</td>
</tr>
<tr>
<td></td>
<td>Input Connector J41</td>
<td>Input Connector J44</td>
<td>and J43</td>
</tr>
<tr>
<td>R41</td>
<td>Forward Configuration</td>
<td>Forward Configuration</td>
<td>Connectors J41</td>
</tr>
<tr>
<td></td>
<td>Input Connector J42</td>
<td>Input Connector J44</td>
<td>and J43</td>
</tr>
</tbody>
</table>

Refer to Section 9.1 for resistor placement.

All configurations can make use of the make-before-break circuitry by using jumper J41 or J44 to connect power to this circuit from an available power supply. Using jumper J41 or J44 provides an identical control scheme regardless of configuration, but the RC delay is dependent upon input voltage.

1.3 Back-to-Back Configuration for Bi-Directional Current Blocking

The second circuit uses two TPS22959 in a back-to-back configuration for bi-directional current blocking up to 15 A.
1.3.1 Key Specifications

Table 4. Key Specifications

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SPECIFICATION</th>
<th>DETAILS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum continuous output current</td>
<td>15 A</td>
<td>Maximum continuous current rating of TPS22959</td>
</tr>
<tr>
<td>Typical ON resistance</td>
<td>8.8 mΩ</td>
<td>See Section 4.2 and Section 8.2</td>
</tr>
<tr>
<td>Maximum reverse leakage current</td>
<td>0.5 µA</td>
<td>See Section 8.1</td>
</tr>
</tbody>
</table>

2 Block Diagram

The block diagram for the TPS22959 load switch in these designs is shown in Figure 3.

![Figure 3. TPS22959 Functional Block Diagram](image)
3  Highlighted Products

3.1  TPS22959
- Integrated Single Channel Load Switch
- $V_{\text{BIAS}}$ Voltage Range: 2.5 V to 5.5 V
- $V_{\text{IN}}$ Voltage Range: 0.8 V to 5.5 V
- Ultra Low $R_{\text{ON}}$ Resistance
  - $R_{\text{ON}} = 4.4 \text{ m\Omega} \text{ at } V_{\text{IN}} = 5 \text{ V (} V_{\text{BIAS}} = 5 \text{ V)}$
- 15-A Maximum Continuous Switch Current
- Low Quiescent Current (20 μA for $V_{\text{BIAS}} = 5 \text{ V}$)
- Low Shutdown Current (1 μA for $V_{\text{BIAS}} = 5 \text{ V}$)
- Low Control Input Threshold Enables Use of 1.2 V or Higher GPIO
- Controlled and Fixed Slew Rate Across $V_{\text{BIAS}}$ and $V_{\text{IN}}$
  - $t_{\text{q}} = 2663 \text{ ms at } V_{\text{IN}} = 5 \text{ V (} V_{\text{BIAS}} = 5 \text{ V)}$
- Quick Output Discharge (QOD)
- SON 8-Terminal Package with Thermal Pad
- Pin-to-pin with TPS22962 (10-A Maximum Continuous Switch Current)
- Pin-to-pin with TPS22969 (6-A Maximum Continuous Switch Current)

3.2  CSD13381F4
- Low On-Resistance
- Low $Q_g$ and $Q_{gd}$
- Low Threshold Voltage
- Ultra-Small Footprint (0402 Case Size)
  - 1.0 mm x 0.6 mm
- Ultra-Low Profile
  - 0.35 mm Height

4  System Design Theory
The functionality of existing load switches can be expanded by using them in the reverse configuration to block reverse current. This section will discuss the key features of the reverse configuration.

4.1  Reverse Current Blocking
When a load switch is placed in the reverse configuration, the intrinsic body diode will face towards the load. If the load voltage is higher than the input voltage, the body diode will remain reverse biased and will not allow reverse current to flow.

4.2  Total ON-Resistance ($R_{\text{ON}}$)
Placing two switches in the series back-to-back configuration will double the total ON Resistance. Using a single switch in the reverse configuration to block current will minimize the total ON resistance and $V = IR$ voltage drop.
4.3 Make-Before-Break Timing Circuit

Figure 4 shows the timing circuit to implement make-before-break logic when switching both from main to standby and from standby to main.

![Diagram of Make-Before-Break RC Timing Circuit]

Figure 4. Make-Before-Break RC Timing Circuit
When Select goes low, Enable A is slowly charged up to the standby voltage (5 V in this case). Enable B follows Enable A through a resistor divider. The RC delay and resistor divider offset allow for Switch A to be enabled before Switch B is disabled.

The following equations can be used to find the voltages at each of the enables during charging.

\[
\text{Enable } A(t) = V_{\text{stby}} \times \frac{R1 + R2 + 100k\Omega}{R1 + R2 + 100k\Omega + 10k\Omega} \times \left(1 - e^{\frac{-t}{(10k\Omega + 100k\Omega) \cdot C_{\text{delay}}}}\right)
\]

\[
\text{Enable } B(t) = \frac{R2}{R1 + R2} \times \text{Enable } A(t)
\]
When Select goes high, Enable A is slowly discharged down to GND. Enable B follows Enable A through a resistor divider. The RC delay and resistor divider offset allow for Switch B to be enabled before Switch A is disabled.

![Figure 6. RC Timing Circuit Discharging](image)

The discharge time will always be less than the charge time because less resistance occurs in a series with the $C_{\text{delay}}$ capacitor. Because of this, it is recommended that $R_1 + R_2 \geq 1\, \text{M}\Omega$ to minimize the time difference between charging and discharging cycles. Furthermore, the shorter discharge time should be used to set the $C_{\text{delay}}$ value. The turn-off delay in Figure 6 should be greater than the turn-on delay of the load switch.

The $R_1 / R_2$ resistor ratio should be set so that Enable B will always surpass the threshold when charging. A lower threshold will allow a higher resistor-divider ratio and minimize the required switch-over delay. The CSD13381F4 FemtoFET™ was specifically chosen for this design because of its small size and low threshold voltage.

Note that in this design, Enable A is controlling the Main Power Supply Switch, and Enable B is controlling the Standby Power Supply Switch. When Select is Low, the main supply will power the load. When Select is High, the standby supply will power the load. The Select logic can be reversed simply by swapping the Main- and Standby-Power Supply connections. Just be sure the make-before-break timing circuit and $V_{\text{BIAS}}$ supplies have power.

The following equations can be used to find the voltages at each of the enables during discharge.

$$\text{Enable A}(t) = \frac{V_{\text{stby}} \times R_1 + R_2 + 100k\Omega}{R_1 + R_2 + 100k\Omega + 10k\Omega} \times e^{-t\left(\frac{1}{100k\Omega} \cdot \frac{1}{R_1 + R_2}\right)^{-1} \times C_{\text{delay}}}}$$  \hspace{1cm} (3)

$$\text{Enable B}(t) = \frac{R_2}{R_1 + R_2} \times \text{Enable A}(t)$$  \hspace{1cm} (4)
5 Getting Started Hardware

5.1 Make-Before-Break 2:1 Power MUX Connections and Test Points

The connections and test points for the make-before-break power MUX (with R48 installed) are summarized in Table 5:

Table 5. Power MUX Circuit Connections and Test Points

<table>
<thead>
<tr>
<th>CONNECTION</th>
<th>NAME</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>J41</td>
<td>Main power input</td>
<td>DC Input to main power switch</td>
</tr>
<tr>
<td>J42, J44</td>
<td>$V_{\text{load}}$</td>
<td>Load connection</td>
</tr>
<tr>
<td>J43</td>
<td>Standby power input</td>
<td>DC Input to standby power switch</td>
</tr>
<tr>
<td>JP41, JP44</td>
<td>make-before-break circuit power rail selection</td>
<td>Connects make-before-break circuit power to one of the four power connectors J41, J42, J43, or J44</td>
</tr>
<tr>
<td>JP42</td>
<td>Switch control</td>
<td>Power supply connection</td>
</tr>
<tr>
<td>JP43</td>
<td>$V_{\text{BIAS}}$ power</td>
<td>Option $V_{\text{BIAS}}$ connection to make-before-break circuit power rail</td>
</tr>
<tr>
<td>TP41</td>
<td>Main power sense</td>
<td>Sense connection to main power switch</td>
</tr>
<tr>
<td>TP52</td>
<td>$V_{\text{load}}$ sense</td>
<td>Sense connection to the switches’ output</td>
</tr>
<tr>
<td>TP43</td>
<td>Standby power sense</td>
<td>Sense connection to standby power switch</td>
</tr>
<tr>
<td>TP45</td>
<td>make-before-break circuit power rail</td>
<td>Connection for external power to make-before-break circuit power rail</td>
</tr>
<tr>
<td>TP47</td>
<td>$V_{\text{ON, Main}}$</td>
<td>Sense connection for main switch enable</td>
</tr>
<tr>
<td>TP48</td>
<td>$V_{\text{ON, Standby}}$</td>
<td>Sense connection for standby switch enable</td>
</tr>
<tr>
<td>TP45</td>
<td>Make-before-break circuit power rail</td>
<td>Connection for external power to make-before-break circuit power rail</td>
</tr>
<tr>
<td>TP46</td>
<td>Inverter input</td>
<td>Sense connection for input to NMOS inverter</td>
</tr>
<tr>
<td>TP49</td>
<td>$V_{\text{BIAS}}$ power</td>
<td>Connection for external power to $V_{\text{BIAS}}$</td>
</tr>
<tr>
<td>TP32, TP36, TP37, TP38</td>
<td>GND</td>
<td>Connection to board ground</td>
</tr>
</tbody>
</table>

5.2 Back-to-Back Circuit Connections and Test Points

The connections and test points for the back-to-back TPS22959 circuit are summarized in Table 6:

Table 6. Back-to-Back Circuit Connections and Test Points

<table>
<thead>
<tr>
<th>CONNECTION</th>
<th>NAME</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>J11</td>
<td>$V_{\text{IN}}$</td>
<td>DC Input to $V_{\text{IN}}$</td>
</tr>
<tr>
<td>J12</td>
<td>$V_{\text{OUT}}$</td>
<td>Load connection for $V_{\text{OUT}}$</td>
</tr>
<tr>
<td>JP12</td>
<td>$V_{\text{BIAS}}$ power</td>
<td>Connects $V_{\text{BIAS}}$ to $V_{\text{IN}}$</td>
</tr>
<tr>
<td>JP11</td>
<td>ON control</td>
<td>Connects ON pin to $V_{\text{IN}}$ or GND</td>
</tr>
<tr>
<td>TP11</td>
<td>$V_{\text{IN}}$ sense</td>
<td>Sense connection to $V_{\text{IN}}$</td>
</tr>
<tr>
<td>TP16</td>
<td>$V_{\text{OUT}}$ sense</td>
<td>Sense connection to $V_{\text{OUT}}$</td>
</tr>
<tr>
<td>TP14</td>
<td>$V_{\text{BIAS}}$</td>
<td>$V_{\text{BIAS}}$ connection</td>
</tr>
<tr>
<td>TP13</td>
<td>ON</td>
<td>Enable connection</td>
</tr>
<tr>
<td>TP12, TP17, TP18, TP19</td>
<td>GND</td>
<td>Connection to board ground</td>
</tr>
</tbody>
</table>
6 Test Setup

This section shows the test setup for both the make-before-break 2:1 Power MUX circuit as well as the back-to-back TPS22959 circuit.

6.1 Make-Before-Break 2:1 Power MUX Test Setup

Figure 7 shows the test points for the power MUX waveform collection:

![Power MUX Waveform Setup Diagram](image-url)

Figure 7. Power MUX Waveform Setup
6.2 Back-to-Back Circuit Reverse Current Blocking Test Setup

Figure 8 shows the proper test setup for measuring the reverse leakage current through the back-to-back load switches when they are disabled:

![Figure 8. Back-to-Back Reverse Current Blocking Test Setup](image)

6.3 Back-to-Back Circuit ON Resistance Test Setup

Figure 9 shows the proper test setup for measuring the ON resistance of the back-to-back TPS22959 circuit:

![Figure 9. Back-to-Back Circuit ON Resistance Test Setup](image)
7 Make-Before-Break 2:1 Power MUX Test Data

This section will cover the test data from the power MUX circuit.

7.1 Switching Waveforms (5 V)

The following waveforms show the switch-over waveforms when both main and standby are at 5 V. During switching, the make-before-break logic allows the current to be temporarily shared between the two supplies to ensure a seamless switch over.

![Switching from Main to Standby (5 V)](image1)

![Switching from Standby to Main (5 V)](image2)

Because very little overlap occurs when switching from standby to main, the $C_{\text{delay}}$ capacitor should not be reduced from 330 nF to prevent a dip in the load voltage when switching.
7.2 Switching Waveforms (3.3 V)

The following waveforms show the switch-over waveforms when both main and standby are at 3.3 V. During switching, the make-before-break logic allows the current to be temporarily shared between the two supplies to ensure a seamless switch over.

Figure 12. Switching from Main to Standby (3.3 V)

Figure 13. Switching from Standby to Main (3.3 V)

Because at least 10 ms of overlap occurs when switching from main to standby and from standby to main, the $C_{\text{delay}}$ capacitor could be reduced from 330 nF for a faster switchover. This reduction would not be possible in the 5-V case because very little overlap occurs when switching from standby to main.
8 Back-to-Back Circuit Test Data

This section will cover the test data from the back-to-back TPS22959 circuit.

8.1 Reverse Leakage Current

Figure 14 shows the reverse leakage current through the back-to-back load switches when they are disabled.

![Figure 14. Back-to-Back Circuit Reverse Leakage Current](image)

8.2 ON Resistance versus Load Current

Figure 15 summarizes the ON resistance measured at various loads:

![Figure 15. Back-to-Back Circuit ON Resistance versus Load Current](image)
9 Design Files

9.1 Schematics

To download the Schematics, see the design files at TIDA-00514.

![Figure 16. Make-Before-Break 2:1 Power MUX Schematic](image1)

![Figure 17. Back-to-Back TPS22959 Schematic](image2)

9.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00514.

9.3 PCB Layout Recommendations

For best performance, all traces should be as short as possible. To be most effective, the input and output capacitors should be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for $V_{IN}$, $V_{OUT}$, and GND helps minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance.
9.4 Layout Prints
To download the layout prints, see the design files at TIDA-00514.

9.5 Gerber Files
To download the Gerber files, see the design files at TIDA-00514.

9.6 Assembly Drawings
To download the assembly drawings, see the design files at TIDA-00514.

10 References
1. Load Switch Thermal Considerations App Report (SLVUA74)
About the Author

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