**TI Designs**

**Universal Sensor IF SAR BoosterPack**

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**TI Designs**

This TI Design showcases an SAR ADC BoosterPack™ for TI LaunchPad™ suitable for different sensors, in particular the ones with low output voltage range and high output impedance.

**Design Resources**

- TIDA-00564 Design Folder
- ADS8320 Product Folder
- REF5030 Product Folder
- LMP7716 Product Folder

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**Design Features**

- Physical Form Factor in BoosterPack for Compatibility With All TI LaunchPads
- Scalable From Generic to Specific Evaluation Within Minutes
- Low-Input Referred Noise and Low-Input Bias Current Suitable
- 16-Bit SAR ADC: ADS8320
- Ideal Choice for High-Impedance Output Sensors

**Featured Applications**

- Factory Automation and Process Control
- Sensors And Field Transmitters

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1 System Overview

1.1 System Description

This TI Design is a universal sensor IF based on a successive approximation register (SAR) ADC built in a BoosterPack form factor to be easily connected to TI LaunchPad for development and testing. The analog front end (AFE) of the board has been designed for sensors with low output voltage range and high output impedance such as thermopiles, infrared (IR) thermometers, thermocouple amplifiers, pH electrode buffers, piezoelectric accelerometers, and many others.

1.2 Key System Specifications

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2 Block Diagram

Figure 1. Block Diagram
2.1 **Highlighted Products**

For more information on each of these devices, see their respective product folders at [www.ti.com](http://www.ti.com).

2.1.1 **ADS8320: High-Speed ADC**

Features:
- 100-kHz sampling rate
- Micropower:
  - 3.8 mW at 100 kHz and 2.7 V
  - 0.3 mW at 10 kHz and 2.7 V
- Power down: 6 µA max
- 8-Pin ceramic package
- Pin compatible to ADS7816 and ADS7822
- SPI

![Figure 2. ADS8320 Functional Block Diagram](image-url)
2.1.2 REF5030: Voltage Reference

- Low temperature drift:
  - High-grade: 3 ppm/°C (max)
  - Standard-grade: 8 ppm/°C (max)
- High accuracy:
  - High-grade: 0.05% (max)
  - Standard-grade: 0.1% (max)
- Low noise: 3 μVpp/V
- Excellent long-term stability:
  - 45 ppm/1000 hr (typ) after 1000 hours
- High output current: ±10 mA
- Temperature range: −40°C to 125°C

![Block Diagram](image-url)

Figure 3. REF5030 Simplified Block Diagram

2.1.3 LMP7716: Low-Noise Amplifier

Features:

- Unless otherwise noted, typical values at \( V_S = 5 \text{ V} \):
  - Input offset voltage: ±150 μV (Max)
  - Input bias current: 100 fA
  - Input voltage noise: 5.8 nV/√Hz
  - Gain bandwidth product: 17 MHz
  - Supply current (LMP7715): 1.15 mA
  - Supply current (LMP7716/LMP7716Q): 1.30 mA
  - Supply voltage range: 1.8 to 5.5 V
  - THD+N at f = 1 kHz 0.001%
  - Operating temperature range: −40°C to 125°C
  - Rail-to-rail output swing
  - Space saving SOT-23 package (LMP7715)
  - 8-Pin VSSOP package (LMP7716/LMP7716Q)
  - LMP7716Q is AEC-Q100 Grade 1 qualified and is manufactured on an automotive grade flow
3 System Design Theory

The analog front-end (AFE) circuitry has to be carefully designed to reduce the noise and increase the sensitivity of the system.

First, determine how the input signal’s bandwidth and full scale range. Next, when selecting the ADC, the device must match the bandwidth of the input signal per Nyquist. This device should also have an appropriate resolution for our signal.

Once the ADC is selected, determine the values of the external input capacitance and input resistance. The quality of the capacitor is critical to avoid distortion generated by the circuit. The value of the capacitor ensures the ADC will have ample charge for each conversion while the value of the resistor ensures that the operational amplifier will be stable.

To select an operational amplifier, determine what style of the input stage is needed. Also select an amplifier that has ample bandwidth for the input signal.

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Figure 4. Analog Front End (AFE)
3.1 SAR ADC

3.1.1 SAR Theory of Operation

The successive approximation converter performs a binary search through all possible quantization levels before converging on the final digital answer. See Figure 5 for the block diagram. An N-bit register controls the timing of the conversion where N is the resolution of the ADC. VIN is sampled and compared to the output of the DAC. The comparator output controls the direction of the binary search, and the output of the SAR is the actual digital conversion. The successive approximation algorithm is as follows [3].

![SAR Block Diagram](image-url)

Figure 5. SAR Block Diagram
3.1.2 Sample-and-Hold

Sample-and-hold (S/H) circuits are critical in converting analog signals to digital signals. The behavior of the S/H is analogous to that of a camera. Its main function is to "take a picture" of the analog signal and hold its value until the ADC can process the information. It is important to characterize the S/H circuit when performing data conversion. Ignoring this component can result in serious error for both speed and accuracy can be limited by the S/H. Ideally, the S/H circuit should have an output similar to that shown in Figure 6. Here, the analog signal is instantly captured and held until the next sampling period. However, a finite period of time is required for the sampling to occur. During the sampling period, the analog signal may continue to vary; therefore, another type of circuit is called a track-and-hold (T/H). Here, the analog signal is "tracked" during the time required to sample the signal. S/H circuits operate in both static (hold mode) and dynamic (sample mode) circumstances. [3].

Figure 6. Output of Ideal S/H Circuit

3.1.3 SAR ADC Selection

The ADS8320 was selected because it best matches the design’s input requirements. The maximum throughput rate of the ADS8320 is 100 ksp/s, the resolution is equal to 16 bits, and the input range of the ADS8320 is equal to the reference voltage supplied to the converter. In this design, the reference voltage is equal to 3 V. Keep in mind these important specifications: the signal acquisition time (t_{ACQ} = 4.5 CLK cycles) and the value of the input capacitance of the SAR converter (C_{SH} = 45 pF).
3.2 Filter Parameters

Place a low-pass filter at the input of the ADC. Choosing the capacitor and resistor values play an important role to have a good AFE design.

C_{\text{FLT}} serves two purposes. First, this capacitor stores energy to charge the ADC internal sampling capacitor. Secondly, C_{\text{FLT}} provides a place for the internal capacitor’s charge to go. Due to the storage capabilities of C_{\text{FLT}}, this design guide will sometimes refer to this capacitor as the "flywheel" capacitor. C_{\text{FLT}} has this alternative name because, like a flywheel, it stores energy for the acquisition time of the ADC. Another name used to describe C_{\text{FLT}} is "charge reservoir" [1].

During acquisition, C_{\text{FLT}} and C_{\text{SH}} exchange charges so the voltage of C_{\text{SH}} changes to equal V_{\text{IN}}. This change allows the user to calculate the charge (Q_{\text{SH}}) needed to charge the internal sampling capacitor to the input voltage. Ideally, the charge reservoir provides enough charge to the internal sampling capacitor so that the voltage on the filter capacitor droops by less than 0.5 LSB of VS. Assuming the worst case condition, the input signal equals the full scale range (V_{\text{FSR}}) and 0.5 LSB of V_{\text{FSR}} equals 22.89 \mu V. This would require a filter capacitor, C_{\text{FLT}}, of 5.9 \mu F to be placed in front of the ADC. The following steps show how C_{\text{FLT}} has been calculated:

\[
Q_{\text{SH}} = Q_{\text{FLT}} \rightarrow C_{\text{SH}} \times V_{\text{FSR}} = C_{\text{FLT}} \times \left( \frac{1}{2} \text{LSB from } V_{\text{FSR}} \right) \rightarrow 135 \text{pC} = C_{\text{FLT}} \times 22.89 \mu V \rightarrow C_{\text{FLT}} = 5.9 \mu F
\]  

(1)

With a capacitance value of 5.9 \mu F, the op-amp may not be able to drive such a large capacitive load. If an external resistor (R_{\text{FLT}}) is added, the R_{\text{FLT}} | C_{\text{FLT}} time constant may not be small enough to allow the input signal to settle in a reasonable amount time. By partitioning the charge reservoir and the operational amplifier, the amplifier provides some of the current to charge the sampling capacitor. Now, as a starting point, the filter cap provides a less than 5% droop when supplying the charge. This suggests a more reasonable value for C_{\text{FLT}} of about 900 pF.

\[
C_{\text{SH}} \times V_{\text{FSR}} = C_{\text{FLT}} \times (0.05 \times V_{\text{FSR}}) \rightarrow 135 \text{pC} = C_{\text{FLT}} \times 0.15 \text{ V} \rightarrow C_{\text{FLT}} = 900 \text{pF}
\]  

(2)

This TI design has a C_{\text{FLT}} equal to 1 nF. This capacitor should be a high quality capacitor with low voltage and frequency coefficients. The recommended capacitor type is C0G. As a check, make sure the filter capacitor value chosen is at least 20 times the internal capacitor value. In this case, the value is more than 20 times the size.

By designing the external capacitor value to be at least 20 times larger than the size of the internal sampling capacitor, 95% of the charge required during the acquisition time comes from the external capacitor, C_{\text{FLT}}. This minimizes the effects of the charge redistribution on the driving amplifier. Additionally, this configuration reduces the voltage droop at the input to the SAR ADC, insuring that the instantaneous voltage droop at the amplifier is less than 5% of the original voltage droop without C_{\text{FLT}}.

The external R_{\text{FLT}} | C_{\text{FLT}} network must settle within the ADC acquisition time. This means that the converter’s acquisition time t_{\text{ACQ}} has to be bigger than the filter time constant (t_{\text{FLT}} for R_{\text{FLT}} | C_{\text{FLT}}) multiplied by a factor k, which is the number of time constants required to settle to within a half LSB to a given number of bits (in this case 12). Considering the CLK frequency is equal to 2.4 MHz (t_{\text{ACQ}} = 1.88 \mu s), the maximum filter time constant for this circuit is 157 ns.

As a rule of thumb, set the external R_{\text{FLT}} | C_{\text{FLT}} settling time constant a bit faster than ideal (for example, 60%) to allow a margin for error of the op-amp load transient and the small signal settling time:

\[
60\% \times t_{\text{ACQ}} \leq k \times t_{\text{FLT}} \rightarrow R_{\text{FLT}} \geq \frac{60\% \times t_{\text{ACQ}}}{k \times C_{\text{FLT}}} = 94.2 \Omega
\]  

(3)

This TI design has an R_{\text{FLT}} equal to 100 \Omega.
3.3 Input Amplifier

Because the system is targeted for high-impedance output sensors, CMOS or JFET input amplifiers are preferable. The LMP7716 is a CMOS amplifier with low-input referred noise and low-input bias current, which make it an ideal choice for sensor interfaces such as thermopiles, IR thermometers, thermocouple amplifiers, and pH electrode buffers.

Most of the time, these sensors have low output voltages of a few microvolts. As a result, the op-amp used for this application needs to have low-offset voltage, low-input voltage noise, and low-input bias current.

Ensure the amplifier settles in enough time for the ADC to complete the signal acquisition. The gain bandwidth product of the amplifier is high enough to make sure that the input signal bandwidth is accounted for, and the amplifier is stable with the filter load. The amplifier has a fast slew rate to charge the filter changes and to quickly react to changes of the input.

Figure 7 shows the chosen configuration of the amplifier [2].

![Figure 7. Operational Amplifier Configuration](image)

The sensitivity at the amplifier output, $S_{AMP}$, is defined by the following:

$$S_{AMP} = \left(1 + \frac{R_2}{R_1}\right) S$$

(4)

where $S$ is the sensitivity of the used sensor.

The resistor $R_B$ is necessary to bias at the input. The capacitor $C_F$ set a low-pass filter with $R_2$. The cut-off frequency of this low pass filter is

$$\frac{1}{2 \times \pi \times C_F \times R_2} = 19.4 \text{ kHz}$$

(5)

Table 2 presents the design parameters used in this TI design.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_B$</td>
<td>10 MΩ</td>
</tr>
<tr>
<td>$R_1$</td>
<td>100 Ω</td>
</tr>
<tr>
<td>$R_2$</td>
<td>10 kΩ</td>
</tr>
<tr>
<td>$C_F$</td>
<td>820 pF</td>
</tr>
<tr>
<td>Gain</td>
<td>101</td>
</tr>
</tbody>
</table>
3.4 Reference Voltage

Data acquisition systems often require stable voltage reference to maintain accuracy. The REF5030 features low noise, very low drift, and high initial accuracy for high-performance data converters. The output of the REF5030 is 3 V, which will fix the voltage range of the ADC.

3.5 LaunchPad Ecosystem

LaunchPads are microcontroller development kits from Texas Instruments focusing on ease of use for evaluation:

- Simple USB interface to PC (no more need for additional debugger to connect to the JTAG port as the logic is already on the LaunchPad board)
- Standardized interface for extension boards (called Booster Packs)

The LaunchPads comply to the following electrical interface specification, which is available as a PDF here: http://www.ti.com/ww/en/launchpad/dl/boosterpack-pinout-v2.pdf

Figure 8. LaunchPad Ecosystem
3.5.1 BoosterPack

Booster Packs are plug-in modules that fit on top of LaunchPads. These innovative tools plug into a consistent and standardized connector on the LaunchPad and allow developers to explore different applications enabled by a TI microcontroller.

Booster Packs are available from Texas Instruments, from third parties, and from the community. They include functions such as capacitive touch, wireless communication, sensor readings, LED lighting control, and more. Booster Packs are available in 20- and 40-pin variants, and multiple Booster Packs can plug into a LaunchPad to enhance the functionality of a design.

![BoosterPack Pinout](image-url)

**Figure 9. BoosterPack Pinout**

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Universal Sensor IF SAR BoosterPack

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4 Getting Started

To connect the TIDA-00564 BoosterPack, ensure that the connector index match on the LaunchPad and the BoosterPack.

Once connected, perform the following actions:
1. Connect the micro-USB of the LaunchPad to the PC.
2. Ensure in the Windows® Device Manager (or alternative naming for other OS) that the board is recognized.
3. Install Energia if not yet done.
4. Load the sketch on the LaunchPad. For the sketch, contact a TI representative.
5. Open the serial monitor to display the read values.

5 Test Setup

The TIDA-00564 was tested with a MSP-EXP430F5529 LaunchPad. The LaunchPad communicates to the TIDA-00564 through SPI, provides the clock and the CS, and reads back data from it. The LaunchPad is connected through micro-USB to the PC where thanks to an Energia sketch one can program the LaunchPad and read back values from a serial monitor.

Two tests were performed: one test applies at the input a sine wave at –1 dB of the full scale range varying the frequency of the signal and then checks the FFT with HSDC PRO; the other tests the output voltage by varying the DC voltage at the input for the full range. Figure 10 shows the test setup.

Figure 10. Test Setup
6 Test Data

6.1 Static Test (DC)

For the static test, a DC signal is applied at the input of the board and the value varies for the full range.

Considering a bias voltage equal to $V_{\text{DD}} \times \frac{R_7}{R_6 + R_7} = 3.3 \times \frac{90.9}{90.9 + 100} = 1.57 \text{ V}$ (see Figure 15), an amplifier gain equal to 101 (see Table 2), and an ADC range from 0 to 3 V (see Figure 15), one can easily calculate the ideal $V_{\text{INMAX}}$ and $V_{\text{INMIN}}$:

$$V_{\text{INMIN}} = \frac{V_{\text{OUTMIN}} - V_{\text{BIAS}}}{\text{Gain}} = \frac{0 - 1.57}{101} = -15.5 \text{ mV}$$  \hspace{1cm} (6)

$$V_{\text{INMAX}} = \frac{V_{\text{OUTMAX}} - V_{\text{BIAS}}}{\text{Gain}} = \frac{3 - 1.57}{101} = -14.2 \text{ mV}$$  \hspace{1cm} (7)

Figure 11 shows the error, which is the measured $V_{\text{OUT}}$ minus the ideal $V_{\text{OUT}}$. Consider that the measured $V_{\text{OUT}}$ is calibrated, meaning the offset and gain error are removed.

The offset voltage is measured by shorting the two inputs. The result is shown in Figure 12. The range (max-min) is equal to 42 codes. Considering that the LSB voltage of this system is equal to $45.78 \mu\text{V}$ (3 V/65536), multiplying it by 42 gets $1.8 \text{ mV}$. Note that the offset voltage of the ADS8320 is $\pm 2 \text{ mV}$ and one of the LMP7716 is $\pm 150 \mu\text{V}$, which explains where these results originated.

![Figure 11. Error (Measured $V_{\text{OUT}}$ Minus Ideal $V_{\text{OUT}}$) versus Input Voltage](image1)

![Figure 12. Offset Voltage](image2)

6.2 Dynamic Test (AC)

For the dynamic test, a sine wave is applied at the input of the board with fixed amplitude equal to 27 mV$_{\text{PP}}$ and a varying frequency of 0.5 kHz, 1 kHz, 5 kHz, and 10 kHz. The sampling frequency is equal to 49 kHz, limited by Energia. 1024 samples were acquired and then processed by the HSDC PRO tool from TI.

The used test setup does not allow the possibility to phase lock the ADC clock and the signal generator clock, so set the coherent frequency instead of the ideal one. This is the reason why in the next figures the frequency is slightly shifted from the ideal value. The following figures show the results of the tests for different frequencies (Blackman window is used).
Figure 13. FFT at 500 Hz (Input Signal –1dBFS)

Figure 14. FFT at 1 kHz (Input Signal –1dBFS)
Figure 15. FFT at 5 kHz (Input Signal –1dBFS)

Figure 16. FFT at 10 kHz (Input Signal –1dBFS)
7 Design Files

7.1 Schematics
To download the schematics for each board, see the design files at TIDA-00564.

Figure 17. TIDA-00564 Schematic
7.2 **Bill of Materials**
To download the bill of materials (BOM) for each board, see the design files at [TIDA-00564](https://www.ti.com).

7.3 **PCB Layout Recommendations**
The board has been designed in a BoosterPack form factor.
- Place in a very precise way the two 20-pin connector at each side of the board so that they perfectly matched with the 20-pin connector of the LaunchPad.
- Ensure the power to the ADS8320 is clean and well bypassed. A 0.1-\(\mu\)F ceramic bypass capacitor should be placed as close to the ADS8320 package as possible. In addition, a 1-\(\mu\)F to 10-\(\mu\)F capacitor and a 5-\(\Omega\) or 10-\(\Omega\) series resistor may be used to low-pass filter a noisy supply.
- Similarly bypass the reference with a 0.1-\(\mu\)F capacitor. Again, a series resistor and large capacitor can be used to low-pass filter the reference voltage.
- Place the GND pin on the ADS8320 on a clean ground point. In many cases, this will be the "analog" ground. Avoid connecting the GND pin too close to the grounding point for a microprocessor, microcontroller, or digital signal processor. If needed, run a ground trace directly from the converter to the power-supply connection point. The ideal layout includes an analog ground plane for the converter and associated analog circuitry.
- Use a supply bypass capacitor ranging between 1 to 10 \(\mu\)F for the REF5030.

7.3.1 **Layer Plots**
To download the layer plots for each board, see the design files at [TIDA-00564](https://www.ti.com).

7.4 **Altium Project**
To download the Altium project files for each board, see the design files at [TIDA-00564](https://www.ti.com).

7.5 **Gerber Files**
To download the Gerber files for each board, see the design files at [TIDA-00564](https://www.ti.com).

7.6 **Assembly Drawings**
To download the Gerber files for each board, see the design files at [TIDA-00564](https://www.ti.com).
8 References

1. Bonnie Baker, *Optimize Your SAR ADC Design*, E2E Community (http://e2e.ti.com/cfs-file/__key/communityserver-discussions-components-files/14/4478_PA_2D00_001--Optimize_5F00_SAR_5F00_converter_5F00_design-REV-b.pdf)


9 About the Author

GIOVANNI CAMPANELLA is an Industrial Systems Engineer with the Field Transmitter Team in the Factory Automation and Control organization. He earned his bachelor’s degree in electronic and telecommunication engineering at the University of Bologna and his master’s degree in electronic engineering at the Polytechnic of Turin in Italy. His design experience covers sensors and analog signal chain (with a focus on fluxgate and analytics sensing technologies) and mixed-signal control of DC-brushed servo drives.
## Revision History

### Changes from Original (September 2015) to A Revision

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