TI Designs

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TIDA-00477 is a 1-kW (1000 W) power factor converter (PFC) designed for telecom, server, and industrial power supplies, and motor drives. This reference design presents a continuous conduction mode boost converter, implemented using a UCD3138A Digital Power Supply controller with all protections built-in. Designed and tested hardware meets or exceeds conducted emission, surge, and EFT EN55014 requirements.

Key highlights of this reference design:

- Provides a ready platform of front-end PFC to address various power supplies and motor drives up to 1 kW
- Improves overall system performance with lower bus ripple, lower bus capacitance, lower RMS currents, and front-end protections
- Meets stringent current THD and power factor norms
- Protects for output overcurrent, overvoltage, and undervoltage conditions

Design Features

- Wide Operating Input Range: 195-V to 270-V AC
- Designed to Drive Wide Range of Downstream DC/DC Converters and Inverter-Fed Motors up to 1 kW
- High Power Factor > 0.99 and < 5% THD From Medium-to-Full Load (50% to 100%); Meets Current THD Regulations as per IEC 61000-3-2
- High Efficiency of > 97% at Full Load Over Entire Operating Voltage Range.
- No Need for External Cooling up to 55°C Ambient Operation for Loads ≤ 850 W
- Communicates Input Power Consumption Information of the Unit Precisely for all Load Conditions
- Built-in 12-V/3-W Supply for Housekeeping Power Needs
- PMBUS and Isolated UART for Communication
- Meets the Requirements of Conducted Emissions Standard – EN55011 Class A, EFT Norm IEC6000-4-4, and Surge Norm IEC61000-4-5
- PFC Converter Designed With a Simple, Small PCB Form Factor (165 × 95 mm)

Design Resources

- TIDA-00477: Design Folder
- UCD3138A: Product Folder
- UCC28881: Product Folder
- UCC27517A: Product Folder
- TLV704: Product Folder
- OPA2350: Product Folder
- ISO7321C: Product Folder

Featured Applications

- Telecom Rectifiers
- Server and Industrial Power Supplies
- Online UPS
- Power Storage Banks
- Motor Drives
## 1 Key System Specifications

### Table 1. Key System Specifications

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SPECIFICATIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage range</td>
<td>195 to 270-V AC (230-V nominal hi-line bus)</td>
</tr>
<tr>
<td>Input supply frequency</td>
<td>47 to 63 Hz</td>
</tr>
<tr>
<td>Output voltage</td>
<td>390-V DC</td>
</tr>
<tr>
<td>Output power</td>
<td>1000 W, 390 V at 2.56 A</td>
</tr>
<tr>
<td>Efficiency</td>
<td>&gt; 97%</td>
</tr>
<tr>
<td>Power Factor</td>
<td>&gt; 0.99</td>
</tr>
<tr>
<td>Protection</td>
<td>Output overcurrent</td>
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<tr>
<td></td>
<td>Output overvoltage</td>
</tr>
<tr>
<td></td>
<td>Output undervoltage</td>
</tr>
<tr>
<td></td>
<td>Open-loop detection</td>
</tr>
<tr>
<td>Line and load regulation</td>
<td>&lt; ± 0.5%</td>
</tr>
<tr>
<td>Operating ambient</td>
<td>-10°C to 55°C</td>
</tr>
<tr>
<td>Board form factor, specs</td>
<td>165 × 95 mm ; PCB type: FR4, two layers</td>
</tr>
<tr>
<td>Conducted emissions</td>
<td>As per EN55011 / EN55022 Class A</td>
</tr>
<tr>
<td>Power line harmonics</td>
<td>As per IEC 61000-3-2 Class A</td>
</tr>
<tr>
<td>EFT</td>
<td>As per IEC-61000-4-4</td>
</tr>
<tr>
<td>Surge</td>
<td>As per IEC-61000-4-5</td>
</tr>
</tbody>
</table>
2 System Description

The power supplies for telecom, server, and industrial systems convert AC line power to isolated constant DC voltage of –48 V in telecom systems, 12 V in server systems, and 24 V in industrial systems. These systems are typical of high power ranging from 1 to 5 kW. These power supplies need a front-end power factor correction circuit to shape the input current of the power supply, to meet the power factor, and match current THD norms such as IEC61000-2-3.

A power factor correction (PFC) circuit shapes the input current of the power supply to be in phase with the mains voltage and maximizes the real power drawn from the mains. In addition, PFC front end offers several benefits:

- Reduces RMS input current
  A power circuit with a 230-V/5-A rating is limited to about 575 W of available power with a PF of 0.5. Increasing the PF to 0.99 will double the deliverable power to 1138 W, allowing higher-power loads to be operated.
- Facilitates power-supply holdup
  The active PFC circuit maintains a fixed intermediate DC bus voltage independent of the input voltage, so the energy stored in the system does not decrease as the input voltage decreases. This allows use of smaller, cheaper bulk capacitors.
- Improves efficiency of downstream converters
  PFC reduces the dynamic voltage range applied to downstream inverters and converters, reducing voltage ratings of rectifiers that results in lower forward drops, and increasing operating duty-cycles causing lower current in switches.
- Increases the efficiency of the power-distribution system
  A lower RMS current reduces distribution wiring losses.
- Reduces the VA rating of standby power generators and stresses on neutral conductors
  Reducing harmonics eliminates the risk of triplen harmonics (the third and multiples thereof) that can amount to dangerous levels in the neutral conductor of Y-connected 3-phase systems.

This reference design uses a UCD3138A PFC controller to implement a boost power factor converter for use in telecom, sever, and industrial systems that demand a PFC up to 1 kW. The design provides a ready platform of active front end to operate downstream DC/DC converters or inverters operating on Hi-line AC voltage range from 195-V to 270-V AC.

Telecom, server, and industrial power supplies and motor drives require high efficiency over their entire operating voltage range and wide load variations from 50% to 100% load. This design demonstrates a high performance power factor stage in a small form factor (165 x 95 mm), operating from 195-V to 270-V AC and delivers up to 1 kW of continuous power output at greater than 97% efficiency. The design also provides precise information on power consumption of the end equipment from the AC input line, which can be used for energy calculations and control the load for power optimization on need basis.

The EMI filter at the front end of the circuit meets EN55011 class-A conducted emission levels. The design meets control circuit needs and drives a small DC fan for cooling by using a built-in housekeeping 2.5-W power supply. The design implements a low-frequency pulse-skipping techniques to regulate the DC bus during no load conditions (achieving very low standby power consumption). The design fully tests and validates for parameters such as regulation, efficiency, EMI signature, output ripple, startup, and switching stresses.

The design meets the key challenges of telecom, server, and industrial power supplies and motor drives to provide safe and reliable power with all built-in protections while delivering high performance with low power consumption and a low bill-of-material (BOM) cost.
3.1 Highlighted Products and Key Advantages

This reference design uses following highlighted products. Key features for selecting the devices for this reference design are provided in the following sections. Each product has further technical details in their respective product datasheets.

3.1.1 UCD3138A — Digital Power Supply Controller

To implement high performance and a small form factor PFC design at 1 kW power, the UCD3138A is the preferred controller as it offers a series of benefits to address the next generation needs of low THD norms and provides a digital interface for health monitoring and controls.

The UCD3138A is a fully programmable, power-optimized digital controller solution offering the benefits of simplicity in design to speed up time to market, while maintaining ample ability to develop high-performance and well-differentiated power supply solutions. The device includes a configurable digital state machine, optimized to meet the performance requirements of telecom and server isolated power applications, along with a general-purpose microcontroller. The controller features optimized digital hardware for implementing a number of innovative power management functions such as burst mode, ideal diode emulation, mode switching, synchronous rectification, and reduced quiescent current draw in the controller. In summary, the UCD3138A addresses key concerns such as high efficiency across the entire operating range, high degree of flexibility for various control schemes and topologies, high integration for increased power density, high reliability, and lowest overall system cost.

Other key features include:
- Digital control of up to three independent feedback loops
- Up to 16-MHz error analog-to-digital converter (EADC)
- Up to eight high-resolution digital pulse width modulated (DPWM) outputs
- Fully programmable, high-performance, 31.25 MHz, 32-bit ARM7TDMI-S processor
- 14-channel, 12-bit, 267 ksp general purpose ADC with integrated filters
- Communication peripherals (I2C/PMBus, two UARTs)
- Configurable PWM edge movement
- Configurable feedback control
- Configurable modulation methods
- Fast, automatic, and smooth mode switching
- High efficiency and light load management
- Soft start and stop with and without pre-bias
- Fast input voltage feed forward hardware
- Feature rich fault protection options
• Internal temperature sensor
• Timer capture with selectable input pins
• Up to five additional general purpose timers
• Built-in watchdog: BOD and POR
• Operating temperature: –40°C to 125°C

3.1.2 UCC27517A — Low-Side Gate Driver
Lower switching losses are necessary to achieve high efficiency. The switching losses of a MOSFET are a function of drive current that needs to pass quickly through the Miller Plateau Region of the power-MOSFET’s switching transition. A high-current gate driver placed closely to FET helps achieve faster turn on and turn off by effectively charging and discharging voltage across its gate-to-drain parasitic capacitor (CGD), thus reducing switching losses effectively.

The UCC27517A is a simple, low-cost, low-side gate-driver device, which offers superior replacement of standard NPN and PNP discrete solutions with peak-source and sink current of 4 A. The device is a single-channel high-speed gate driver and has symmetrical drive with negative input voltage handling (–5 V) ability. The UCC27517A operates over a wide VDD range of 4.5 to 18 V and wide temperature range of –40°C to 140°C.

Other key features include:
• Fast propagation delays (13 ns typical)
• Outputs held low during VDD UVLO (ensures glitch-free operation at power up and power down)
• Hysteretic-logic thresholds for high-noise immunity
• Output held low when input pins are floating
• 5-pin DBV (SOT-23) package helps to optimize the space

3.1.3 UCC28881 — 700-V Lowest Quiescent Current Off-Line Switcher
With an integrated 700-V power MOSFET, current sensing, and eliminating bias winding, the UCC28881 offers an easy to use AC/DC solution with minimal external component count and ideal device for low wattage in-house power supplies due to its unique built-in features. The key values of the UCC28881 solution are low quiescent power consumption, low component count, and robust operation with load short and inductor runaway protection.

Other key features include:
• Integrated 700-V start-up current source and power MOSFET
• < 100-µA IC quiescent current
• Self-biased switcher: Start-up and operation bias directly from rectified mains voltage
• No external current sense resistor
• Robust performance with load short and inductor current runaway
• Soft start and thermal shutdown

3.1.4 TLV704 — 24-V Input Voltage, 150-mA, Ultralow IQ Low-Dropout Regulators
To optimize no load power loss and meet the control circuit power needs, the low dropout (LDO) linear regulator TLV704 is selected. The TLV704 operates over a wide input voltage range of 2.5 to 24 V and provides 2% typical accuracy. The device is stable with an effective capacitance of 0.47 µF. This makes the TLV704 an ideal solution for always on systems, which require very little idle state power dissipation.

Other key features include:
• Current output up to 150 mA
• Low power IQ = 3.2 µA
3.1.5 **OPA2350 — High-Speed, Single-Supply, Rail-to-Rail Operational Amplifier**

An operational amplifier (op amp) strengthens signals to accommodate the measurement range of the UCD3138 for current sensing feedback. The op amp should have sufficient bandwidth and rail-to-rail operation for exact detection of current sense feedback. This design requires a low-noise, rail-to-rail swing, high-speed op amp, so the OPA2350 is selected. The features of the OPA2350 make it ideal for driving sampling ADCs used for control loops. In addition, the amplifier’s wide operating temperature range and wide common-mode range ensures device performance in the most demanding environments.

Other key features include:
- Rail-to-rail input and output
- Wide bandwidth: 38 MHz
- High slew rate: 22 V/µs
- Low noise: 5 nV/√Hz
- Single supply operation: As low as 2.5 V
- Wide common-mode range

3.1.6 **ISO7321C — Low-Power, Dual-Channel 1/1 Digital Isolator With Fail-Safe High**

For isolated communication interface dual channel isolator, the ISO7321C is the preferred choice, as it provides up to 3000 V$_{RMS}$ for 1 minute per UL 1577. The device is capable of operating up to 25 Mbps and has an integrated glitch filter to aid in low-frequency operation. In fail-safe condition, the ISO7321C output defaults to high level.

Other key features include:
- Low power consumption, Typical $I_{CC}$ per channel at 1 Mbps: 1 mA (3.3-V supply)
- Qualified for:
  - IEC 61000-4-2 Level 3 ESD at 6 kV
  - IEC61000-4-4 Level 4 EFT at 4-kV Power, 4-kV I/O
  - IEC 61000-4-5 Level 4 Surge at 6 kV (Air), 8 kV (Oil)
- Wide temperature range: –40°C to 125°C
4 System Design Theory

This reference design is a 1-kW boost power factor converter, operating in continuous conduction mode (CCM) and implemented using the UCD3138A Digital Power Supply controller. The design is specifically tailored for telecom, server, and industrial power supplies and motor drives. This serves as a superior alternative to existing analog control based PFC circuits used to meet the power harmonic norms. This design is intended for operation at country specific line voltages between 195-V to 265-V AC. Under full load conditions, the system has greater than 97% efficiency over the wide input operating voltage range from 195-V to 270-V AC. The design includes several embedded protections, which include output overvoltage protection and output short-circuit protection. In addition, the design provides precise information of the power consumption of the unit.

The main focus of this design is a low EMI, high efficiency, high power factor, and protected DC power rail for targeted applications.

4.1 PFC Regulator Operating Mode

The PFC shapes the input current of the power supply to maximize the real power available from the mains. The PFC must also comply with low harmonic (low THD) regulatory requirements such as IEC61000-3-2. Currently, two modes of operation have been widely used for PFC implementations: CCM and critical conduction mode (CrM). For higher power circuits, the topology of choice is the boost converter operating in CCM and with average current mode control. For lower power applications, the CrM boost topology is typically used.

For high power levels such as 1 kW, CCM operation is preferred as it has a lower peak and RMS currents. Lower peak currents significantly reduce the stress in power MOSFET, diode, and inductor. In addition, filtering is easier because the current is more continuous through the boost inductor. Finally, the switching frequency remains constant for the CCM operation, so the boost inductor design and EMI filter designs are easier.

4.2 PFC Circuit Component Design

The UCD3138A is configured for fixed frequency in CCM and requires minimal external components for high wattage PFC regulator implementation. The following sections illustrate the design process and component selection for this design.

4.2.1 Design Goal Parameters

Table 2 shows the design goal parameters for this design. These parameters are used in further calculations for the selection of components.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
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<td>INPUT</td>
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</tr>
<tr>
<td>$V_{IN}$</td>
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<td>270</td>
<td>$V_{AC}$</td>
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</tr>
<tr>
<td>$f_{LINE}$</td>
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<td>63</td>
<td>Hz</td>
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<td>$V_{OUT}$</td>
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<tr>
<td>PF</td>
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</tr>
<tr>
<td>$\eta$</td>
<td>96%</td>
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</tr>
</tbody>
</table>
### 4.2.2 Current Calculations

The input fuse, bridge rectifier, and input capacitor are selected based upon the input current calculations. First, determine the maximum average output current, $I_{\text{OUT(max)}}$:

$$I_{\text{OUT(max)}} = \frac{P_{\text{OUT(max)}}}{V_{\text{OUT}}}$$

$$I_{\text{OUT(max)}} = \frac{1000 \text{ W}}{390 \text{ V}} = 2.56 \text{ A}$$ (1)

The maximum input RMS line current ($I_{\text{IN RMS(max)}}$) is calculated using the parameters from Table 2 and the efficiency and power factor initial assumptions:

$$I_{\text{IN RMS(max)}} = \frac{P_{\text{OUT(max)}}}{\eta \times V_{\text{IN(min)}} \times PF}$$

$$I_{\text{IN RMS(max)}} = \frac{1000 \text{ W}}{0.96 \times 195 \text{ V} \times 0.99} = 5.40 \text{ A}$$ (2)

The maximum input current ($I_{\text{IN(max)}}$) and the maximum average input current ($I_{\text{IN AVG(max)}}$) can be determined based upon the calculated RMS value and assuming the waveform is sinusoidal:

$$I_{\text{IN(max)}} = \sqrt{2} \times I_{\text{IN RMS(max)}}$$

$$I_{\text{IN(max)}} = \sqrt{2} \times 5.40 \text{ A} = 7.63 \text{ A}$$ (3)

$$I_{\text{IN AVG(max)}} = \frac{2}{\pi} \times I_{\text{IN(max)}}$$

$$I_{\text{IN AVG(max)}} = \frac{2}{\pi} \times 7.63 \text{ A} = 4.86 \text{ A}$$ (4)

### 4.2.3 Bridge Rectifier

The maximum input AC voltage is 270-V AC, so the DC voltage can reach voltage levels of up to 385-V DC. Considering a safety factor of 30%, select a component with voltage rating greater than 500-V DC. The input bridge rectifier must have an average current capability that exceeds the input average current ($I_{\text{IN AVG(max)}}$). A higher current bridge rectifier optimizes the power loss due to diode forward voltage drop.

This design uses a 1000-V, 15-A diode GBJ1508 for input rectification.

Forward voltage drop of bridge rectifier diode, $V_{F_{\text{BRIDGE}}} = 0.85 \text{ V}$

The power loss in the input bridge ($P_{\text{BRIDGE}}$) can be calculated as:

$$P_{\text{BRIDGE}} = 2 \times V_{F_{\text{BRIDGE}}} \times I_{\text{IN AVG(max)}}$$

$$P_{\text{BRIDGE}} = 2 \times 0.85 \text{ V} \times 4.86 \text{ A} = 8.26 \text{ W}$$ (5)

Select an appropriately sized heat sink to maintain the safe operating area of the bridge rectifier.
4.2.4 Inductor Ripple Current

The TIDA-00477 operates best in CCM. If the chosen inductor allows a relatively high-ripple current, the converter will be forced to operate in Discontinuous Mode (DCM) at light loads and at the higher input voltage range. High-inductor ripple currents have an impact on the boundary of CCM and DCM and results in higher light-load THD. This also affects the choices for the input capacitor, current sense resistor (RSENSE), and internal compensation values tuned in the software of the UCD3138A. Allowing an inductor ripple current (ΔI RIPPLE) of 20% or less will result in CCM operation over the majority of the operating range but requires a boost inductor that has a higher inductance value and the inductor itself will be physically large. In this design, the inductor size has a 40% peak to peak ripple current to optimize performance with size and cost. The focus of the design minimizes space with the understanding that the converter operates in DCM at the higher input voltages and at light loads but is optimized well for a nominal input voltage of 230-V AC at full load.

4.2.5 Input Capacitor

Select the input capacitor based on the input ripple current and an acceptable high frequency input voltage ripple. Allowing an inductor ripple current (ΔI RIPPLE) of 40% and a high frequency voltage ripple factor (ΔV RIPPLE IN) of 2%, the maximum input capacitor value (CIN) is calculated by first determining the input ripple current (I RIPPLE) and the input voltage ripple, VIN RIPPLE:

\[ I_{\text{RIPPLE}} = \Delta I_{\text{RIPPLE}} \times I_{\text{IN(max)}} \]  
\[ V_{\text{IN, RIPPLE}} = \Delta V_{\text{RIPPLE, IN}} \times V_{\text{IN, RECTIFIED(min)}} \]  
\[ V_{\text{IN, RIPPLE}} = 0.02 \times (\sqrt{2} \times 195 \text{ V}) = 5.52 \text{ V} \] (7)

The recommended value for the input X-capacitor can now be calculated as:

\[ C_{\text{IN}} = \frac{I_{\text{RIPPLE}}}{8 \times f_{\text{SW}} \times V_{\text{IN, RIPPLE}}} \]  
\[ C_{\text{IN}} = \frac{3.05 \text{ A}}{8 \times 100 \text{ kHz} \times 5.52 \text{ V}} = 0.69 \mu\text{F} \] (8)

A standard value 1.0-µF X2 film capacitor is used.
4.2.6 Boost Inductor

Based upon the allowable inductor ripple current discussed previously, select the boost inductor \(L\_{\text{BST}}\) after determining the maximum inductor peak current, \(I_{\text{L\_PEAK}}\):

\[
I_{\text{L\_PEAK(max)}} = I_{\text{IN(max)}} + \frac{I_{\text{RIPPLE}}}{2}
\]

\[
I_{\text{L\_PEAK(max)}} = 7.63\ A + \frac{3.05\ A}{2} = 9.155\ A
\]

Calculate the minimum value of the boost inductor based upon the acceptable ripple current \(I_{\text{RIPPLE}}\) at a worst case duty cycle of 0.5:

\[
L_{\text{BST(min)}} \geq \frac{V_{\text{OUT}} \times D \times (1 - D)}{f_{\text{SW}} \times I_{\text{RIPPLE}}}
\]

\[
L_{\text{BST(min)}} \geq \frac{390\ V \times 0.5 \times (1 - 0.5)}{(100\ kHz \times 3.05\ A)} \geq 319\ \mu\text{H}
\]

The actual value of the boost inductor used is \(L_{\text{BST}} = 320\ \mu\text{H} \).

The duty cycle of operation is a function of the rectified input voltage and will continuously change over the half line cycle. Calculate the duty cycle \(\text{DUTY}_{\text{(max)}}\) at the peak of minimum input voltage:

\[
\text{DUTY}_{\text{(max)}} = \frac{V_{\text{OUT}} - V_{\text{IN\_RECTIFIED(min)}}}{V_{\text{OUT}}}
\]

\[
\text{DUTY}_{\text{(max)}} = \frac{390\ V - (1.414 \times 195\ V)}{390\ V} = 0.293
\]

4.2.7 Boost Diode

The output diode must have a blocking voltage that exceeds the output overvoltage of the converter and average current same as \(I_{\text{OUT(max)}}\). The diode is generally an ultra-fast recovery diode or a silicon carbide Schottky diode.

For high wattages such as 1 kW, using a silicon carbide Schottky diode, although more expensive, will eliminate the reverse recovery losses and result in less power dissipation. Select the C3D04060A, 600-V/7.5-A SiC diode, as the output diode.

The estimated power loss with SiC diode is \(V_{F\ 125C} = 1.25\ V;\ Q_{RR} = 0\).

\[
P_{\text{DIODE}} = 1.25\ V \times 2.56\ A + 0.5 \times 100\ kHz \times 390\ V \times 0\ nC = 3.20\ W
\]

If an ultra-fast diode is preferred over a silicon carbide Schottky diode, select the BYV29FX-600, a 600-V/9-A diode, for this design. Estimate the diode losses with ultra-fast diodes based on the forward voltage drop \(V_f\) at 125°C and the reverse recovery charge \(Q_{RR}\) of the diode:

\[
P_{\text{DIODE}} = V_f \times I_{\text{OUT(max)}} + 0.5 \times f_{\text{SW}} \times V_{\text{OUT}} \times Q_{RR}
\]

\[
P_{\text{DIODE}} = 1.5\ V \times 2.56\ A + 0.5 \times 100\ kHz \times 390\ V \times 13\ nC = 4.09\ W
\]

Use an appropriately sized heat sink for the boost diode.
4.2.8 Switching Element

A UCC27517A gate driver drives the MOSFET switch for which VCC bias voltages are limited to less than 12 V from the bias supply. Use an external gate drive resistor to limit the rise time and to dampen any ringing caused by the parasitic inductances and capacitances of the gate drive circuit; this will meet any EMI requirements of the converter. This design uses a 5.0-Ω resistor; the final value of any design is dependent upon the parasitic elements associated with the layout of the design. To facilitate a fast turnoff, a standard 100-V, 1-A Schottky diode or switching diode is placed anti-parallel with the gate drive resistor. Place a 10-kΩ resistor between the gate of the MOSFET and ground to discharge the gate capacitance and protect from inadvertent dv/dt triggered turn on.

Calculate the drain to source RMS current \( I_{\text{DS,RMS}} \) through switching FET by using the following equations:

\[
I_{\text{DS,RMS}} = \frac{P_{\text{OUT(max)}}}{V_{\text{IN,RECTIFIED(min)}}} \times \sqrt{2 - \frac{16 \times V_{\text{IN,RECTIFIED(min)}}}{3 \times \pi \times V_{\text{OUT}}}}
\]

\[
I_{\text{DS,RMS}} = \frac{1000 \text{ W}}{275 \text{ V}} \times \sqrt{2 - \frac{16 \times 275 \text{ V}}{3 \times \pi \times 390 \text{ V}}} = 3.24 \text{ A}
\]  

The maximum voltage across the FET is the maximum output boost voltage (that is, 420 V), which is the overvoltage set point of the PFC converter to shut down the output. Considering a derating of 30%, the voltage rating of the MOSFET should be greater than 550-V DC.

Select the IPP60R190P6 MOSFET of 600 V and 25 A at 25°C / 12 A at 100°C for the current design.

Estimate the conduction losses of the switch MOSFET in this design using the \( R_{\text{DS(on)}} \) at 125°C, found in the device datasheet, and the calculated drain to source RMS current, \( I_{\text{DS,RMS}} \):

\[
P_{\text{COND}} = I_{\text{DS,RMS}}^2 \times R_{\text{DS(on)}}
\]

\[
P_{\text{COND}} = 3.24^2 \text{ A} \times (0.37 \text{ Ω}) = 3.884 \text{ W}
\]  

Estimate the switching losses using the rise time, \( t_r \), and fall time, \( t_f \), of the MOSFET gate, and the output capacitance losses, \( C_{\text{OSS}} \):

\[
P_{\text{SW}} = f_{\text{SW}} \left[ 0.5 \times V_{\text{OUT}} \times I_{\text{IN(max)}} \times (t_r + t_f) + 0.5 \times C_{\text{OSS}} \times V_{\text{OUT}}^2 \right]
\]

\[
P_{\text{SW}} = 100 \text{ kHz} \times \left[ 0.5 \times 390 \text{ V} \times 7.63 \text{ A} \times (12 \text{ ns} + 9 \text{ ns}) + 0.5 \times 61 \text{ pF} \times 390^2 \text{ V} \right] = 3.588 \text{ W}
\]

Total FET losses:

\[
P_{\text{COND}} + P_{\text{SW}} = 3.884 + 3.588 = 7.472 \text{ W}
\]

Use an appropriately sized heat sink for the MOSFET.
4.2.9 Sense Resistor

Select a current sense resistor based on two key parameters:

- Optimizing the power loss in the circuit
- Requiring gain and bandwidth of the op amp used to amplify the current sense signal

For current sensing feedback, the OPA2350 strengthens the signals and accommodates the signal range within the measurement range of the UCD3138. In the UCD3138, the ADC used from current sensing has the measurement range of 0 to 1.6 V and has the analog comparator range of 0 to 2.5 V. To have the best signal-to-noise ratio and maximum input signal corresponding to overcurrent condition, $R_{\text{SENSE}}$ selected is 0.008 Ω.

For the signal conditioning, each input signal should follow the subsequent guidelines to limit the amplified signal within the range of ADC previously mentioned. The maximum op amp gain is defined by:

$$
K_1 \leq \frac{1.6 \text{ V}}{I_{\text{IN(max)}} \times 1.2 \times R_{\text{SENSE}}}
$$

In Equation 18, a factor of 20% is taken for the overcurrent limit.

$$
K_1 \leq \frac{1.6 \text{ V}}{7.63 \text{ A} \times 1.2 \times 0.008 \text{ Ω}} = 21.84
$$

Set a gain of 21.1 using resistors R24 and R26 across the current sense amplifier, U3, as shown in .

![Sense Resistor Schematic](image)

**Figure 2. Sense Resistor Schematic**

Calculate the power dissipated across the sense resistor, $P_{\text{RSENSE}}$:

$$
P_{\text{RSENSE}} = I_{\text{IN,RMS(max)}}^2 \times R_{\text{SENSE}}
$$

$$
P_{\text{RSENSE}} = 5.40^2 \text{ A} \times 0.008 \text{ Ω} = 0.233 \text{ W}
$$
### 4.2.10 Output Capacitor

Size the output capacitor, $C_{\text{OUT}}$, to meet holdup requirements of the converter. Assuming the downstream converters require the output of the PFC stage to always remain above 280-V DC ($V_{\text{OUT_HOLDUP(min)}}$) during one line cycle ($t_{\text{HOLDUP}} = 1 / f_{\text{LINE(min)}}$), the minimum calculated value for the capacitor is:

$$C_{\text{OUT(min)}} ≥ \frac{2 \times P_{\text{OUT(max)}} \times t_{\text{HOLDUP}}}{V_{\text{OUT}}^2 - V_{\text{OUT_HOLDUP(min)}}^2}$$

$$C_{\text{OUT(min)}} = \frac{2 \times 1000 \, \text{W} \times 21.3 \, \text{ms}}{(390^2 \, \text{V} - 280^2 \, \text{V})} = 578 \, \mu\text{F}$$

(20)

De-rate this capacitor value by 10%; the actual capacitor used is 660 µF.

To avoid triggering the output overvoltage or undervoltage protection features of the controller, verify that the maximum peak-to-peak output ripple voltage will be less than 5% of the output voltage. If the output ripple voltage is greater than 5% of the regulated output voltage, a larger output capacitor is required. The maximum peak-to-peak ripple voltage, occurring at twice the line frequency, and the ripple current of the output capacitor is calculated:

$$V_{\text{OUT_ripple(pp)}} < 0.05 \times V_{\text{OUT}}$$

(21)

$$V_{\text{OUT_ripple(pp)}} = \frac{I_{\text{OUT(max)}}}{2π \times 2 \times f_{\text{LINE(min)}} \times C_{\text{OUT}}}$$

$$V_{\text{OUT_ripple(pp)}} = \frac{I_{\text{OUT(max)}}}{2π \times 2 \times f_{\text{LINE(min)}} \times C_{\text{OUT}}}$$

(22)

The required ripple current rating at twice the line frequency is equal to:

$$I_{\text{COUT_2fline}} = \frac{I_{\text{OUT(max)}}}{\sqrt{2}}$$

$$I_{\text{COUT_2fline}} = \frac{2.56 \, \text{A}}{\sqrt{2}} = 1.81 \, \text{A}$$

(23)

A high frequency ripple current through the output capacitor exists:

$$I_{\text{COUT_HF}} = \frac{16 \times V_{\text{OUT}}}{3 \times π \times V_{\text{IN_RECTIFIED(min)}}} - 1.5$$

$$I_{\text{COUT_HF}} = 2.31 \, \text{A} \times \frac{16 \times 390 \, \text{V}}{3 \times π \times 1.414 \times 195 \, \text{V}} - 1.5 = 2.43 \, \text{A}$$

(24)

Select the output capacitor based on the total ripple current in the output capacitor, calculated as follows:

$$I_{\text{COUT_RMS(total)}} = \sqrt{(I_{\text{COUT_2fline}})^2 + (I_{\text{COUT_HF}})^2}$$

$$I_{\text{COUT_RMS(total)}} = \sqrt{(1.81 \, \text{A})^2 + (2.43 \, \text{A})^2} = 3.03 \, \text{A}$$

(25)
4.2.11 Output Voltage Set Point

For low power dissipation and minimal contribution to the voltage set point, use 600 kΩ for the top voltage feedback divider resistor, RFB1. Use multiple resistors in series due to the maximum allowable voltage across each resistor.

For each input signal to the UCD3138, the magnitude accommodates the measurement range of the device. In the UCD3138, the ADC measurement range is 0 to 2.5 V. To have the best signal-to-noise ratio, maximize the input signal. For this reason, the signal conditioning for each input signal must follow these guidelines:

For \( V_{\text{OUT}} \), the voltage divider:

\[
K_{V_{\text{OUT}}} \leq \frac{2.5 \, \text{V}}{V_{\text{OUT(max)}}}
\]

(26)

When the maximum output voltage \( V_{\text{OUTMAX}} \) is 420-V DC, including the overvoltage protection set at 415-V DC:

\[
K_{V_{\text{OUT}}} \leq \frac{2.5 \, \text{V}}{420 \, \text{V}} = 0.00595
\]

Considering the above constraints on the gain, select the bottom divider resistor, \( R_{\text{FB2}} \), to meet the feedback voltage of 2.0 V at \( V_{\text{OUT}} \) of 390 V.

\[
R_{\text{FB2}} = \frac{V_{\text{REF}} \times R_{\text{FB1}}}{V_{\text{OUT}} - V_{\text{REF}}}
\]

(27)

\[
R_{\text{FB2}} = \frac{2.0 \, \text{V}}{390 \, \text{V}} \times R_{\text{FB1}} = 3.07 \, \text{kΩ}
\]

Select a standard value 3.16 kΩ resistor for \( R_{\text{FB2}} \).

Add a 0.1-µF capacitor across RFB2 to filter out noise.
4.3 **Bias Power**

An auxiliary housekeeping power supply powers the UCD3138A control circuit, UCC27517A Gate Driver, and the inrush current limiting bypass relay. In addition, when the converter operates at power greater than or equal to 850 W, external cooling is required. To meet each need, the board produces an auxiliary power supply of 2.5 W using a low quiescent current, high voltage off-line switcher UCC28881. This device, including the integrated 700 V Power MOSFET, offers a low part count and a relatively low cost solution for implementing buck regulator to generate bias power.

The PFC pre-regulator output stage powers a buck converter and must start up prior to the PFC stage being operational. Therefore, design the circuit to operate over a wide input (100-V to 450-V DC) voltage. The buck converter output is designed for 12 V and 250 mA of current to meet the following power needs:

<table>
<thead>
<tr>
<th>DEVICE</th>
<th>VOLTAGE (V)</th>
<th>MAX CURRENT (mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>UCD3138A controller</td>
<td>3.3</td>
<td>100</td>
</tr>
<tr>
<td>Relay</td>
<td>12</td>
<td>35</td>
</tr>
<tr>
<td>Gate Driver</td>
<td>12</td>
<td>35</td>
</tr>
<tr>
<td>Fan (optional)</td>
<td>12</td>
<td>75</td>
</tr>
</tbody>
</table>

The application and implementation section of the UCC28881 datasheet explains the design of power stage components (output filter inductor, output filter capacitor, and feedback circuitry).

4.4 **Designing the Firmware on UCD3138A Controller for Single-Phase PFC**

The UCD3138 digital power supply controller has multiple peripherals inside the device, which have been specifically optimized to enhance the performance of PFC circuit.

A step-by-step guide for the design of the UCD3138A firmware required for the TIDA-00477 PFC is explained in the PMP10804 Test Results ([TIDUAY4](#)).

The document covers the hardware interface, voltage loop and current loop implementation, system protection, firmware structure, internal state machines, and other advanced features. Finally, a graphical user interface (GUI) and a guide for tuning the coefficients of a PFC system are presented.
5 Getting Started Firmware

This section details the necessary equipment, test setup, and procedure instructions for the TIDA-00477 board programming with provided software.

5.1 Programming the UCD3138A

Equipment and necessary files needed for programming the device:

- PMBus to USB Interface Adapter Kit: The USB Interface Adapter (HPA172)
  Accessories include:
  - USB interface adapter
  - USB cable (5-pin B Mini Male to Type A Male)
  - Ribbon cable (Socket to Socket, 10-pin, 2 headers, polarized)

![USB Adapter (HPA172) Outlook](image)

Figure 3. USB Adapter (HPA172) Outlook

- GUI installations file "TI-Fusion-Digital-Power-Designer-2.0.16.exe" or later version.
- Firmware File TIDCAX3_TIDA-00477_Program_V1.x0.
- PC computer operating system: Microsoft® Windows® XP®, or Vista®, or Windows 7®.
5.1.1 Equipment Setup (GUI)

1. Find Installation File
   The GUI installation file is "TI-Fusion-Digital-Power-Designer-Version-2.0.16.exe" or later version.

2. Install the software
   Double click and launch the ".exe" file to start the installation. Click "Next" until an agreement page appears. After reading the agreement, click "I accept the agreement." Click "Install".

3. Launch UCD3138 Device GUI
   After the installation, click "Finish" to exit setup; then click "Exit Program". The GUI for the TIDA-00477 board can be launched through the following steps:
   (a) Click the Windows "Start" button.
   (b) Click "All Programs".
   (c) Click "Texas Instruments Fusion Digital Power Designer".
   (d) Click "Device GUls".
   (e) Click "UCD3xxx & UCD9xxx Device GUI".

Figure 4. GUI Launch Path
5.1.2 Hardware Setup

Figure 5 shows the connection between TIDA-00477 and the PC computer through a USB Interface Adapter (HPA172).

To connect the USB Adaptor:
1. Connect one end of the ribbon cable to the TIDA-00477 board at connector J4 and connect the other end to the USB interface adapter (HPA172).
2. Connect the Mini connector of the USB cable to the USB interface adapter and connect the other end to the USB port of the PC Computer.
3. The LED on HPA172 should be illuminated. If not, un-plug the USB cable and reconnect. If the LED is still not illuminated, change with a new HPA172 USB adapter. If the LED is illuminated, proceed to the next step.
5.1.3 Procedure

1. Launch the GUI by the steps described in Section 5.1.1. Wait until the Figure 6 window appears.
2. Click "Scan Device in ROM Mode", then wait and check Figure 6 on its "Log" and confirm "Found ROM v2 IC v3 – UCD31xx". If "Found ROM" does not show, take the following steps:
   (a) Click "Device ID".
   (b) Click "Command Program" to jump to ROM (sendByte0xD9).
   (c) Click "Scan Device in ROM Mode" again.

If the device is detected, proceed to the next step.

![Figure 6. OK Indication (Found ROM)](image-url)
3. On the GUI shown in Figure 6, click "Firmware Download". A new window appears, shown in Figure 7. In this new window:

(a) Check "Download data flash".
If "DO NOT write program checksum" radio button is selected as in Figure 7, the firmware will not execute once the PFC powers up.
Click "Command ROM" to execute the program.

if "Write program checksum", radio button is selected, the firmware will execute automatically once the PFC powers up.

(b) Click "Select file".
Find "TIDCAX3_TIDA-00477_Program_V1.x0".
Click "Download".

(c) After the program downloads, click "Close" as shown in Figure 7.
6 Getting Started Hardware

This section details the necessary equipment, test setup, and procedure instructions to test and validate the TIDA-00477 board.

6.1 Test Conditions

For input, the power supply source (V\textsubscript{IN}) must range from 195-V to 270-V AC. Set the input current limit of input AC source to 7.5 A.

For output, use an electronic variable load or a variable resistive load, which must be rated greater than or equal to 400 V and must vary the load current from 0 mA to 3.0 A.

6.2 Test Equipment Required for Board Validation

- Isolated AC source
- Single-phase power analyzer
- Digital oscilloscope
- Multimeters
- Electronic load or resistive load

6.3 Test Procedure

1. Connect input terminals (Pin-1 and Pin-3 of connector J1) of the reference board to the AC power source.
2. Connect output terminals (Pin-1 and Pin-3 of connector J2) to electronic load, maintaining correct polarity. Pin-1 is V DC output and Pin-3 is GND terminal.
3. Set and maintain a minimum load of about 10 mA.
4. Increase the input voltage gradually from 0 V to turn on voltage of 195-V AC.
5. Start the load to draw current from the output terminals of the PFC.
6. Observe startup conditions for smooth switching waveforms.
7. For power greater than or equal to 850 W, an external fan can be used for cooling. A low wattage, high LFM fan such as 612NMLE is recommend for usage with 12 V output provided at connector J3. Ensure that fan is rated for 12-V operation and power less than or equal to 0.5 W.
8. Connect the fan at connector J3, maintaining correct polarity.
9. If low wattage fan is not available, a cooling fan can be powered from an external DC lab power supply.
7 Test Results

Test results are divided in multiple sections that cover the steady state performance, functional performance waveforms and test data, transient performance waveforms, thermal measurements, conducted emission measurements and surge and EFT measurements.

7.1 Performance Data

7.1.1 Efficiency and Regulation With Load Variation

Table 4 shows the data at 230-V AC input:

Table 4. Efficiency and Regulation with Load 230-V AC Input

<table>
<thead>
<tr>
<th>V_{INAC} (V)</th>
<th>I_{INAC} (A)</th>
<th>PF</th>
<th>P_{INAC} (W)</th>
<th>I_{THD} (%)</th>
<th>V_{OUT} (V)</th>
<th>I_{OUT} (A)</th>
<th>P_{OUT} (W)</th>
<th>EFF (%)</th>
<th>REG (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>230</td>
<td>0.19</td>
<td>0.57</td>
<td>24.20</td>
<td>26.00</td>
<td>390.70</td>
<td>0.05</td>
<td>20.30</td>
<td>83.90</td>
<td>-0.09</td>
</tr>
<tr>
<td>230</td>
<td>0.26</td>
<td>0.76</td>
<td>45.40</td>
<td>16.90</td>
<td>391.30</td>
<td>0.10</td>
<td>40.10</td>
<td>88.50</td>
<td>0.07</td>
</tr>
<tr>
<td>230</td>
<td>0.49</td>
<td>0.93</td>
<td>104.80</td>
<td>9.83</td>
<td>391.20</td>
<td>0.25</td>
<td>99.00</td>
<td>94.40</td>
<td>0.06</td>
</tr>
<tr>
<td>230</td>
<td>0.91</td>
<td>0.98</td>
<td>204.50</td>
<td>6.25</td>
<td>391.20</td>
<td>0.50</td>
<td>196.80</td>
<td>96.30</td>
<td>0.05</td>
</tr>
<tr>
<td>230</td>
<td>1.34</td>
<td>0.99</td>
<td>303.60</td>
<td>2.97</td>
<td>391.10</td>
<td>0.75</td>
<td>294.60</td>
<td>97.00</td>
<td>0.03</td>
</tr>
<tr>
<td>230</td>
<td>1.77</td>
<td>0.99</td>
<td>403.20</td>
<td>2.19</td>
<td>391.10</td>
<td>1.00</td>
<td>392.10</td>
<td>97.30</td>
<td>0.01</td>
</tr>
<tr>
<td>230</td>
<td>2.20</td>
<td>1.00</td>
<td>503.00</td>
<td>1.87</td>
<td>391.00</td>
<td>1.25</td>
<td>489.80</td>
<td>97.40</td>
<td>0.00</td>
</tr>
<tr>
<td>230</td>
<td>2.63</td>
<td>1.00</td>
<td>603.30</td>
<td>1.80</td>
<td>390.90</td>
<td>1.50</td>
<td>587.70</td>
<td>97.40</td>
<td>-0.02</td>
</tr>
<tr>
<td>230</td>
<td>3.07</td>
<td>1.00</td>
<td>703.80</td>
<td>1.59</td>
<td>390.90</td>
<td>1.75</td>
<td>685.60</td>
<td>97.40</td>
<td>-0.04</td>
</tr>
<tr>
<td>230</td>
<td>3.51</td>
<td>1.00</td>
<td>804.40</td>
<td>1.47</td>
<td>390.80</td>
<td>2.01</td>
<td>783.60</td>
<td>97.40</td>
<td>-0.05</td>
</tr>
<tr>
<td>230</td>
<td>3.92</td>
<td>1.00</td>
<td>899.50</td>
<td>1.50</td>
<td>390.80</td>
<td>2.24</td>
<td>875.40</td>
<td>97.30</td>
<td>-0.05</td>
</tr>
<tr>
<td>230</td>
<td>4.47</td>
<td>1.00</td>
<td>1027.00</td>
<td>1.60</td>
<td>390.80</td>
<td>2.55</td>
<td>997.90</td>
<td>97.20</td>
<td>-0.05</td>
</tr>
</tbody>
</table>

7.1.2 Standby Power

The standby power was noted at multiple AC input voltages with a constant negligible load on the output DC bus and with the PFC controller enabled and disabled. The results are tabulated in Table 5 and Table 6:

Table 5. PFC Circuit ON: Load: Constant Current: 1.92 mA

<table>
<thead>
<tr>
<th>V_{INAC} (V AC)</th>
<th>I_{INAC}(A)</th>
<th>P_{INAC} (W)</th>
<th>V_{OUT} (V)</th>
<th>I_{OUT} (A)</th>
<th>P_{OUT} (W)</th>
<th>NO LOAD POWER (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>195</td>
<td>0.100</td>
<td>4.62</td>
<td>391</td>
<td>0.002</td>
<td>0.75</td>
<td>3.87</td>
</tr>
<tr>
<td>230</td>
<td>0.110</td>
<td>4.12</td>
<td>391</td>
<td>0.002</td>
<td>0.75</td>
<td>3.37</td>
</tr>
<tr>
<td>270</td>
<td>0.124</td>
<td>3.87</td>
<td>391</td>
<td>0.002</td>
<td>0.75</td>
<td>3.11</td>
</tr>
</tbody>
</table>

Table 6. PFC Circuit OFF: Resistor R86 Removed\(^{(1)}\)

<table>
<thead>
<tr>
<th>V_{INAC} (VAC)</th>
<th>I_{INAC}(A)</th>
<th>P_{INAC} (W)</th>
<th>V_{OUT} (V)</th>
<th>I_{OUT} (A)</th>
<th>P_{OUT} (W)</th>
<th>NO LOAD POWER (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>195</td>
<td>0.095</td>
<td>2.88</td>
<td>275</td>
<td>0.001</td>
<td>0.37</td>
<td>2.51</td>
</tr>
<tr>
<td>230</td>
<td>0.106</td>
<td>3.25</td>
<td>322</td>
<td>0.002</td>
<td>0.51</td>
<td>2.74</td>
</tr>
<tr>
<td>270</td>
<td>0.122</td>
<td>3.55</td>
<td>381</td>
<td>0.002</td>
<td>0.71</td>
<td>2.84</td>
</tr>
</tbody>
</table>

\(^{(1)}\) Resistor R86 removed to isolate PWM output of UCD to gate driver

Three main branches contribute no load power:
- Input AC voltage sensing resistors
- Output DC bus voltage sensing resistors
- Buck regulator delivering power to controller, relay and gate driver
Power loss contribution and reduction possibilities:
- AC input and DC output sensing resistors consume approximately 0.55 W. Increasing resistor values can decrease the power consumed by AC input and DC output sensing resistors.
- LDO power loss used to power controller is approximately 0.87 W and by using a DC-DC converter to converter 12-V bias to 3.3 V the power loss is mitigated.

7.2 Performance Curves

7.2.1 Efficiency and Power Factor With Load and Line Variation

Figure 8 and Figure 9 show the measured efficiency and power factor in the system with AC input voltage variation.

Figure 8. Efficiency Versus Output Load Current ($I_{OUT}$)

Figure 9. Power Factor versus Load Current
7.2.2 Input THD With Load and Line Regulation

Figure 10 shows the measured input THD of the system with AC input voltage variation. Figure 11 shows the measured load regulation of the output with AC input voltage variation.
7.3 Functional Waveforms

7.3.1 Switching Node Waveforms

The waveform at switching (SW) node was observed along with the MOSFET current for 230-V AC and 270-V AC under full load (2.31 A) conditions.

![Waveform Image]

**Figure 12. SW Node Waveform and MOSFET Current at $V_{INAC} = 230$-V AC, Full Load**

**Figure 13. SW Node Waveform Turnon Cycle at $V_{INAC} = 230$-V AC, Full Load**

**Figure 14. SW Node Waveform Turnoff Cycle at $V_{INAC} = 230$-V AC, Full Load**

**NOTE:** Red trace: Drain voltage, 100 V/div; Green trace: Drain current, 5 A/div
7.3.2 Input Voltage and Current Waveform

Figure 15 shows the input current waveform at 230-V AC with full load condition.

Figure 15. Input Voltage and Input Current at $V_{INAC} = 230$-V AC, Full Load
7.3.3 Inrush Current Waveform

Inrush current drawn by the system is observed and recorded at maximum input voltage of 270-V AC.

![Inrush Current Waveform](image)

Figure 16. Output Voltage and Input Inrush Current at $V_{INAC} = 270$ V, Full Load

7.3.4 Output Ripple

![Output Ripple](image)

Figure 17. Output Voltage Ripple at $V_{INAC} = 230$ V, Full Load

Figure 18. Output Voltage Ripple at $V_{INAC} = 230$ V, Full Load, Only 50-Hz Component

**NOTE:** Ripple observed at 390-V DC output loaded to 2.56 A at 230-V AC.
7.3.5 Turn-on Characteristics

The 390-V output turn on at full load (2.31 A) was recorded at 230-V AC.

![Figure 19. Output Turn-on Waveform at V_{INAC} = 230 V With Light Load of 0.5 A](image1)

![Figure 20. Output Turn-on Waveform at V_{INAC} = 230 V, With Full Load of 2.56 A](image2)

**NOTE:** Red trace: Output DC bus, 100 V/div; Blue trace: Input voltage, 100 V/div.

7.4 Transient Waveforms

7.4.1 Transient Load Response

Observed load transient performance with the load switched at a 0.2-m wire length. Switch the output load using electronic load.

\[ V_{IN} = 230-V AC, \text{ load transient from 0.5 to 2.56 A with vice-versa performance at 390 V output.} \]

![Figure 21. Output Voltage Waveform at V_{INAC} = 230 V, Load Transient From 0.5 to 2.56 A](image3)

![Figure 22. Output Voltage Waveform at V_{INAC} = 230 V, Load Transient From 2.56 to 0.5 A](image4)

**NOTE:** Red trace: Output voltage, 20 V/div, AC coupling; Green trace: Output current, 1 A/div.
7.5 **Conducted Emissions**

Conducted emissions will generally be more at full load. Choose this operating point for measuring EMI.

7.5.1 **With Resistive Load at Output**

Connect the 230-V AC input, 2.56 A resistive load to the PSU using short leads. In a pre-compliance test setup, the conducted emissions were compared against EN55011 class-A limits and found to meet these limits satisfactorily.

![Conducted Emissions per EN55011 Class A](image)

*Figure 23. Conducted Emissions per EN55011 Class A*
7.6 Surge and Fast Transient Test

Per EN55014, surge and EFT tests are completed on the boards. The test condition and test results are tabulated in Table 7:

Table 7. Surge and EFT Test Result

<table>
<thead>
<tr>
<th>BASIC STANDARD</th>
<th>PORT</th>
<th>REQUIREMENTS OF IEC 61000-6-2/EN 50082-2: IMMUNITY STANDARD FOR INDUSTRIAL ENVIRONMENTS</th>
<th>PERFORMANCE CRITERION REQUIRED</th>
<th>TEST RESULT</th>
</tr>
</thead>
<tbody>
<tr>
<td>IEC/EN 61000-4-4: EFT</td>
<td>AC input</td>
<td>±2 kV, 5 kHz</td>
<td>B&lt;sup&gt;(1)&lt;/sup&gt;</td>
<td>Passed with performance criterion A&lt;sup&gt;(2)&lt;/sup&gt;</td>
</tr>
<tr>
<td>IEC/EN 61000-4-5: Surge</td>
<td>AC input</td>
<td>±4 kV line to earth ±2 kV line to line</td>
<td>B&lt;sup&gt;(1)&lt;/sup&gt;</td>
<td>Passed with performance criterion A&lt;sup&gt;(2)&lt;/sup&gt;</td>
</tr>
</tbody>
</table>

<sup>(1)</sup> Temporary loss of function or degradation of performance that ceases after the disturbance ceases

<sup>(2)</sup> Normal performance within limits specified by the design/manufacturer
Figure 24. Power Stage, Current, and Voltage Sensing
Figure 25. Controller and Communication Interface
## 8.2 Bill of Materials

To download the bill of materials (BOM), see the design files at [TIDA-00477](#).

<table>
<thead>
<tr>
<th>QTY</th>
<th>REFERENCE</th>
<th>PART DESCRIPTION</th>
<th>MANUFACTURER</th>
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<tr>
<td>1</td>
<td>PCB</td>
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<tr>
<td>1</td>
<td>BR1</td>
<td>Diode, Bridge Rectifier, GPP 15A 800V GBJ</td>
<td>Micro Commercial Components</td>
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<tr>
<td>2</td>
<td>C1, C2</td>
<td>CAP, Film, 0.68 µF, 630 V, +/- 20%, TH</td>
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<td>B32923C3684M</td>
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<tr>
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<td>C3</td>
<td>CAP, Film, 1.5 µF, 630 V, +/- 20%, 0.017 ohm, TH</td>
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<td>3</td>
<td>C4, C5, C6</td>
<td>CAP, ALUMINIUM, RADIAL, 220 uF, 450 V, 20%, TH</td>
<td>RUBYCON</td>
<td>450QXW220MEFC18X50</td>
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<td>4</td>
<td>C7, C8, C9, C10</td>
<td>CAP, CERM, 2200 pF, 250 V, +/- 20%, E, Radial Disc D10.5x7mm</td>
<td>TDK</td>
<td>CS11-E2GA22M4NS</td>
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<td>C11</td>
<td>CAP, Film, 0.047 µF, 630 V, +/- 20%, TH</td>
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<td>C12</td>
<td>CAP, CERM, 0.1 µF, 50 V, +/- 10%, X7R, 0603</td>
<td>AVX</td>
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<td>C13</td>
<td>CAP, CERM, 1 µF, 25 V, +/- 10%, X7R, 0603</td>
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<td>C15, C16</td>
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<td>C17, C18, C22</td>
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<td>C29</td>
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<td>C31, C41, C42</td>
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<td>C36, C39</td>
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<td>H1, H2, H3, H4, H5, H6, H7, H8</td>
<td>Bumpon, Hemisphere, 0.44 X 0.20, Clear</td>
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<td>SJ-5303 (CLEAR)</td>
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<td>H9, H10, H11</td>
<td>Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead</td>
<td>B&amp;F Fastener Supply</td>
<td>NY PMS 440 0025 PH</td>
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<td>Assmann</td>
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<td>TERMINAL BLOCK 5.08MM VERT 3POS, TH</td>
<td>On-Shore Technology</td>
<td>ED120/3DS</td>
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<td>PEC02SAAN</td>
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<td>J4</td>
<td>Header (shrouded), 100mil, 5x2, Gold, TH</td>
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<td>Header, 100mil, 8x1, Tin, TH</td>
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<td>Header, 100mil, 3x2, Tin, TH</td>
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<td>PEC03DAAN</td>
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<td>Relay, SPDT (1 Form C), 5A, 5 VDC, TH</td>
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<td>L1</td>
<td>INDUCTOR, 320 uH, 9.2 A, 10%, TH</td>
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<td>L2, L3</td>
<td>INDUCTOR, CHoke, COMMON MODE, 5 mH, 8.9 A, 22 mOHM, TH</td>
<td>Bourns Inc</td>
<td>8113-RC</td>
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<td>Inductor, Wirewound, 2.2 mH, 0.33 A, 3.2 ohm, TH</td>
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<td>M1, M2, M3</td>
<td>Mounting bracket for PCC-SMP</td>
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<td>RES, 75, 1%, 1 W, 2010</td>
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8.3 **Layout Guidelines**

A careful PCB layout is critical in a high-current fast-switching circuit to provide appropriate device operation and design robustness. With all switching power supplies, attention to detail in the layout can save time in later troubleshooting.

8.3.1 **Power Stage Specific Guidelines**

Follow these key guidelines to route the power stage components:

- Minimize the loop area and trace length of the power path circuits, which contain high frequency switching currents. This will help reduce EMI and improve the converter’s overall performance.
- Keep the switch node as short as possible. A short and optimal trace width helps to reduce induced ringing caused by parasitic inductance.
- Keep traces with high dV/dt potential and high di/dt capability away from, or shielded from, sensitive signal traces with adequate clearance and ground shielding.
- Keep power ground and control ground separate for each power supply stage. Tie them together (if they are electrically connected) in one point near DC input return or output return of the given stage.
- Ensure that when multiple capacitors are used in parallel for current sharing, the layout is symmetrical across both capacitor leads. If the layout is dissimilar, the capacitor with the lower series trace impedance will reach higher peak currents and become hotter ($i^2R$).
- Tie heat sinks of all the power switching components to their respective power grounds.
- Place protection devices such as TVS, snubbers, capacitors, or diodes physically close to the device they are intended to protect, and route with short traces to reduce inductance.
- Choose width of PCB traces based on acceptable temperature rise at the rated current as per IPC2152 as well as acceptable DC and AC impedances. The traces should withstand the fault currents (such as short circuit current) before electronic protection devices, such as fuses or circuit breakers, are activated.
- Determine the distances between various traces of the circuit according to the requirements of applicable standards. For this design, follow the [UL 60950-1 safety standard](https://www.ti.com) to maintain the creepage and clearance from live line to neutral line, and to safety ground, as defined in Tables 2K through 2N of this standard.
- Adapt the thermal management to fit the end-equipment requirements.
8.3.2 UCD3138A Controller Specific Guidelines

Follow these guidelines to route the controller components and signal circuits:

- The UCD3138A is a highly integrated controller with a large number of mixed signals. Group each pin, select good components, have appropriate connections to each pin, and place well on the PCB to reduce noise coupling and prevent chip malfunction.

- To avoid chip malfunction:
  1. Group all digital circuitry and analog circuitry
  2. Place digital circuitry close to each other.
  3. Place analog circuitry close to each other.
  4. Make trace connections among them

- Locate all controller support components at specific signal pins close to their connection pin. Connect the other end of the component to the AGND or DGND, respectively, with shortest trace length.

- Find detailed recommendations of each pin connection and its associated component in the UCD3138A Datasheet.

- Reference grounds AGND or DGND for the device can be common ground, signal ground (SGND), or separate grounds. In either case, these grounds should be a copper plane or island. If separate AGND or DGND planes exist, tie them together close to the chip.

- Make the trace routing for the voltage sensing and current sensing circuit components to the device as short as possible to reduce parasitic effects on the current limit and current and voltage monitoring accuracy. These traces must not have any coupling to switching signals on the board.

- Connect the SGND plane to high current ground (main power ground) at a single point that is at the negative terminal of DC IO capacitor, respectively.

8.3.3 Gate Driver Specific Guidelines

Follow these key guidelines to route the high-frequency high-current gate driver:

- Locate the driver device as close as possible to the power device to minimize the length of high current traces between the output pins of gate drive and the gate of the power device.

- Locate the VDD bypass capacitors between VDD and GND as close as possible to the driver with minimal trace length to improve the noise filtering. These capacitors support high-peak current being drawn from VDD.

- Minimize the turnon and turnoff current-loop paths (driver device, power MOSFET, and VDD bypass capacitor) as much as possible in order to keep the stray inductance to a minimum.

- Star point grounding minimizes noise coupling from one current loop to another. Connect the GND driver to the other circuit nodes, such as the power switch source or the PWM controller ground, at one single point. Ensure that the connected paths are short (to reduce inductance) and wide (to reduce resistance).

8.3.4 Layout Prints

To download the layout prints for each board, see the design files for TIDA-00477.

8.4 Altium Project

To download the Altium project files, see the design files at TIDA-00477.

8.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00477.

8.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00477.
9 Software Files

To download the software files for this reference design, see the design files at TIDA-00477.

10 References


11 Terminology

SLYZ022 — TI Glossary: Lists and explains terms, acronyms, and definitions.

Specific terms used in the document:

- **PWM** — Pulse Width Modulation
- **FETs, MOSFETs** — (Metal–Oxide–Semiconductor) Field-Effect Transistor
- **IGBT** — Insulated Gate Bipolar Transistor
- **ESD** — Electrostatic Discharge
- **RMS** — Root Mean Square

12 About the Author

**LATIF AMEER BABU** is a Systems Architect at Texas Instruments, responsible for developing reference design solutions for the industrial segment. Latif brings to this role his extensive experience in power electronics, high frequency DC-DC converter, and analog circuit design. Latif earned his master of technology in power electronics and power systems from Indian Institute of Technology, Mumbai; IN. Latif is a member of the Institute of Electrical and Electronics Engineers (IEEE) and has one US patent.

**BOSHENG SUN** is a Systems Engineer at Texas Instruments responsible for systems solution, firmware design and collateral development for TI’s high voltage power controller products. Bosheng earned a B.S. degree from Tsinghua University, China in 1995, and an M.S. degree from Cleveland State University, Ohio in 2003, both in electrical engineering. Bosheng has three US patents.
## Revision History

### Changes from Original (November 2015) to A Revision

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NOTE: Page numbers for previous revisions may differ from page numbers in the current version.
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