TI Designs — Precision: Verified Design
Low-Cost Digital Programmable Gain Amplifier Reference Design

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Circuit Description
This simple and low-cost programmable gain amplifier design creates non-inverting gains ranging from 6dB (2V/V) to 60dB (1000V/V). The design is based on a general purpose op amp and a digital potentiometer as one of the gain-setting elements. The digital potentiometer is controlled with a standard I2C digital interface.

Design Resources
TIPD204 All Design files
OPA316 Product Folder
TPL0102 Product Folder

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Low-Cost Digitally Programmable Amplifier
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Design Summary

The design requirements are as follows:

- Supply Voltage: ±1.3 V to ±2.5 V
- Gain Control: I2C Digital Communication
- Gain Range: 6dB – 60dB (2V/V – 1000V/V)

The design goals and performance for this low-cost digital programmable gain amplifier are summarized in Table 1. Figure 1 depicts the results for the design.

### Table 1: Comparison of Design Goals, Calculated, and Measured Performance

<table>
<thead>
<tr>
<th>Specification</th>
<th>Goals</th>
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<th>Measured</th>
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<td>Gain Range</td>
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</tr>
</tbody>
</table>

**Figure 1: Measured Transfer Function over the Full Range of Input Codes**
2 Theory of Operation

A standard non-inverting amplifier is created from an op amp, a feedback resistor, $R_F$, and an input, or gain-setting resistor, $R_G$, as shown in Figure 2. The transfer function for this standard op amp building block is shown in Equation 1.

\[
V_{OUT} = V_{IN} \cdot \left(1 + \frac{R_F}{R_G}\right)
\]

Figure 2: Non-Inverting Amplifier Circuit

To turn the non-inverting amplifier into a digitally controlled programmable gain amplifier, either the $R_F$ or $R_G$ resistance must be variable based on a digital control signal. Figure 3 and Equation 2 display the circuit and transfer function displayed in this design. $R_{LIMIT}$ is included in the circuit to set the maximum gain in the circuit, preventing an unbounded gain condition as the variable $R_G$ resistance approaches 0 Ω.

\[
V_{OUT} = V_{IN} \cdot \left(1 + \frac{R_F}{R_{LIMIT} + R_G}\right)
\]

Figure 3: Non-Inverting Programmable Amplifier Circuit Topology
For the non-inverting topology it is advantageous to control the $R_G$ resistance for two reasons. First, with a fixed $R_F$ resistance the feedback network resistance remains constant. Therefore, the output current delivered to the feedback network doesn’t change with gain and $R_F$ can be configured based on the circuit’s current consumption and noise requirements. Second, if a bandwidth limiting capacitor, $C_F$, is placed into the circuit to limit the bandwidth, the cutoff frequency, $f_{(3dB)}$, won’t vary as the gain changes. The cutoff frequency equation is shown in Equation 3.

$$f_{(3dB)} = \frac{1}{2\pi R_F C_F}$$ (3)

It is important to note that because of the non-inverting topology, the filtering effect will reduce the gain of the circuit down to 1V/V, but will not create a true single-pole filtering effect as created with a feedback capacitor in the inverting topology. This is because at high frequencies the $C_F$ capacitor will short out the $R_F$ resistance resulting in a feedback impedance, $Z_F$, near 0Ω. However, based on the transfer function for a non-inverting amplifier the gain will never decrease below 1V/V. This is shown in Equation 4.

$$\text{Gain} = \frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{R_F}{R_{GLIMIT} + R_G}\right) = \left(1 + \frac{0}{R_{GLIMIT} + R_G}\right) = 1V/V$$ (4)

3 Component Selection

3.1 TPL0102 Digital Potentiometer

The TPL0102 features two linear-taper potentiometers that are digitally controlled with a standard two-wire I2C communication protocol. The TPL0102 features a resistance range from roughly 0 Ω to 100 kΩ with 256 steps (8-bits). The TPL0102 can be configured as a two-terminal rheostat as used in this application or as a three-terminal potentiometer. A non-volatile memory (EEPROM) is used to store the wiper position between power cycles, returning the wiper to the previously programmed position once power is returned. The device features performance specifications of $\leq 0.5$ LSBs of integral non-linearity (INL), $\leq 0.25$ LSBs of differential non-linearity (DNL), and <2LSBs of zero-scale and full-scale errors.

3.2 OPA316 Op Amp

The OPA316 is a low-cost, low-voltage rail-to-rail input/output CMOS op amp. It features a power supply range from 1.8 V to 5.5 V, a unity gain bandwidth of 10 MHz, quiescent current of 400 μA and input noise of 11 nV/√Hz. The input offset voltage is 0.5 mV and input bias current is ±5 pA.

3.3 Passive Component Selection

To achieve the desired gain range from 6dB (2 V/V) to 60dB (1000 V/V) the $R_F$ and $R_G$ are selected based on the resistance range of the TPL0102 digital potentiometer, which is 0 Ω – 100 kΩ. To achieve the low-end gain of 6 dB (2 V/V) the $R_F$ resistor will be selected to be 100 kΩ as shown in Equation 5. The $R_{GLIMIT}$ resistance is assumed to be significantly smaller than the maximum resistance of the TPL0102 ($R_{G_MAX}$) so it falls out of the equation.

$$\text{Gain} = \frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{R_F}{R_{GLIMIT} + R_G}\right) = 2V/V$$

$$\Rightarrow R_F = \frac{2V/V - 1V/V}{100k\Omega} = 100k\Omega$$ (5)

The $R_{GLIMIT}$ resistance will be set based on the maximum gain goal of 60 dB (1000 V/V) as shown in Equation 6. The $R_{G_MIN}$ resistance of the TPL0102 is ideally 0 Ω.
\[
\text{Gain} = \frac{V_{\text{OUT}}}{V_{\text{IN}}} = \left(1 + \frac{R_F}{R_{\text{LIMIT}} + R_{G\text{,MIN}}} \right) = 1000 \text{V/V}
\]

\[\Rightarrow R_{\text{LIMIT}} = \frac{100 \text{k}\Omega}{1000 \text{V/V} - 1 \text{V/V}} = 99.9 \Omega
\]

\(R_{\text{LIMIT}}\) was selected to be a 100 \(\Omega\) resistor because it’s the closest standard value.

The complete circuit for this design including the selected passive components and the TPL0102 parasitic capacitances is shown in Figure 4.

![Detailed Programmable Gain Amplifier Circuit Schematic](image)

**Figure 4: Detailed Programmable Gain Amplifier Circuit Schematic**

As shown, the parasitic capacitance of the “L” pin of the TPL0102 is presented directly at the inverting input of the op amp requiring a feedback capacitor to prevent oscillations and other stability issues. As explained in Section 2 and Equation 3, the \(C_F\) capacitor also limits the gain-bandwidth of the circuit. The bandwidth limit for this circuit will be set to 50kHz. Therefore, the \(C_F\) capacitor was set to 33pF based on the closest standard value to the of the results shown in Equation 7.

\[
f_{(-3dB)} = 50 \text{kHz} = \frac{1}{2\pi R_F C_F}
\]

\[\Rightarrow C_F = \frac{1}{2\pi \times 100 \text{k}\Omega \times 50 \text{kHz}} = 31.8 \text{pF}
\]

The \(R_F\) and \(R_{\text{LIMIT}}\) resistors are selected for 1% tolerance to match the ±2LSB (out of 256) gain accuracy of the TPL0102.

### 4 Circuit Performance Calculations

The gain accuracy of this design is based on the specifications of the TPL0102 and the accuracy of the passive components selected in Section 3.

The TPL0102 also has some limitations on the range of resistances it produces which will limit the final gain range. The wiper-to-low resistance has a maximum value of 99.61k\(\Omega\) which sets the minimum gain to a little above 2V/V, as shown in Equation 8.

\[
\text{Gain}_{\text{MIN}} = \frac{V_{\text{OUT}}}{V_{\text{IN}}} = \left(1 + \frac{R_F}{R_{\text{LIMIT}} + R_{G\text{,MAX}}} \right) = \left(1 + \frac{100 \text{k}\Omega}{100\Omega + 99.6 \text{1k}\Omega} \right) = 2.003 \text{V/V}
\]
While the minimum wiper-to-low resistance of the TPL0102 is ideally 0 Ω, the typical terminal resistance is 60 Ω with a maximum value of 200 Ω. This limits the typical $R_{G,MIN}$ resistance to 60 Ω, which limits the maximum gain to 626 V/V or roughly 56 dB as shown in Equation 9.

$$\text{Gain}_{MIN} = \frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{R_F}{R_{GLIMIT} + R_{G,MIN}}\right) = \left(1 + \frac{10k\Omega}{100\Omega + 60\Omega}\right) = 626\, \text{V/V} = 55.9\, \text{dB}$$ \hspace{1cm} (9)

5 PCB Design

The PCB schematic and bill of materials can be found in Appendix A.

5.1 PCB Layout

For optimal performance of this design follow standard precision PCB layout guidelines, including proper decoupling close to all mixed signal integrated circuits and providing adequate power and GND connections with large copper pours.

The layout for the TIPD204 design is shown in Figure 5.

![Figure 5: Altium PCB Layout](image)

Note that this PCB is also used for TIPD205 and TIPD206 which is why there are some extra components not described in this document. Refer to the Bill of Materials to understand which components are used in TIPD204.
6 Verification and Measured Performance

The measured transfer function over the full range of input code values is shown in Figure 6. The minimum gain is 6dB and the maximum gain is 55.6dB as expected based on the calculations in Section 4.

![Gain vs Frequency](image)

Figure 6: Calibrated Output Current Error vs. RTD Temperature

6.1 Measured Result Summary

The measured performance is summarized and compared with the goals and calculated values in Table 2.

Table 2: Comparison of Design Goals, Simulated, and Measured Performance

<table>
<thead>
<tr>
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</tr>
</tbody>
</table>
7 Modifications

There are a few additional digital potentiometers that could be used to achieve similar designs to the one featured in TIPD204. They are listed in Table 3.

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Resolution</th>
<th>Resistance Range</th>
<th>Channels</th>
<th>Smallest Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPL0102</td>
<td>8 bits</td>
<td>0 – 100kΩ</td>
<td>2</td>
<td>QFN-14</td>
</tr>
<tr>
<td>TPL022</td>
<td>8 bits</td>
<td>0 – 10kΩ</td>
<td>2</td>
<td>WQFN-16</td>
</tr>
<tr>
<td>TPL0501</td>
<td>8 bits</td>
<td>0 – 100kΩ</td>
<td>1</td>
<td>8SOT-23</td>
</tr>
</tbody>
</table>

Since this design is for a basic circuit building block, there are many other op amp options that would be good candidates for this design depending on the design goals. Designs requiring higher levels of DC accuracy would benefit from the lower offset voltages and drifts featured in zero-drift (chopper) devices. A few other options are listed in Table 4.

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Bandwidth</th>
<th>Offset Voltage</th>
<th>Noise</th>
<th>Quiescent Current</th>
<th>Smallest Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPA316</td>
<td>10 MHz</td>
<td>500 μV</td>
<td>11nV/√Hz</td>
<td>400 μA</td>
<td>SC70-5</td>
</tr>
<tr>
<td>OPA317</td>
<td>0.3 MHz</td>
<td>90 μV</td>
<td>55nV/√Hz</td>
<td>21 μA</td>
<td>SC70-5</td>
</tr>
<tr>
<td>OPA313</td>
<td>1 MHz</td>
<td>2500 μV</td>
<td>25nV/√Hz</td>
<td>50 μA</td>
<td>SC70-5</td>
</tr>
<tr>
<td>OPA314</td>
<td>3 MHz</td>
<td>2500 μV</td>
<td>14nV/√Hz</td>
<td>150 μA</td>
<td>SC70-5</td>
</tr>
</tbody>
</table>

8 About the Authors

Collin Wells is an applications engineer in the Precision Linear group at Texas Instruments where he supports industrial products and applications. Collin received his BSEE from the University of Texas, Dallas.

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Appendix A.

A.1 Electrical Schematic

The Altium electrical schematic for this design can be seen in Figure 7.

Figure 7: Altium Schematic

A.2 Bill of Materials

The bill of materials for this circuit can be seen in Figure 8.

Figure 8: Bill of Materials
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