**TI Designs**  
**Getting Power from Earphone Jack**

**Design Overview**
This circuit is designed to power a small system attached to smartphone audio jack. The audio jack is power-limited and can output square or sine signal. The reference design includes a charge pump and a boost converter. The charge pump is used to filter AC output of one audio channel into a DC voltage and the ultra-low quiescent current boost converter TPS610981 is used to generate a regulated 3.3V. This reference design can work at a minimum 0.4V (peak) audio output sine (or square) signal and 2.2V biased voltage for micro-phone. The whole solution size is only 2.3 cm².

**Design Features**
- 0.4V to 2.2Vac (peak) input voltage range
- 3.3V and more than 1mA output current capability with 0.4Vac (peak) input
- Small solution size
- Smartphone remote control
- E-bank
- Mobile payment
- Sensor

**Design Resources**
- **Design Page**  
- **TPS610981**  
- **LMV7271**  
- **CSD17483F4**

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1 Key System Specifications

Table 1: System Specification

<table>
<thead>
<tr>
<th>Specification</th>
<th>Test condition</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage range</td>
<td>-40 ~85°C</td>
<td>0.4V-2.2Vac (peak)</td>
</tr>
<tr>
<td>Output voltage range</td>
<td>-40 ~85°C</td>
<td>3.2V-4.4V</td>
</tr>
<tr>
<td>Output Current</td>
<td>-40 ~85°C</td>
<td>&gt;1mA</td>
</tr>
</tbody>
</table>
2 System Description
The audio earphone jack is a common interface port in smartphone. Some smartphone APPs can work with hardware accessories through the earphone jack. The accessories can be e-bank, mobile payment, remote control and sensor. The reference design implements a power supply solution using the audio signal from the earphone jack for an accessory attached.

The standard 3.5mm audio plug contains 4 traces as shown in figure 1:

![Figure 1: Audio Plug](image)

Where
1. Left earphone (output)
2. Right earphone (output)
3. Common ground
4. Microphone (input)

Figure 2 is a typical application block diagram of a low power accessory attached to the earphone jack. The right channel functions as the communication line. Signal from smartphone is transmitted to the sub-system. The left channel provides power for the whole system. The microphone receives information from sub-system. A typical sub-system consists of low power MCU and sensors.

![Figure 2: Application Block Diagram](image)

The earphone jack power supply reference design is realized with the ultra-low power boost converter TPS610981 and a charge pump as shown in Figure 3. To improve the efficiency of the charge pump, a low threshold voltage NMOS FET is used to replace the traditional diode, controlled by a low power comparator LMV7271.

The minimum startup voltage of TPS610981 is 0.7V. After the startup phase is finished, the input voltage can be as low as 0.4V. The quiescent current of the TPS610981 is 300nA under no load condition.
2.1 **LMV7271**

The LMV7271 is a rail-to-rail input low power comparator. It consumes only 9-µA supply current while achieving 800-ns propagation delay.

The LMV7271 is available in SC70 and SOT-23 packages. With this tiny package, the PCB area can be significantly reduced. It is ideal for low voltage, low power, and space-critical designs.

The LMV7271 features a push-pull output stage which allows operation with minimum power consumption when driving a load.

2.2 **TPS610981**

The TPS610981 is an ultra-low power solution for products powered by coin battery, one-cell Li-Ion battery, or Li-polymer battery. It integrates a low-dropout linear regulator (LDO) with a boost converter and provides two output rails. The boost output VMAIN is designed as an always-on supply for a main system, and the LDO output VSUB is to power peripheral devices.

The TPS610981 has two modes controlled by the MODE pin: active mode and low power mode. In active mode, both outputs are enabled with enhanced response performance. In low power mode, the LDO is disabled to disconnect peripherals. The TPS610981 consumes only 300nA quiescent current.

The TPS610981 supports automatic pass-through function. When input voltage is higher than a pass-through threshold, the boost converter stops switching and passes the input voltage to VMAIN rail; when input voltage is lower than the threshold, the boost works in boost mode and regulates output at the target value.

The TPS610981 can provide up to 50 mA total output current at 0.7 V input to 3.3 V output conversion. The boost is based on a hysteretic controller topology using synchronous rectifier to obtain maximum efficiency at minimal quiescent current.

The TPS610981 is available in 1.5 mm × 1.5 mm WSON package to enable small circuit layout size.

2.3 **CSD17483F4**

The CSD17483F4 N-Channel MOSFET is a tiny footprint NMOS. The maximum $V_{GS(th)}$ is 1.1V and the drain-source voltage limit is 30V. CSD17483F4 is very good for this application with 0.21ohm typical on resistance at $V_{GS}$=3.3V.
3 System Design Theory

3.1 Charge pump

The charge pump is used to filter AC input from the left channel to DC voltage. Typical waveforms are shown in figure 4. Three phases are included: charge phase, discharge phase and hold phase.

3.1.1 Operating Principle

Phase 1—Charge phase
After the hold phase, the left channel goes down. VN will follow down and once VN goes below zero, the comparator LMV7271 will be triggered and output high voltage to turn on the NMOS FET. Charge will be stored on the \( C_{fly} \), the voltage across the capacitor \( V_{fly} \) will ramp up. The simplified circuit is shown in figure 5. When VN goes higher than zero, LMV7271 will turn off the NMOS FET and the charge phase finished.

Phase 2—Discharge phase
After the charge phase, \( V_{fly} \) is constant, VN will follow up with the input—\( V_{sine} \). Once VN reaches \( V_{cp} \) plus \( V_{diode} \) (the diode forward voltage), energy stored in the \( C_{fly} \) will be delivered to the output cap \( C_{boost} \) and the following boost converter. The simplified circuit is shown in figure 6. When VN is lower than \( V_{cp} \) plus \( V_{diode} \), D1 will block the path from \( V_{cp} \) to VN, discharge phase finished.

Figure 4: Typical Waveforms of the Charge Pump

Figure 5: NMOS ON
Phase 3—Hold phase
The period between the charge phase and discharge phase is the hold phase. During this period, both the NMOS and schottky diode are off, $V_{fly}$ is constant. The capacitor $C_{boost}$ will deliver the energy to the following boost converter.

### 3.2 Boost Converter

Figure 3 shows the boost converter to power the sub-system based on the TPS610981. The MODE pin is grounded, then VMAIN will be regulated at 3.3V and the ultra-low power mode is enabled. When input voltage is higher than VMAIN, TPS610981 will automatically switch to bypass mode. The detail operating principle can be found in the datasheet (SLVS873B).

For this application, the input voltage can go as low as 0.4V after the startup phase. With a chosen minimum input voltage of 0.4V, output current of 1mA and efficiency of 60%, the input current is 13.75mA. TPS610981 has the peak current at 350mA (minimum) which is enough to cover the worst case. This application operates in burst mode. A 4.7uH inductor with small package size 1608 or 2016 is preferred.

A 10uF 6.3V ceramic capacitor is selected as the output capacitor.

### 3.3 Auxiliary Power Supply Circuit

The simplified circuit of the auxiliary power supply circuit is shown in figure 7. This part can be removed if the input sine peak voltage is higher than 0.65V. Before the input voltage of TPS610981 ramps up, current will directly flow through the schottky diode D2 to VMAIN from the MIC input. VMAIN should be charged to 1.8V to start the comparator and TPS610981. The current path will be blocked when the TPS610981 enters normal operation and VMAIN outputs 3.3V. The resistor $R_{mic}$ of 100 ohm is reasonable if the MIC bias voltage is 2.2V.
4 Getting Started Hardware

4.1 Schematic

The schematic of the whole power supply system is shown in Figure 8. Attentions should be paid on if the peak value of the input sine signal is less than 0.5V.
1. At least one of C5 and C6 must be installed.
2. The diodes D₁ and D₂ should have a low forward voltage (<=0.25V at TA=25°C, I_D=10mA)

4.2 Bill of Materials

<table>
<thead>
<tr>
<th>Designator</th>
<th>Quantity</th>
<th>Value</th>
<th>Description</th>
<th>Package</th>
<th>Part Number</th>
<th>Manufacturer</th>
</tr>
</thead>
<tbody>
<tr>
<td>C₁</td>
<td>1</td>
<td>47uF</td>
<td>CAP, CERM, 47 μF, 6.3 V, +/-20%, X5R, 0603</td>
<td>0603</td>
<td>GRM188R60J476M</td>
<td>Murata</td>
</tr>
<tr>
<td>C₂, C₇, C₈</td>
<td>3</td>
<td>10uF</td>
<td>CAP, CERM, 10 μF, 6.3 V, +/-20%, X5R, 0603</td>
<td>0603</td>
<td>C0603C106M9PAC</td>
<td>Kemet</td>
</tr>
<tr>
<td>C₃</td>
<td>1</td>
<td>0.1uF</td>
<td>CAP, CERM, 0.1 μF, 6.3 V, +/-10%, X5R, 0402</td>
<td>0402</td>
<td>GRM155R60J104KA</td>
<td>Murata</td>
</tr>
<tr>
<td>C₄, C₅, C₆</td>
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<td>100uF</td>
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<td>Murata</td>
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<td>D₁, D₂</td>
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<td></td>
<td>Diode, Schottky, 20 V, 1A, SOD-323</td>
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<td>NSR0320MW2T1-D</td>
<td>ON Semi</td>
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<tr>
<td>J₁, J₂, J₃, J₄, J₅</td>
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<td></td>
<td>Header, 100mil, 2x1, Gold, TH</td>
<td>TSW-102-07-G-S</td>
<td>TSW-102-07-G-S</td>
<td>Samtec</td>
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<td>L₁</td>
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<td>4.7uH</td>
<td>Inductor, Wire wound, 4.7 μH, 0.95 A, 0.38 ohm, SMD</td>
<td>MAKK2016</td>
<td>MAKK2016T4R7M</td>
<td>Taiyo Yuden</td>
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<tr>
<td>Q₁</td>
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<td>MOSFET, N/P-CH, 30 V, 1.5 A, 1.0x0.35x0.6mm</td>
<td>YJC0003A</td>
<td>CSD17483F4T</td>
<td>TI</td>
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<tr>
<td>R₁</td>
<td>1</td>
<td>100</td>
<td>RES, 100, 1%, 0.1 W, 0603</td>
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<td>CRCW0603100RFKEA</td>
<td>Vishay</td>
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<tr>
<td>R₄</td>
<td>1</td>
<td>402</td>
<td>RES, 402, 1%, 0.1 W, 0603</td>
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<td>CRCW0603402RFKEA</td>
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<tr>
<td>U₁</td>
<td>1</td>
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<td>Single 1.8V Low Power Comparators with Rail-to-Rail Input</td>
<td>SOT23</td>
<td>LMV7271MFX</td>
<td>TI</td>
</tr>
<tr>
<td>U₂</td>
<td>1</td>
<td></td>
<td>Low Input Voltage Synchronous Boost with ultra-Low Quiescent Current and Integrated LDO/Load Switch, DSE5006A</td>
<td>WSON</td>
<td>TPS610981DSE</td>
<td>TI</td>
</tr>
</tbody>
</table>
5 Test Data

Typical values are at $V_{sine} = 0.4\text{V (peak)}$, $T_a=25\text{°C}$, unless otherwise noted.

5.1 Output Capability

Table 3: Max Output Capability with Different Audio Waveforms

All done with $C_{\text{boost}}=200\mu\text{F}$, $C_p=47\mu\text{F}, T_a=-40\text{°C}$

<table>
<thead>
<tr>
<th>Peak value of input voltage (V)</th>
<th>Load capability for Sine (mW)</th>
<th>Load capability for Square with 50% duty (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.4</td>
<td>8.8</td>
<td>13</td>
</tr>
<tr>
<td>0.45</td>
<td>17</td>
<td>21</td>
</tr>
<tr>
<td>0.5</td>
<td>25</td>
<td>28</td>
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<tr>
<td>0.55</td>
<td>35.5</td>
<td>38</td>
</tr>
<tr>
<td>0.6</td>
<td>48.5</td>
<td>51</td>
</tr>
<tr>
<td>0.7</td>
<td>75</td>
<td>82</td>
</tr>
</tbody>
</table>

5.2 Startup Waveform

Figure 9: No Load Startup with VMAIN Pre-biased by MIC Voltage
5.3 Switching waveform

Figure 10: No Load Startup

Figure 11: Rload=3.3K Ohm, Charge Pump Switching

Figure 12: Rload=3.3K Ohm, Boost Converter Switching

5.4 Load Transient
Figure 13: I_{out}=0\text{-}1\text{mA}\text{-}0

6 Design Files

6.1 Schematics
To download the Schematics for each board, see the design files at http://www.ti.com/tool/PMP9777

6.2 Bill of Materials
To download the Bill of Materials for each board, see the design files at http://www.ti.com/tool/PMP9777

6.3 PCB Layout Recommendations

6.3.1 Layout Prints
To download the Layout Prints for each board, see the design files at http://www.ti.com/tool/PMP9777

Figure 14: PMP9777 Top Overlay

Figure 15: PMP9777 Top Solder Mask
Figure 16: PMP9777 Top Layer

Figure 17: PMP9777 Bottom Layer

Figure 18: PMP9777 Bottom Solder Mask
6.4 **Altium Project**
To download the Altium project files for each board, see the design files at http://www.ti.com/tool/PMP9777

6.5 **Gerber files**
To download the Gerber files for each board, see the design files at http://www.ti.com/tool/PMP9777

6.6 **Assembly Drawings**

![Figure 19: PMP9777 Assembly Drawing](image-url)
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