Design Overview

This verified reference design is a signal-conditioning solution for the front-port QSFP28, which supports two 100-Gigabit Ethernet (GbE) ports compatible with 100G-CR4/SR4/LR4, 40G-CR4/SR4/LR4, and 10G SFF-8431 requirements. The design is applicable to optical and passive or active copper cables. The design also allows for reach extension between the switch ASIC and the front-port QSFP28, which is often required for the outermost ports of a top-of-rack (ToR) switch or for add-in mezzanine implementations of QSFP28 line cards. This reference design offers the flexibility for users to upgrade from a DS280BR810 repeater to the pin-compatible DS250DF810 retimer.

Design Resources

- TIDA-00427: Tool Folder Containing Design Files
- DS280BR810: Product Folder
- MSP430F5529: Overview Page
- TPD4E004: Product Folder
- TPS735: Product Folder
- TPS75725: Product Folder

Design Features

- Front-Port Stacked QSFP28 Implementation With Signal Conditioning to Support 10-, 40-, and 100-GbE Optical and Passive Copper
- Extends Reach Between Switch and Front-Port up to Three Times Beyond CAUI-4 Host Channel Loss Limit
- Low-Power and Low-Cost Solution for Front-Port Signal Conditioning
- Applicable to Top-of-Rack (ToR) Switch and Line Card Systems
- Single Power Supply—Does Not Require Firmware, heatsink, or Reference Clock
- Lab-Tested HW Example Including 10-, 40-, and 100-GbE Specific Test Data

Featured Applications

- Ethernet Switch
- Optical Networking
- Server NIC Card
Introduction

An IMPORTANT NOTICE at the end of this TI reference design addresses authorized use, intellectual property matters and other important disclaimers and information.

1 Introduction

This TIDA-00427 design guide summarizes the results of 100G CAUI-4 testing using the DS280BR810 low-power, 28-Gpbs, 8-channel linear repeater from Texas Instruments (TI). This guide also provides test results against the specifications of 40-GbE nPPI and SFF8431. The DS280BR810 has been tested in an egress signal-conditioning configuration against the jitter and eye mask requirement for CAUI-4 using a 2×1 stacked QSFP28 connector and host compliance board (HCB). These tests demonstrate the excellent signal conditioning capabilities of the DS280BR810 linear repeater and show that the DS280BR810 can extend the reach between the host application-specific integrated circuit (ASIC) and front-port cage by more than three times beyond the CAUI-4 host PCB channel limits.

The DS280BR810 is available in a small 8- × 13-mm leadless BGA package, which fits easily behind a standard 2x1 stacked QSFP28 connector, such as the TE Connectivity QSFP28 connector (2198373-1) used in these tests.


**2 Block Diagram**

*Figure 1* shows the typical front-port applications of the DS280BR810 device.

![Block Diagram](image)

*Figure 1. Typical Front-Port Applications of DS280BR810*
3 System Description

Using the DS280BR810 linear repeater for 100-GbE front-port applications provides several advantages over a traditional PHY. Table 1 lists the key advantages for a generic 36-port switch card application.

Table 1. System-Level Benefits Breakdown for Generic 36-Port 100-GbE Switch Card

<table>
<thead>
<tr>
<th>CRITERIA</th>
<th>TI DS280BR810 IMPLEMENTATION</th>
<th>TRADITIONAL CR4 PHY IMPLEMENTATION</th>
<th>BENEFIT OF TI</th>
</tr>
</thead>
<tbody>
<tr>
<td>No. of devices</td>
<td>18 (Egress signal conditioning only) 36 (Egress + ingress signal conditioning)</td>
<td>18 (Egress + ingress signal conditioning)</td>
<td>Flexible</td>
</tr>
<tr>
<td>Total device PCB area consumed</td>
<td>18 × 104 mm² = 1872 mm² (Egress only) 36 × 104 mm² = 3744 mm² (Egress + ingress)</td>
<td>Approx. 18 × 361 mm² = 6498 mm²</td>
<td>Less than half the PCB area</td>
</tr>
<tr>
<td>No of power rails</td>
<td>One only (2.5 V)</td>
<td>Three or more</td>
<td>Simpler power supply design</td>
</tr>
<tr>
<td>Input-to-output latency</td>
<td>&lt; 100 ps</td>
<td>Up to several hundred ns</td>
<td>Smaller latency</td>
</tr>
<tr>
<td>Reference clock required</td>
<td>No reference clock required</td>
<td>Low-jitter reference clock fan-out to all PHYs</td>
<td>No reference clock</td>
</tr>
<tr>
<td>PCB design flexibility</td>
<td>Uni-directional configuration allows for flexibility in device placement → more optimized for compact PCB design</td>
<td>Limited flexibility; lane swapping is complicated and limited</td>
<td>More flexibility in routing</td>
</tr>
<tr>
<td>User experience</td>
<td>Simple-to-use one-time configuration over I²C or EEPROM; all devices can share one EEPROM.</td>
<td>Firmware load required</td>
<td>Faster initialization</td>
</tr>
<tr>
<td>Implementation cost</td>
<td>Minimal external passive components (that is, decoupling capacitors), no requirement for supply filtering or reference clock distribution</td>
<td>Numerous passive components typically used (power supply filters, low-jitter reference clock fan-out, and so forth)</td>
<td>Lower overall BOM cost</td>
</tr>
</tbody>
</table>
4 System Design Theory

4.1 100-GbE CAUI-4 Egress Testing

100-GbE CAUI-4 is a parallel physical interface that allows for the construction of compact optical transceiver modules for 100GBASE-SR4/LR4 with clock and data recovery circuits inside. As a result, the IEEE 802.3bm standard, which governs the CAUI-4 interface, has defined the electrical requirements at the host board output to ensure the proper functioning of the attached optical modules. This user’s guide also shows test results for the specifications of 40-GbE nPPI and SFF8431.

The experiments in this report demonstrate the ability of the DS280R810 to provide excellent signal conditioning for the purposes of meeting CAUI-4 transmit electrical specifications.

4.1.1 CAUI-4 Specifications

CAUI-4 specifies jitter limits at a test point, which is equivalent to the output of the host compliance board (HCB). Figure 2 shows this test point, which is known as compliance point TP1a.

![Figure 2. Host CAUI-4 Compliance Point](image)

Table 2 lists the key specifications for CAUI-4 at the host output compliance point.

<table>
<thead>
<tr>
<th>INTERFACE SPECIFICATION</th>
<th>EYE HEIGHT (MIN)</th>
<th>PEAK-PEAK OUTPUT VOLTAGE (MAX)</th>
<th>EYE WIDTH (MIN)</th>
<th>COMMENT</th>
</tr>
</thead>
<tbody>
<tr>
<td>CAUI-4</td>
<td>95 mV</td>
<td>900 mV</td>
<td>0.46 UI1(1)</td>
<td>IEEE 802.3bm, Table 83E-1</td>
</tr>
</tbody>
</table>

(1) Based on the 802.3bm 83E.4.2 specification, which is defined at 1E-15 BER

4.1.2 Setup—Hardware

The hardware setup for these tests consists of:

- Centellax BERT (SSB-16000J and PG32)
- Evaluation kit (EVK) of 25-Gb/s Retimer DS250DF810 from TI
- Variable ISI channel, CLE1000
- Molex zQSFP+TM Host Compliance Boards (HCB)
- Agilent DCAx sampling scope with 86108B precision time base (PTB) module
- SMA cables, 1x8 MXP Huber-Suhner cables
**Figure 3** shows the test setup. In this scenario, the Centellax transmitter PG32 transmits a PRBS9 data pattern at 25.78125 Gbps, which is required by CAUI-4 for transmitter testing. The output of the PG32 connects with the input of the DS250DF810 device on the DS250DF810EVK through a 1x8 MXP Huber-Suhner cable. The DS250DF810 device locks to the data and retransmits the signal to its output. This data passes through a variable ISI channel CLE1000 into the HCB and then into the input of the QSFP28 board (red). The DS280BR810 linear repeater on the QSFP28 board equalizes and redrives the signal towards the QSFP28 connector. The Agilent DCAx scope measures the equalized eye at the output of the HCB and checks the eye height and eye width against the CAUI-4 specifications.

The intention of this test fixture is to mimic a line card or rack-mounted switch card design, similar to what **Figure 4** shows.
Figure 5 shows the DS280BR810 QSFP28 reference design board. The test board has two 100G QSFP28 ports arranged in a stacked 2x1 configuration on each side.

![DS280BR810 QSFP28 Reference Design Board (Top and Bottom)](image)

On the top side of the board, one HOST silk mark is labeled on the left side and one CABLE silk mark is labeled on the right side. These labels simplify the description of one specific QSFP 28 connector. Reference the top image in the preceding Figure 5.

On the schematic or PCB design of this board, the top QSFP port on the HOST side connects with the top QSFP port on the CABLE side. The bottom QSFP port on the HOST side connects with the bottom QSFP port on the CABLE side. Refer to the TIDA-00427 DS280BR810 100G QSFP28 Test Setup for the setup of this reference design board (TIDUBF8).

4.1.3 Results

The host transmitter output of eye height, peak-peak of the signal, and eye width have been measured for various combinations of losses. Table 3 summarizes the results.

**Table 3. Host Transmit Output Eye Height and Eye Width Results for CAUI-4**

<table>
<thead>
<tr>
<th>ISI SETTING</th>
<th>INPUT LOSS</th>
<th>OUTPUT LOSS</th>
<th>TOTAL LOSS</th>
<th>PORT</th>
<th>PRE</th>
<th>MAIN</th>
<th>PST</th>
<th>BW</th>
<th>BST1</th>
<th>BST2</th>
<th>VOD</th>
<th>DIFFERENTIAL INNER EYE HEIGHT AT 1E-15 PROBABILITY (mV pk-pk)</th>
<th>DIFFERENTIAL OUTER EYE HEIGHT AT 1E-15 PROBABILITY (mV pk-pk)</th>
<th>EYE WIDTH AT 1E-15 PROBABILITY (UI pk-pk)</th>
<th>100-GbE CAUI-4</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>BOT</td>
<td>–3</td>
<td>17</td>
<td>0</td>
<td>3</td>
<td>3</td>
<td>0</td>
<td>2</td>
<td>233</td>
<td>837</td>
<td>0.59</td>
<td>None</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>TOP</td>
<td>–3</td>
<td>17</td>
<td>0</td>
<td>3</td>
<td>3</td>
<td>0</td>
<td>2</td>
<td>232</td>
<td>819</td>
<td>0.60</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>BOT</td>
<td>–3</td>
<td>13</td>
<td>0</td>
<td>3</td>
<td>3</td>
<td>0</td>
<td>2</td>
<td>147</td>
<td>711</td>
<td>0.53</td>
<td>7</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>TOP</td>
<td>–3</td>
<td>13</td>
<td>0</td>
<td>3</td>
<td>3</td>
<td>0</td>
<td>2</td>
<td>153</td>
<td>682</td>
<td>0.53</td>
<td>12</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>BOT</td>
<td>–5</td>
<td>15</td>
<td>0</td>
<td>3</td>
<td>5</td>
<td>0</td>
<td>2</td>
<td>199</td>
<td>751</td>
<td>0.54</td>
<td>18</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>TOP</td>
<td>–5</td>
<td>15</td>
<td>0</td>
<td>3</td>
<td>5</td>
<td>0</td>
<td>2</td>
<td>189</td>
<td>740</td>
<td>0.52</td>
<td>23</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>BOT</td>
<td>–3</td>
<td>17</td>
<td>0</td>
<td>3</td>
<td>5</td>
<td>0</td>
<td>2</td>
<td>149</td>
<td>818</td>
<td>0.54</td>
<td>29</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>TOP</td>
<td>–3</td>
<td>17</td>
<td>0</td>
<td>3</td>
<td>5</td>
<td>0</td>
<td>2</td>
<td>137</td>
<td>805</td>
<td>0.52</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>BOT</td>
<td>–3</td>
<td>15</td>
<td>2</td>
<td>3</td>
<td>5</td>
<td>2</td>
<td>2</td>
<td>129</td>
<td>809</td>
<td>0.55</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>TOP</td>
<td>–3</td>
<td>15</td>
<td>2</td>
<td>3</td>
<td>5</td>
<td>2</td>
<td>2</td>
<td>134</td>
<td>792</td>
<td>0.55</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>BOT</td>
<td>–4</td>
<td>16</td>
<td>0</td>
<td>3</td>
<td>5</td>
<td>2</td>
<td>2</td>
<td>120</td>
<td>749</td>
<td>0.53</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>TOP</td>
<td>–4</td>
<td>16</td>
<td>0</td>
<td>3</td>
<td>5</td>
<td>2</td>
<td>2</td>
<td>119</td>
<td>740</td>
<td>0.55</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>BOT</td>
<td>–6</td>
<td>14</td>
<td>0</td>
<td>3</td>
<td>5</td>
<td>3</td>
<td>3</td>
<td>127</td>
<td>766</td>
<td>0.49</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>TOP</td>
<td>–6</td>
<td>14</td>
<td>0</td>
<td>3</td>
<td>5</td>
<td>3</td>
<td>3</td>
<td>124</td>
<td>754</td>
<td>0.52</td>
<td></td>
</tr>
</tbody>
</table>

(1) The pre, main, and post cursor setting of DS250DF810 determines the output amplitude and dB of de-emphasis. Reference the datasheet of DS250DF810 for further details.

(2) DS280BR810 is configured as eq_high_gain=1 and linear mode when performing the CAUI-4 tests.
In Table 3, the ISI setting is None for situations where the variable ISI channel CLE1000 has been bypassed. Consequently, at the input of the DS280BR810 linear repeater, the following components mainly contribute to the channel loss:

- Trace on the DS250DF810EVK and 1x8 MXP Huber-Suhner cable, which totals 3.9 dB
- HCB board, 3.5 dB
- QSFP28 connector, 1 dB
- Trace on the QSFP28 board, 1.7 dB

At the output of the DS280BR810 linear repeater, the following components mainly contribute to the channel loss:

- Trace on the QSFP28 board, 1.2 dB
- QSFP28 connector, 1 dB
- HCB board, 3.5 dB
- SMA cable, 0.7 dB

As Table 3 shows, by adding the CLE1000 in the middle of the test channel and varying its setting from 2 to 29, the channel loss at the input of the DS280BR810 linear repeater varies from 13.1 dB up to 22.4 dB at 12.9 GHz. The loss at the output of the DS280BR810 linear repeater is always fixed as 6.4 dB at 12.9 GHz.

All test results have met the CAUI-4 specifications and have margins that can be observed in the last three columns of Table 3.

In some applications, the output of the DS280BR810 linear repeater must also support 40-GbE nPPI and 10-GbE SFF8431 specifications. The table in Figure 6 shows the results of the tests performed with the same channel configuration of the 25-Gbps CAUI-4 tests using the same ASIC (DS250DF810) transmitter setting. The settings of the DS280BR810 linear repeater are almost the same except that eq_high_gain has been set to 0 to avoid violating the ≤ 700-mV peak-peak specification of the nPPI and SFF8431. In the real application, the boost and VOD settings of the DS280BR810 device occasionally require fine tuning to meet all the specifications and achieve greater margins of the nPPI and SFF8431 specifications.

Figure 6. Host Transmit Output—Eye Height and Eye Width Results for nPPI and SFF8431

(1) DS280BR810 is configured as eq_high_gain=0 and is in linear mode when performing the nPPI and SFF8431 tests.
5 Detailed Results

5.1 100-GbE CAUI-4

The following figures show the jitter and eye mask measurements for different loss configurations between the host transmitter and the DS280BR810 input on a 100-GbE front-port application.

Figure 7. ISI Setting None—Bottom

Figure 8. ISI Setting None—Top
Figure 9. ISI Setting 2—Bottom

Figure 10. ISI Setting 2—Top
Figure 11. ISI Setting 7—Bottom

Figure 12. ISI Setting 7—Top
Figure 13. ISI Setting 12—Bottom

Figure 14. ISI Setting 12—Top
Figure 15. ISI Setting 18—Bottom

Figure 16. ISI Setting 18—Top
Figure 17. ISI Setting 23—Bottom

Figure 18. ISI Setting 23—Top
Figure 19. ISI Setting 29—Bottom

Figure 20. ISI Setting 29—Top
5.2 40-GbE nPPI and SFF8431

The following figures show the jitter and eye mask measurements for different lengths of PCB media between the host transmitter and the DS280BR810 input in a 40-GbE nPPI and 10-GbE SFF8431 front-port application.

Figure 21. ISI Setting None—Bottom

Figure 22. ISI Setting None—Top
Figure 23. ISI Setting 2—Bottom

Figure 24. ISI Setting 29—Top
5.3 Layout Considerations

Stacked QSFP28 cages are commonly used in 100-GbE switch applications. The 8-channel DS280BR810 linear repeater easily fits behind a standard 2x1 stacked QSFP28 cage to service all eight egress channels or all eight ingress channels. The fact that the DS280BR810 is unidirectional allows for optimal placement of the signal conditioner: close to the cage for egress applications and close to the switch ASIC for ingress applications.

Figure 25 shows an example layout for the high-speed egress channels between two DS280BR810 devices (placed on the top of the PCB) and a stacked QSFP+ cage (placed on the top of the PCB). The DS280BR810 does not require a heat sink or airflow because the power consumption is 100 mW/channel.

![Figure 25. Example Layout for Egress and Ingress Repeaters Alongside Stacked QSFP28 Cage](image)

6 Conclusion

The DS280BR810 linear repeater can enable CAUI-4 TX compliance for channels with up to 22 dB of insertion loss between the Host TX and the DS280BR810 input. The CAUI-4 specification normally limits the insertion loss between the host transmitter and the front-port cage to 7.3 dB. The tests in this report demonstrate that the DS280BR810 linear repeater enables host PCB loss three times greater than the CAUI-4 specifications, extending the channel from 7.3 dB to approximately 22 dB.
7  Design Files

7.1 Schematics
To download the schematics, see the design files at TIDA-00427.

7.2 Bill of Materials
To download the bill of materials (BOM), see the design files at TIDA-00427.

7.3 Layer Plots
To download the layer plots, see the design files at TIDA-00427.

7.4 CAD Project
To download the CAD project files, see the design files at TIDA-00427.

7.5 Gerber Files
To download the Gerber files, see the design files at TIDA-00427.

7.6 Software Files
To download the software files, see the design files at TIDA-00427.

8  References

1. Texas Instruments, DS250DF810 25 Gbps Multi-Rate 8-Channel Retimer, DS250DF810 Data Sheet (SNLS495)
**IMPORTANT NOTICE FOR TI REFERENCE DESIGNS**

Texas Instruments Incorporated ("TI") reference designs are solely intended to assist designers ("Buyers") who are developing systems that incorporate TI semiconductor products (also referred to herein as "components"). Buyer understands and agrees that Buyer remains responsible for using its independent analysis, evaluation and judgment in designing Buyer’s systems and products.

TI reference designs have been created using standard laboratory conditions and engineering practices. **TI has not conducted any testing other than that specifically described in the published documentation for a particular reference design.** TI may make corrections, enhancements, improvements and other changes to its reference designs.

Buyers are authorized to use TI reference designs with the TI component(s) identified in each particular reference design and to modify the reference design in the development of their end products. **HOWEVER, NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY THIRD PARTY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT, IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used.**

Information published by TI regarding third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

**TI REFERENCE DESIGNS ARE PROVIDED “AS IS”. TI MAKES NO WARRANTIES OR REPRESENTATIONS WITH REGARD TO THE REFERENCE DESIGNS OR USE OF THE REFERENCE DESIGNS, EXPRESS, IMPLIED OR STATUTORY, INCLUDING ACCURACY OR COMPLETENESS. TI DISCLAIMS ANY WARRANTY OF TITLE AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, QUIET ENJOYMENT, QUIET POSSESSION, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS WITH REGARD TO TI REFERENCE DESIGNS OR USE THEREOF. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY BUYERS AGAINST ANY THIRD PARTY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON A COMBINATION OF COMPONENTS PROVIDED IN A TI REFERENCE DESIGN. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, SPECIAL, INCIDENTAL, CONSEQUENTIAL OR INDIRECT DAMAGES, HOWEVER CAUSED, ON ANY THEORY OF LIABILITY AND WHETHER OR NOT TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES, ARISING IN ANY WAY OUT OF TI REFERENCE DESIGNS OR BUYER’S USE OF TI REFERENCE DESIGNS.**

TI reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques for TI components are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

Reproduction of significant portions of TI information in TI data books, data sheets or reference designs is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has the necessary expertise to create and implement safeguards that anticipate dangerous failures, monitor failures and their consequences, lessen the likelihood of dangerous failures and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in Buyer’s safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed an agreement specifically governing such use.

Only those TI components that TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components that have not been so designated is solely at Buyer's risk, and Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2016, Texas Instruments Incorporated