Design Overview

The TIDA-00796 reference design is a complete resolver solution based on the system-on-chip (SoC) PGA411-Q1 sensor interface. A typical application for this TI Design is in electric vehicle (EV) and hybrid electric vehicle (HEV) powertrain systems. The PGA411-Q1 based design solves excitation amplifier, boost converter, diagnostics, and signal conditioning and reduces the PCB area. This altogether reduces overall cost and time-to-market.

Design Features

- SPI and Optional Parallel Interface to a Host System
- Interfacing With F28069™ controlSTICK and F28069M LaunchPad™ Development Kits
- 4-V_{RMS} or 7-V_{RMS}, 10- to 20-kHz Excitation Signal
- Integrated Step-up Converter for Excitation Amplifier
- Programmable Fault Detection Thresholds and Filters
- 5-V or 7- to 42-V Supply
- Compact 30×70-mm 4-Layer PCB
- AEC-Q100 Components

Featured Applications

- EV and HEV Powertrain Systems
- Power Steering
- Start-Stop Systems
- Motor Control

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1 Key System Specifications

Table 1. TIDA-00796 Technical Parameters

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SPECIFICATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating voltage</td>
<td>4.75 to 5.25 V from USB or 7 to 42 V external</td>
</tr>
<tr>
<td>Current consumption</td>
<td>100 mA with LTN 58 resolver and 4 V\text{_{RMS}} (USB powered)</td>
</tr>
<tr>
<td></td>
<td>typ. 70 mA with LTN 58 resolver and 4 V\text{_{RMS}} (external 9-V supply)</td>
</tr>
<tr>
<td>Resolver excitation voltage</td>
<td>typ. 4 V\text{<em>{RMS}} and 7 V\text{</em>{RMS}}</td>
</tr>
<tr>
<td>Resolver excitation frequency</td>
<td>Adjustable 10 to 20 kHz</td>
</tr>
<tr>
<td>Measured accuracy</td>
<td>Better than ±0.35° with LTN 58 resolver</td>
</tr>
<tr>
<td>Resolution</td>
<td>10 b or 12 b</td>
</tr>
<tr>
<td>Visual indicator</td>
<td>3 × LED (power rails and fault condition)</td>
</tr>
<tr>
<td>Resolver connection</td>
<td>PCB terminal block, 2.54-mm spacing</td>
</tr>
<tr>
<td>Logic levels</td>
<td>CMOS 3.3 V</td>
</tr>
<tr>
<td>Construction</td>
<td>4-layer PCB with top and bottom component placement</td>
</tr>
<tr>
<td>Dimensions</td>
<td>30 × 70 mm</td>
</tr>
<tr>
<td>System interface</td>
<td>Four wire SPI and additional GPIOs on 4×8-pin header with 2.54-mm spacing</td>
</tr>
<tr>
<td></td>
<td>Parallel interface with 1.27-mm raster</td>
</tr>
</tbody>
</table>
2 System Description

Resolver’s popularity in the automotive industry has been constantly growing, especially since demand for EV and HEV vehicles have been increasing as well. A typical resolver construction allows use in harsh environment while keeping reasonable costs. A power steering, start-and-stop system or traction inverter are the most common use cases in automotive.

The TIDA-00796 targets an application example of a resolver interface as shown on Figure 1.

![Figure 1. Typical Powertrain Inverter](image)

A typical powertrain inverter has a low-voltage control unit, often called a “cold side”, and a power unit called a “hot side”. Both units can share the same PCB or can be separated. The control unit has only low-voltage signals and must be galvanically isolated from any high-voltage circuitry.

The control unit has a host microcontroller that controls an electric motor. The power supply for the controller and low-voltage systems comes from the onboard DC-DC converter and from the system basis chip (SBC). The microcontroller is interfaced with the ECU using a CAN interface. Additional safety logic, for example an FPGA, may be used to achieve required safety level. The host microcontroller uses several feedback signals such as current, voltage, temperature, and velocity to control the system. The latter is usually based on a resolver technology. The resolver location is usually on the motor shaft. Because there is only mechanical coupling with the high-voltage system, the resolver interface can be located on the control unit, and additional galvanic isolation is not necessary.

The power unit has IGBT drivers to control IGBT gate signals properly. An HV flyback type converter supplies the power unit circuitry and is usually redundant with the DC-DC converter on the control unit. Voltage, current, and temperature measurements are galvanically isolated from the control unit.

A three-phase H-bridge based on IGBTs creates the output of the inverter. The DC Link capacitor and output terminals are connected through copper busbars.
2.1 Design Features

The main purpose of the TIDA-00796 reference design is to create an advanced PGA411-Q1 system for debugging and evaluation. The board is intended to be a daughter board for a host system as shown on Figure 2.

While the EVM gives better flexibility, the reference design provides maximum performance, careful component selection, and a subsystem implementation example including a bill of materials and PCB layout.

Figure 2. TIDA-00796 Overview

Important features include:

- Complete SoC solution for a resolver with integrated exciter, analog front-end (AFE), boost converter, and safety diagnostics
- Power from USB (5 V) or from the auxiliary DC-DC buck converter with 7- to 42-V wide input voltage range
- Interfacing with 3.3-V logic
- Four-wire SPI with optional parallel output interface to a host system
- Support for 4-V_{RMS} or 7-V_{RMS}, 10- to 20-kHz excitation signal
- Programmable fault detection thresholds and filters
- AEC-Q100 components
- Interfacing with F28069 controlSTICK and F28069M LaunchPad development kits
- Compact 30×70-mm four-layer PCB
- Demo source code for controlSTICK available and compatibility with TIDA-00363 firmware
3 Block Diagram

A simplified block diagram of the TIDA-00796, which highlights important blocks, is shown in Figure 3.

![Block Diagram of TIDA-00796](image)

3.1 Highlighted Products

The following TI products are used in this TI Design:

- The PGA411-Q1 is a resolver-to-digital converter (RDC) that is capable of both exciting and reading the sine and cosine angle from a resolver sensor. The exciter amplifier and boost regulator power supply are integrated on the chip.
- The TLV713P-Q1 series of low-dropout (LDO) linear regulators are low quiescent current LDOs with excellent line and load transient performance and are designed for power-sensitive applications. These devices provide a typical accuracy of 1%.
- The LM2842-Q1 are PWM DC/DC buck (step-down) regulators. With a wide input range from 4.5 to 42 V, they are suitable for a wide range of applications such as power conditioning from unregulated sources.
Figure 4. Functional Block Diagram of PGA411-Q1
Features:

- Qualified for automotive applications
- AEC-Q100 qualified with the following results:
  - Device temperature grade 1: –40°C to 125°C ambient operating temperature range
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C4B
- RDC
- Exciter preamplifier and power amplifier
- Exciter-boost power supply with spread spectrum
- Analog front-end
- Automatic offset calibration
- Type-II PI controller tracking loop
- Parallel, encoder, or SPI data output
- Analog data output
- SafeTI™ semiconductor component
  - Designed for functional safety applications
  - Developed according to the requirements of ISO 26262
- Automatic and manual phase correction
- Sensor-input fault detection
- Diagnostics interrupt output
- Internal and external oscillator
- Analog and logic built-in self-test for fault detection
- 64-pin HTQFP PowerPAD™ IC package
Features:

- AEC-Q100 qualified with the following results:
  - Device temperature grade 1: –40°C to 125°C ambient operating temperature range
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C4B
- Input voltage range: 1.4 to 5.5 V
- Stable operation with or without capacitors
- Foldback overcurrent protection
- Package: 5-pin SOT-23
- Very LDO: 230 mV at 150 mA
- Accuracy: 1%
- Low Iₒ: 50 μA
- Available in fixed-output voltages: 1 to 3.3 V
- High PSRR: 65 dB at 1 kHz
- Active output discharge
3.1.3 LM2842-Q1

Figure 6. Functional Block Diagram of LM2842-Q1

Features:
- The LM2841-Q1 is an automotive grade product that is AEC-Q100 Grade 1 qualified (−40°C to 125°C operating junction temperature)
- Input voltage range: 4.5 to 42 V
- Output current options: 100 mA, 300 mA, and 600 mA
- Feedback pin voltage: 0.765 V
- 550 kHz (X) or 1.25 MHz (Y) switching frequency
- Low shutdown IQ, 16-μA typical
- Short circuit protected
- Internally compensated
- Soft-start circuitry
- Small overall solution size (SOT-6L package)
4 System Design and Component Selection

Table 2 lists the general annotations used in Section 4.

<table>
<thead>
<tr>
<th>ANNOTATION</th>
<th>DESCRIPTION</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_r(t)$</td>
<td>Resolver excitation signal, general form</td>
<td>V</td>
</tr>
<tr>
<td>$V_s(t)$</td>
<td>Resolver SIN output signal, general form</td>
<td>V</td>
</tr>
<tr>
<td>$V_c(t)$</td>
<td>Resolver COS output signal, general form</td>
<td>V</td>
</tr>
<tr>
<td>$V_{OE}$</td>
<td>Differential output voltage from the excitation amplifier</td>
<td>V</td>
</tr>
<tr>
<td>$V_{OE1}$, $V_{OE2}$, $V_{OEx}$</td>
<td>Output voltage from the excitation amplifier referenced to QGND</td>
<td>V</td>
</tr>
<tr>
<td>TS</td>
<td>Resolver transformation ratio</td>
<td>—</td>
</tr>
<tr>
<td>$\theta$</td>
<td>Resolver angle</td>
<td>° or rad</td>
</tr>
<tr>
<td>EXTOUT</td>
<td>DC offset for exciter amplifier, defined in PGA411-Q1 register</td>
<td>V</td>
</tr>
<tr>
<td>$V_{IE1}$, $V_{IE2}$, $V_{IEx}$</td>
<td>Voltage on IE1, IE2 PGA411-Q1 exciter feedback pins</td>
<td>V</td>
</tr>
<tr>
<td>$V_{RES}$</td>
<td>Resolver output voltage on SIN or COS output</td>
<td>V</td>
</tr>
<tr>
<td>$V_{RES}(t)$</td>
<td>Resolver output signal on SIN or COS output, general form</td>
<td>V</td>
</tr>
<tr>
<td>$V_{COM}(t)$</td>
<td>Common mode HF noise picking to the resolver harness</td>
<td>V</td>
</tr>
<tr>
<td>$V_{OCOS}$</td>
<td>Voltage on resolver cosine output (OCOS) pin</td>
<td>V</td>
</tr>
<tr>
<td>(amp)</td>
<td>Subscript for amplitude</td>
<td>—</td>
</tr>
<tr>
<td>(p-p)</td>
<td>Subscript for peak-to-peak value</td>
<td>—</td>
</tr>
<tr>
<td>(RMS)</td>
<td>Subscript for Root-Mean-Square value</td>
<td>—</td>
</tr>
<tr>
<td>(max)</td>
<td>Subscript for maximum value</td>
<td>—</td>
</tr>
<tr>
<td>(min)</td>
<td>Subscript for minimum value</td>
<td>—</td>
</tr>
<tr>
<td>(DC-offset)</td>
<td>Subscript for signal center line (DC offset)</td>
<td>—</td>
</tr>
</tbody>
</table>
4.1 Resolver Basics

The resolver is an angular sensor using the principle of a rotary transformer distributing its magnetic flux into two secondary windings fixed at right (90°) angles to each other. A single-turn resolver provides absolute position over a 360° angle. A resolver needs harmonic excitation $V_R$ (Equation 1) for the primary winding. The angle $\Theta$ is then given by the secondary $V_S$ (Equation 2) and $V_C$ (Equation 3) windings voltage ratio (Equation 4). TS represents a transformation ratio, which is typically in range of 0.35 to 0.5. A simplified electrical schematic for typical resolver is shown in Figure 7.

$$V_R(t) = V_{OE(amp)} \times \sin(\omega t)$$  \hspace{1cm} (1)

$$V_S(t) = TS \times V_{OE(amp)} \times \sin(\omega t) \times \sin \Theta$$  \hspace{1cm} (2)

$$V_C(t) = TS \times V_{OE(amp)} \times \sin(\omega t) \times \cos \Theta$$  \hspace{1cm} (3)

$$\frac{V_S(t)}{V_C(t)} = \frac{TS \times V_{OE(amp)} \times \sin(\omega t) \times \sin \Theta}{TS \times V_{OE(amp)} \times \sin(\omega t) \times \cos \Theta} = \frac{\sin \Theta}{\cos \Theta} = \tan \Theta$$  \hspace{1cm} (4)

$$\Theta = \arctan \left( \frac{V_S(t)}{V_C(t)} \right)$$

Calculating the output angle using arcus tangents method is the traditional way mostly used in microcontroller based solutions. The PGA411-Q1 uses a tracking loop method instead. See the device’s datasheet for further details (SLASE76).

![Figure 7. Resolver Electrical Schematic](image-url)
4.2 Exciter Amplifier

Figure 8 shows typical single-ended (referenced to QGND) waveforms of an exciter amplifier while Figure 9 shows differential representation with Equation 5.

\[ V_{OE} = V_{OE1} - V_{OE2} \]  \hspace{1cm} (5)

![Figure 8. Exciter Amplifier Output Waveforms With Respect to QGND](image)

![Figure 9. Exciter Amplifier Output Waveform as Seen by Resolver](image)
Table 3 and Table 4 describe single-ended and differential voltage levels of the exciter amplifier output, respectively.

### Table 3. Exciter Amplifier Voltage Levels (Single-Ended)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{(p-p)}$</td>
<td>5.65</td>
<td>V</td>
</tr>
<tr>
<td>$V_{(amp)}$</td>
<td>2.83</td>
<td>V</td>
</tr>
<tr>
<td>EXTOUT</td>
<td>(by default) 2.00</td>
<td>V</td>
</tr>
</tbody>
</table>

### Table 4. Exciter Amplifier Voltage Levels (Differential)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{(p-p)}$</td>
<td>11.31</td>
<td>V</td>
</tr>
<tr>
<td>$V_{(amp)}$</td>
<td>5.65</td>
<td>V</td>
</tr>
<tr>
<td>$V_{(RMS)}$</td>
<td>4</td>
<td>V</td>
</tr>
</tbody>
</table>

4.2.1 DC Feedback Signal Path

Resistors in the feedback path for IEx pins keep the signal on a reasonable level. The nominal input impedance of IEx pins is 40 kΩ. The complete feedback path is in Figure 10. Planar resistors in the PGA411-Q1 are referenced as $R_a$ and $R_b$.

The voltage level on IEx pins is defined per Equation 6.

$$V_{IEx} = V_{OE} \frac{R_a + R_b}{R_a + R_b + R_9}$$

(6)
The system is designed to work in 4-V_{RMS} and 7-V_{RMS} modes. The maximum voltage on the OEx pin is defined per Equation 7 where EXTOUT is programmable in the range 0.5 to 2 V, and V_{OEx(p-p)} corresponds to the single-ended peak-to-peak voltage of the excitation signal (see Figure 8).

\[ V_{OEx(max)} = EXTOUT + V_{OEx(p-p)} \]  

(7)

The minimum voltage on OEx pins is defined by EXTOUT only as per Equation 8.

\[ V_{OEx(min)} = EXTOUT \]  

(8)

Combination of Equations Equation 6, Equation 7, and Equation 8 gives the minimum (Equation 9) and maximum (Equation 10) voltage on IEx pins.

\[ V_{IEx(min)} = \frac{EXTOUT \times (R_a + R_b)}{R_a + R_b + R_{9(10)}} \]  

(9)

\[ V_{IEx(max)} = \left( \frac{EXTOUT + V_{p-p}}{R_a + R_b + R_{9(10)}} \right) \times (R_a + R_b) \]  

(10)

Equation 10 and Equation 9 define single-ended constrains for selecting R9 and R10 resistors.

From the excitation waveforms on Figure 8 and Figure 9, the maximum differential voltage between IEx pins is given by Equation 11.

\[ V_R(t) = V_{OE(amp)} \times \sin(\omega t) \]  

(11)

Equation 11 defines differential constrains for selecting R9 and R10 resistors.

**NOTE:** Unless otherwise is noted, all voltages are referenced to QGND.

Table 5 shows IEx input impedance tolerance analysis. Resistor value R9, R10 = 68 k with 1% tolerance corresponds to the TIDA-00796 design.

<table>
<thead>
<tr>
<th>R9, R10 = 68 k</th>
<th>EXTOUT = 2 V</th>
<th>IE1, IE2 INPUT IMPEDANCE</th>
<th>RECOMMENDED VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>IE1, IE2 INPUT IMPEDANCE</td>
<td>MIN 30K</td>
<td>TYP 40K</td>
<td>MAX 50K</td>
</tr>
<tr>
<td>( V_{IEx(min)} )</td>
<td>4 V_{RMS}</td>
<td>0.61</td>
<td>0.74</td>
<td>0.85</td>
</tr>
<tr>
<td></td>
<td>7 V_{RMS}</td>
<td>0.61</td>
<td>0.74</td>
<td>0.85</td>
</tr>
<tr>
<td>( V_{IEx(max)} )</td>
<td>4 V_{RMS}</td>
<td>2.13</td>
<td>2.57</td>
<td>2.94</td>
</tr>
<tr>
<td></td>
<td>7 V_{RMS}</td>
<td>3.64</td>
<td>4.41</td>
<td>5.04</td>
</tr>
<tr>
<td>( V_{IEx(diff-max)} )</td>
<td>4 V_{RMS}</td>
<td>1.52</td>
<td>1.83</td>
<td>2.1</td>
</tr>
<tr>
<td></td>
<td>7 V_{RMS}</td>
<td>3.03</td>
<td>3.67</td>
<td>4.19</td>
</tr>
</tbody>
</table>

The TIDA-00796 is designed to be functional in 4-V_{RMS} mode in any condition and in 7-V_{RMS} for typical input impedance. Exceeding \( V_{IEx(max)} \) causes signal clipping on IEx pins, although static performance of the chip changes only slightly.
4.2.2 AC Signal Path

C17 and C19 together with R9 and R10 form a low-pass filter for each signal path. Such a filter reduces noise infiltration in the tracking loop. Select the cutoff point of the filter according to the excitation frequency. Start with a –3-dB cutoff point frequency three times bigger than the excitation frequency. The roll-off point for the low-pass filter is defined per Equation 12. It is important to take Ra and Rb loading effect into account.

\[
f_{-3\,\text{dB}} = \frac{R_{9(10)} + R_a + R_b}{2 \times \pi \times (R_a + R_b) \times C_{17(19)}}
\]  

(12)

The TIDA-00796 has roll-off point set to 92.93 kHz. The signal attenuation at a default 10-kHz excitation frequency is approximately 50 mdB, which corresponds to the scale factor of 0.994.

4.2.3 Protection Circuit

The PGA411-Q1 exciter amplifier is protected against undervoltage, overvoltage, mutual short, short to power, short to ground, and overcurrent. The TIDA-00796 uses only four Schottky diodes (D9, D10, D12, and D13) for board-level ESD protection.

4.2.4 Design Notes

Do not assemble C41 and C18. R7 and R8 are for debugging purposes only. Omit these components in the final design. The TIDA-00796 exciter output implementation is shown on Figure 11.

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**Figure 11. TIDA-00796 Exciter Output Implementation**
4.3 **AFE**

### 4.3.1 AFE Waveforms

Figure 12 shows typical resolver output waveforms. $V_{\text{RES}}$ represents the actual resolver signal, $V_a(t)$ or $V_c(t)$. Signals $V_a$ and $V_b$ are single-ended signals as seen by the AFE input. Amplitude asymmetry as well as DC bias offset are discussed in Section 4.3.2.

![Figure 12. Typical Resolver Output Waveforms](image)

### 4.3.2 DC Signal Path

Typically, SIN and COS signal paths are identical. For this reason, the following text refers to the COS signal path only. Figure 13 shows simplified signal path as an example.

<table>
<thead>
<tr>
<th>GAIN $^*$</th>
<th>$R_g$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.75</td>
<td>15 kΩ</td>
</tr>
<tr>
<td>1</td>
<td>20 kΩ</td>
</tr>
<tr>
<td>2.25</td>
<td>45 kΩ</td>
</tr>
<tr>
<td>3.5</td>
<td>70 kΩ</td>
</tr>
</tbody>
</table>

The signal from the resolver secondary winding is floating. Resistors $R_{12}$ and $R_{21}$ help to provide appropriate DC biasing. Start by taking the recommended values from the PGA411-Q1 datasheet (SLASE76).

![Figure 13. AFE Signal Path](image)
The first effect of resistors R12 and R21 is the DC offset (with respect to QGND) for lIZx signals. The easiest way how to understand this is to take the moment when the input sine wave amplitude is zero. The voltage source with zero voltage is a short circuit, thus R12 and R21 form a simple resistor divider (omitting loading effect) as shown in Figure 14.

![Figure 14. DC Biasing Simplified](image)

Current flowing in such a circuit is given by Equation 13.

\[
i(t) = \frac{V_{PSV\_FE} - V_{res}(t)}{R_{12} + R_{21}}
\]  


Voltage at point B is given by Equation 14. Voltage at point A is given by Equation 15.

\[
V_B = \left( \frac{V_{PSV\_FE} - V_{res}(t)}{R_{12} + R_{21}} \right) \times R_{21} = \frac{V_{PSV\_FE} \times R_{21}}{R_{12} \times R_{21}} - V_{res}(t) \frac{R_{21}}{R_{12} + R_{21}}
\]

\[
V_A = V_B + V_{res}(t) = \frac{V_{PSV\_FE} \times R_{21}}{R_{12} + R_{21}} - V_{res}(t) \left( \frac{R_{21}}{R_{12} + R_{21}} + V_{res}(t) = \frac{V_{PSV\_FE} \times R_{21}}{R_{12} + R_{21}} + V_{res}(t) \left( 1 - \frac{R_{21}}{R_{12} + R_{21}} \right) \right)
\]

where \( \frac{V_{PSV\_FE} \times R_{21}}{R_{12} + R_{21}} \) represents the DC offset.

R12 and R21 do not only affect DC biasing but also signal amplitude at point A and B. However, previous equations completely omit the loading effects of R15, R16, R17, R18, R_{g}, and \( V_{COMAFE} \) but give raw imagination of signal levels in the circuit. See Section 4.2.4 for more details.
Resistors R15, R16, R17, and R18 set the proper gain of the AFE as seen on Figure 15. The difference amplifier is symmetric, where R15 = R17 and R16 = R18. Voltage gain is defined per Equation (16).

\[ G = \frac{V_{OCOS}}{V_{res}} = \frac{R_f}{R_f + R_{15} + R_{16}} \tag{16} \]

The AFE DC gain for the TIDA-00796 is set to:

\[ G = \frac{20 \text{ k}}{20 \text{ k} + 27 \text{ k} + 27 \text{ k}} = 0.270 \]  

Table 6 shows signals levels for the TIDA-00796. When the gain of the internal difference amplifier is set to \( G = 1 \), the voltage swing on IZx inputs corresponds to the output voltage (OCOS) swing. When other gain is selected, Equation 18 applies where \( G \) is the overall gain and \( G_{INT} \) is the gain set in the DEV_AFE_CFG register.

\[ V_{IZx} = \frac{V_{res} \times G}{G_{INT}} \tag{18} \]

Table 6. Voltage Swing on AFE Input and Output

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>MODE</th>
<th>TRANSFORMATION RATIO TS</th>
<th>RECOMMENDED VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{RES(p-p)} )</td>
<td>4 \text{ V}_{\text{RMS}}</td>
<td>3.95</td>
<td>5.66</td>
<td>6.79</td>
</tr>
<tr>
<td></td>
<td>7 \text{ V}_{\text{RMS}}</td>
<td>6.93</td>
<td>9.90</td>
<td>11.88</td>
</tr>
<tr>
<td>( V_{IZx(p-p)} )</td>
<td>4 \text{ V}_{\text{RMS}}</td>
<td>1.06</td>
<td>1.53</td>
<td>1.83</td>
</tr>
<tr>
<td></td>
<td>7 \text{ V}_{\text{RMS}}</td>
<td>1.87</td>
<td>2.67</td>
<td>3.21</td>
</tr>
<tr>
<td>( V_{OCOS(p-p)} )</td>
<td>4 \text{ V}_{\text{RMS}}</td>
<td>1.06</td>
<td>1.53</td>
<td>1.83</td>
</tr>
<tr>
<td></td>
<td>7 \text{ V}_{\text{RMS}}</td>
<td>1.87</td>
<td>2.67</td>
<td>3.21</td>
</tr>
</tbody>
</table>

\(^{(1)}\) Internal gain = 1

Take into account these three design constrains:
1. OSIN and OCOS pins are referenced to internal COMAFE = 2.5 V. Voltage swing on these pins must remain between 0.5 to 4.5 V \( (V_{OS}, V_{OC} \) in the PGA411-Q1 datasheet).
2. Differential input voltage swing \( V_{IZx(p-p)} \) must be between 0.188 to 3 V.
3. The signal on IZx pins referenced to QGND must be between 0.5 to 4.5 V. R12 and R21 help achieve this without affecting the overall gain.

The red highlighted value in Table 6 exceeds the recommended range. Overall gain must be modified for resolvers with higher transformation ratio.
4.3.3 AC Signal Path

The TIDA-00796 uses two AFE filter stages:

- The recommended filtering for PGA411-Q1 is required to meet the chip specification
- The application specific filter stage improves EMC robustness, especially when long resolver leads are used. This filter is optional on the PCB and may be bypassed by R13, R20 and R29, R36. The design of this filter is not a part of this design guide.

4.3.3.1 Recommended Filtering for PGA411-Q1

Each stage contains a differential and common-mode filter to reduce noise and improve the overall performance of the chip.

Common-mode filter topology is shown in Figure 16. Take IZx input impedance into account. For DC analysis, non-inverting inputs IZ3 and IZ4 have an input impedance defined as Rf+Rg, the input impedance of the IZ1, IZ2 pins is given only by Rg. This difference applies only if both IZx pins are investigated separately. However, it also means changing VRES(t) differential voltage. To determine the cut-off frequency, the differential voltage must remain constant (for example, 0 V). That corresponds to zero voltage on the op amp output, and both inputs then see the Rf+Rg input impedance with reference to the ground.

![Figure 16. AFE Common-Mode Input Filter](image)

The transfer function of a loaded RC low-pass filter on the Figure 16 is defined as per Equation 19. For jω = 0, the transfer function corresponds to a simple voltage divider as is expected.

\[
H(j\omega) = \frac{R_f + R_g}{(R_f + R_g) + (R_f + R_g)j\omega C_{23} + 1} \times (R_{15} + R_{16})
\]  

(19)

The –3-dB cutoff frequency is defined at the point where the magnitude of the power drops to half of the DC value. At this point, voltage transfer drops to \(1/\sqrt{2}\) as per Equation 20:

\[
|H(j\omega)| = \frac{1}{\sqrt{2}} \times H(0)
\]  

(20)

Solving Equation 19, where \(\omega = 2\pi f\) defines the angular frequency, returns the cutoff frequency as per Equation 21.

\[
f_{I Z_{1\text{, commune}}(-3\text{ dB})} = \frac{(R_f + R_g) + (R_{15} + R_{16})}{2 \times \pi \times (R_{15} + R_{16}) \times (R_f + R_g) \times C_{23}}
\]  

(21)

The common-mode cut-off frequency for the TIDA-00796 is 101.8 kHz.

Differential filter topology consists of R15, R16, R17, R18, C26, C23, and C29. The common-mode filter capacitors directly impact the differential filter cutoff frequency. Placing capacitor C26 between the R15, R16 and R17, R18 pairs gives additional flexibility to set optimal cutoff frequencies for both.
The topology of the differential filter is shown in Figure 17. The differential IZx input impedance is defined as \(2 R_g\) because there is ideally a zero-voltage difference between the op amp inputs due to the negative feedback. The filter is symmetric and can be simplified for evaluation as shown in Figure 18.

However, a second-order RC filter with DC load brings a very complex cutoff frequency formula and circuit simulator for the analysis is recommended instead.

### 4.3.3.2 Application Specific Filter Stage

This design guide does not have a detailed design of this filter. R13, R20 together with C24, C30 set the common-mode cutoff frequency while C27 sets the differential frequency. However, R13 and R20 also have directly impact the overall DC gain. An alternate way may be using common-mode choke L3, to which DC resistance is not significant. C27 and C28 must be then used to provide the path of the AC current return to compensate the choke’s finite coupling factor. Consider the filter loading effect while calculating cutoff frequencies.

### 4.3.4 Protection Circuit

Analogous to the exciter amplifier, the PGA411-Q1 IEx pins are internally protected from undervoltage, overvoltage, mutual short, short to power, short to ground, and overcurrent. The TIDA-00796 uses only four Schottky diodes (D14, D15, D16, and D17 for COS or D18, D19, D20, and D21 for SIN) for board-level ESD protection. Additional protection circuits are application specific. Use external transient protection such as MOVs or TVSs in harsh environments.
### 4.3.5 Design Notes

A good understanding of the AFE signal path is very important. The right formulas help to set the correct diagnostic thresholds for the system, which are critical in safety applications. However, some mathematical expressions are very complex and using the right simulation software such as TINA-TI is more productive. Figure 19 shows a typical simulation example with the components selection corresponding to the TIDA-00796.

![Figure 19. TINA-TI Simulation Circuit for AFE DC Analysis](image)

Figure 19 shows the resolver output signal (10 kHz, 7 V\textsubscript{RMS}, TS = 0.5) and OCOS monitor output. The result corresponds to Table 6.

![Figure 20. Signal From Resolver (V\textsubscript{RES}) versus Output Cosine Signal (V\textsubscript{OCOS})](image)
Figure 21 shows an AC analysis of the AFE differential filter. The cutoff frequency is at 56.69 kHz with a –40-dB roll-off per decade (second-order filter).

Figure 21. AFE Differential Filter Analysis

Figure 22 shows an AC analysis of the AFE common-mode filter. The cutoff frequency is at 101.58 kHz with a –20-dB roll-off per decade (first-order filter).

Figure 22. AFE Common-Mode Filter Analysis
Figure 23 shows the AFE implementation in the TIDA-00796. An application specific filter is not implemented. Capacitors C28 and C37 provide an AC current return path.

Figure 23. TIDA-007496 AFE Schematics
4.4 Power Supplies

The TIDA-00796 has three different power supplies on the board:

- Auxiliary step-down DC-DC converter to power the board when supplying from external voltage from 7 to 42 V
- Linear regulator (LDO) for digital logic
- Step-up converter for the exciter amplifier

4.4.1 Auxiliary Step-Down DC-DC Converter

A complete circuit diagram of the converter is shown in Figure 24. Diode D1 provides reverse polarity protection and diode D2 basic transient and overvoltage protection. Input capacitors C2, C3 are optimized for input voltage range and output current of the converter (SLTA055). Resistor R1 and capacitor C7 defines the soft-start constant, which varies with the input voltage. Capacitor C1 is a bootstrap capacitor. Consider the maximum voltage rating for this capacitor. Feedback resistor dividers R2 and R5 program the output voltage. Diode D5, inductor L1, and output capacitors C4, C5, and C6 are parts of the step-down switching topology. Capacitor C4 is placed as short to L1 and D5 as possible to reduce HF switching noise. Capacitors C5 and C6 store energy from the inductor. This altogether has as short current loop given by the PCB layout as possible.

A selected step-down regulator with a switching frequency of 550 kHz allows using inductor L1 type to be same as the inductor used in the step-up converter. For a given input voltage range, the step-down converter operates in constant conduction mode with an output current above 100 mA.

![Figure 24. Auxiliary Step-Down DC-DC Converter](image-url)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage range</td>
<td>7 to 42 V</td>
<td>V</td>
</tr>
<tr>
<td>Output voltage</td>
<td>typ. 5 V</td>
<td>V</td>
</tr>
<tr>
<td>Switching frequency</td>
<td>550 kHz</td>
<td></td>
</tr>
<tr>
<td>Output current</td>
<td>max. 600 mA</td>
<td></td>
</tr>
</tbody>
</table>
4.4.2 Linear Regulator (LDO)

The digital logic is powered from the TLV713P-Q1 family linear regulator. A circuit diagram for the linear regulator is shown in Figure 25.

**Figure 25. LDO**

4.4.3 Step-up Converter

Figure 26 shows a step-up converter that provides voltage for the exciter amplifier. The converter is controlled by the internal circuitry in the PGA411-Q1. Resistor R38 is for debugging purposes only. Components C14, L2, D8, C15, and C16 are parts of the step-up converter topology and must be located in close proximity. Switch and the feedback divider are integrated in the PGA411-Q1. Output voltage is programmable in the DEV_CONFIG1 register bits MODEVEXT. All component values are selected according to the PGA411-Q1 datasheet (SLASE76). This allows constant conduction operation in most PGA411-Q1 operation modes. Diode D11 is optional switch protection and is not needed if proper layout practices are maintained. Capacitor C15 is placed as short to D8 and C14 as possible to reduce HF switching noise. Output capacitor C16 stores energy from the inductor. Capacitor C40 is optional when external power supply is used. However, in this condition, the step-up converter remains operational. Switching frequency is typically 414 kHz with a 10% spread spectrum modulation.

**Figure 26. Step-up Converter for Exciter Amplifier**
### Table 8. Technical Parameters of Step-up Converter

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage range</td>
<td>4.75 to 8.5</td>
<td>V</td>
</tr>
<tr>
<td>Output voltage</td>
<td>Software adjustable, 12 to 18</td>
<td>V</td>
</tr>
<tr>
<td>Switching frequency</td>
<td>414 ± 10 % modulation</td>
<td>kHz</td>
</tr>
<tr>
<td>Output current</td>
<td>Internally limited by switch capability see the datasheet.</td>
<td>mA</td>
</tr>
<tr>
<td>Efficiency</td>
<td>See Figure 49</td>
<td></td>
</tr>
<tr>
<td>Output ripple</td>
<td>typ. &lt; 40 mV</td>
<td>mV</td>
</tr>
</tbody>
</table>

#### 4.5 Host Interface

The PGA411-Q1 is interfaced to the host system through four different channels:

- SPI is mandatory to configure the PGA411-Q1
- GPIOs for additional signals such as RESET, FAULTRES, and so on
- PARALLEL high throughput data interface to, for example, an FPGA
- ANALOG for redundant signal path

#### 4.5.1 SPI

SPI on the PGA411-Q1 uses a standard four-wire interface and a clock frequency up to 8 MHz.

- NCS: Chip select. The PGA411-Q1 ignores all communication when the pin is logic high.
- SCLK: SPI clock signal
- SDI: The PGA411-Q1 SPI data input. Also referenced to MOSI (master out, slave in)
- SDO: The PGA411-Q1 SPI data output. Also referenced to MISO (master in, slave out)

The default configuration of SPI is:

- CPOL = 0: Clock idle state is logic low
- CPHA = 1: Data are captured on a falling edge

The PGA411-Q1 differentiates read or write operations depending on the register address. Every access must contain a right CRC-6 checksum. The checksum is calculated from the first three bytes (address and data).

A real-life example of SPI transfer is shown in Figure 27. Figure 27 represents writing a 0x8FC0 value to the DEV_OVUV1 register. The complete 32b packet corresponds to 0x878FC019 where 0x87 represents the DEV_OVUV1 write address, 0x8FC0 are data to be written, and 0x19 is CRC-6. Bytes are transferred from the most significant to the least significant. The PGA411-Q1 returns content of the previously accessed register. This content is usually discarded after the write operation unless a safety check during sequential write is implemented.

![Figure 27. Example SPI Write Operation](image-url)
Read operation comes in two phases. The first is a dummy read, which sets the internal register pointer of the PGA411-Q1 to the desired DEV_OVUV2 register (Figure 28). A complete 32b packet corresponds to 0x6B00F000. 0x6B is DEV_OVUV2 read address, 0x00F0 is SPI dummy content, and 0x00 is CRC-6. Return data from this read corresponds to the register, which has been read previously and can be discarded.

The second read operation on Figure 29 returns the content of the desired register. A complete 32b packet is identical with the previous read. This time, the PGA411-Q1 returns content of the desired DEV_OVUV2 register because this location was accessed in the previous access.

**NOTE:** Some registers must be unlocked before accessing. See the PGA411-Q1 datasheet for further details (SLASE76).

---

**Figure 28. Dummy Read Access**

**Figure 29. Second Phase of Read Operation**

### 4.5.2 GPIO

The host controller general purpose input output (GPIO) pins are used for interfacing the PGA411-Q1. The TIDA-00796 uses the following signals (signal direction is referenced to the PGA411-Q1):

- **ECLKSEL:** Clock oscillator select input. Internal oscillator is selected when the signal is low.
- **FAULTRES:** Fault reset input. Faults are cleared on the signal transition from high to low. Holding the signal low masks all faults.
- **OUTA, OUTB, OUTZ:** Incremental encoder outputs, which can be processed by eQEP periphery in the C2000™ controller
- **BMODE0:** Resolution select input. 10b (BMODE0 = low) or 12b (BMODE0 = high) operation
- **AMODE:** Accelerated mode input. Accelerated mode is enabled when the signal is logic high
- **FAULT:** Fault detection signal output. The pin uses open collector output. The signal is low when no fault is detected. External pullup resistor is required.
- **PRD:** Data parity check output, mostly used with the parallel interface
- **RESET_N:** The PGA411-Q1 reset input. Reset is active low.
- **INHB:** Input signal to low allows to freeze data (data hold) on the parallel interface.
- **OMODE:** Data output format select input. Pulling the signal enables PGA411-Q1 encoder emulated mode.
- **VA0, VA1:** Data output select input for angle and velocity (see the PGA411-Q1 datasheet [SLASE76]).
4.5.3 Parallel

A parallel interface provides highest data throughput and update rate. It is best for interfacing with programmable logic such as FPGA. Corresponding signals are:

- ORD[0-11]: Parallel data output for angle and velocity
- ORD[12]: Unused
- ORD[13]: Parallel interface clock output

INHB, OMODE, VA0 and VA1 signals affect parallel interface behavior. See the datasheet for further details.

**NOTE:** SPI is used to configure the PGA411-Q1 even when parallel interface is used.

4.5.4 Analog

The PGA411-Q1 has several analog outputs, which help with debugging and may also provide an alternate single-ended signal path to the host microcontroller. The TIDA-00796 reference design wires these signals to corresponding test points on the PCB.

- COMAFE (TP2): Common-mode output for the AFE, typ. 2.5 V
- ORS (TP3): Internal-exciter signal-reference output (exciter preamplifier out), which provides support for optional external exciter amplifier
- AOUT (TP4): Analog representation of the angle and velocity with 10b resolution
- OCOS (TP5): Single-ended (referenced to QGND) resolver cosine output
- OSIN (TP6): Single-ended (referenced to QGND) resolver sine output

4.6 Visual Indicator and Fault Reset

The TIDA-00796 has three LEDs. Two green LEDs (D3, D4) show the presence of 5-V and 3.3-V rail voltages as shown in Figure 30.

**Figure 30. Power-Good Signalization on TIDA-00796**

*Used LEDs (Wurth) are very bright even at 1 mA
Copyright © 2016, Texas Instruments Incorporated*
When a fault condition is reported by the PGA411-Q1, the red LED D6 turns on. The fault signal is an open-collector type. For that reason, the signal is buffered by the configurable multiple-function gate SN74LVC1G97. An internal logic diagram of the gate is shown in Figure 31. The chip provides up to nine different logic operations with regards to the used input configuration. See the device’s product page for further information (http://www.ti.com/product/SN74LVC1G97).

![Figure 31. Logic Diagram of SN74LVC1G97](image)

The TIDA-00796 uses buffer configuration of the SN74LVC1G97 as shown in Figure 32.

![Figure 32. TIDA-00796 FAULT Signalization](image)

The FAULT condition can be reset using a software controlled FAULTRES signal or manually by pressing the FAULTRES button S1.
4.7 PGA411-Q1 Subsystem

Figure 33 shows the overall PGA411-Q1 subsystem and how it is implemented in the TIDA-00796. An analog supply is generated from a P5V rail. Capacitors C11, C12, and C13 and ferrite bead FB1 form a low-pass filter and effectively separate sensitive analog circuitry from the general 5-V power supply rail. Capacitor C20 is output capacitor for the internal voltage regulator. Bypass capacitors C21 and C22 are located as close the PGA411-Q1 as possible. Crystal oscillator Y1 together with load capacitors C33 and C34 provide a clock signal to the PGA411-Q1. Bypass capacitors C40 and C25 are optional. The 10k pullup or pull-down resistors ensure defined reset value when the host microcontroller has GPIO pins in a high-impedance state.

Figure 33. PGA411-Q1 Subsystem
5 Getting Started Hardware

Figure 34 shows a photo of the top side of the TIDA-00796, highlighting important connectors and jumpers. For each connector, the pin “1” is highlighted with a small triangle on the service print or with a square in the case of J4 and J5.

Table 9. Host Processor Interface Connectors J4, J5 (Top View Corresponding to Figure 34)

<table>
<thead>
<tr>
<th>J4</th>
<th>PIN</th>
<th>DESCRIPTION</th>
<th>PIN</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>Not connected</td>
<td>1</td>
<td>Not connected</td>
</tr>
<tr>
<td>3</td>
<td>2</td>
<td>Not connected</td>
<td>4</td>
<td>Not connected</td>
</tr>
<tr>
<td>5</td>
<td>3</td>
<td>BMODE0</td>
<td>6</td>
<td>Not connected</td>
</tr>
<tr>
<td>7</td>
<td>4</td>
<td>ECLKSEL</td>
<td>8</td>
<td>VUSB</td>
</tr>
<tr>
<td>9</td>
<td>5</td>
<td>FAULTRES</td>
<td>10</td>
<td>SDO</td>
</tr>
<tr>
<td>11</td>
<td>6</td>
<td>Not connected</td>
<td>11</td>
<td>PRD</td>
</tr>
<tr>
<td>13</td>
<td>7</td>
<td>AMODE</td>
<td>12</td>
<td>SDI</td>
</tr>
<tr>
<td>15</td>
<td>8</td>
<td>Not connected</td>
<td>13</td>
<td>RESET_N</td>
</tr>
<tr>
<td>16</td>
<td>9</td>
<td>FAULT</td>
<td>14</td>
<td>GND</td>
</tr>
<tr>
<td>16</td>
<td>10</td>
<td>OUTB</td>
<td>15</td>
<td>Not connected</td>
</tr>
<tr>
<td>16</td>
<td>11</td>
<td>SCLK</td>
<td>16</td>
<td>GND</td>
</tr>
<tr>
<td></td>
<td>12</td>
<td>OUTZ</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Figure 34. TIDA-00796 Board

External Voltage Supply 7 - 42 V
Fault reset button
External Voltage Supply 7 - 42 V
Fault reset button
### Table 10. Parallel Interface Connector J3

<table>
<thead>
<tr>
<th>PIN</th>
<th>DESCRIPTION</th>
<th>PIN</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>INHB</td>
<td>2</td>
<td>ORD8</td>
</tr>
<tr>
<td>3</td>
<td>GND</td>
<td>4</td>
<td>ORD7</td>
</tr>
<tr>
<td>5</td>
<td>GND</td>
<td>6</td>
<td>ORD6</td>
</tr>
<tr>
<td>7</td>
<td>GND</td>
<td>8</td>
<td>ORD5</td>
</tr>
<tr>
<td>9</td>
<td>OMODE</td>
<td>10</td>
<td>ORD4</td>
</tr>
<tr>
<td>11</td>
<td>GND</td>
<td>12</td>
<td>ORD3</td>
</tr>
<tr>
<td>13</td>
<td>VA0</td>
<td>14</td>
<td>ORD2</td>
</tr>
<tr>
<td>15</td>
<td>GND</td>
<td>16</td>
<td>ORD1</td>
</tr>
<tr>
<td>17</td>
<td>VA1</td>
<td>18</td>
<td>ORD0</td>
</tr>
<tr>
<td>19</td>
<td>GND</td>
<td>20</td>
<td>ORD13</td>
</tr>
<tr>
<td>21</td>
<td>ORD9</td>
<td>22</td>
<td>ORD12</td>
</tr>
<tr>
<td>23</td>
<td>ORD10</td>
<td>24</td>
<td>ORD11</td>
</tr>
</tbody>
</table>

### Table 11. Resolver Connector J7

<table>
<thead>
<tr>
<th>PIN</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>EXC–</td>
</tr>
<tr>
<td>2</td>
<td>EXC+</td>
</tr>
<tr>
<td>3</td>
<td>COS–</td>
</tr>
<tr>
<td>4</td>
<td>COS+</td>
</tr>
<tr>
<td>5</td>
<td>SIN–</td>
</tr>
<tr>
<td>6</td>
<td>SIN+</td>
</tr>
</tbody>
</table>

### Table 12. Jumper J2, J6 Configuration

<table>
<thead>
<tr>
<th>HEADER</th>
<th>PINS</th>
<th>SETTING</th>
</tr>
</thead>
<tbody>
<tr>
<td>J2</td>
<td>1-2</td>
<td>The board is powered from the host processor interface connector (for example, USB)</td>
</tr>
<tr>
<td></td>
<td>2-3</td>
<td>The board is powered from external supply</td>
</tr>
<tr>
<td>J6</td>
<td>1-2</td>
<td>The exciter amplifier is powered from integrated step-up converter</td>
</tr>
</tbody>
</table>
|        | 2-3  | The exciter amplifier is powered from external voltage supply  
**CAUTION:** In this configuration input voltage must not exceed VEXT maximum ratings |

**NOTE:** Some USB ports may not deliver sufficient power during the device startup. A voltage drop on the power rail or USB cable can cause spurious controller reset. In such a case, use the external power supply.
5.1 TIDA-00796 controlSTICK Interfacing

The TIDA-00796 is preferred to be used with the F28069 controlSTICK as seen on Figure 35. The controlSTICK does not have 5 V from the USB available on the output connector by default. When the reference design is being powered from USB then a 0-Ω resistor R15 must be manually assembled as on Figure 36.

NOTE: If planning to run standalone application from FLASH memory, remove R9.
5.2 **TIDA-00796 LaunchPad XL Interfacing**

Figure 37 shows the reference design interfacing with the C2000 LaunchPad XL. An additional PCB adapter is needed. Design data for the adapter is part of the TIDA-00796 design files.

This configuration allows easy host interface signals probing with a logic analyzer or oscilloscope. The adapter contains two additional LEDs and a button connected to the C2000 GPIO pins, which, if needed, can be used for system debugging.

![Figure 37. Interfacing TIDA-00796 With C2000 LaunchPad XL](image)

**NOTE:**

C2000 LaunchPad XL power supplies do not provide sufficient current for the TIDA-00796 startup. Use an external power supply for the reference design when the C2000 LaunchPad XL is used.

5.2.1 **TIDA-00796 First Powering**

Follow these steps while first powering the reference design:

1. Check J2, J6 configuration.
2. Verify that J4-J5 connector is plugged into the host system with the right orientation and alignment.
3. Plug in a USB cable to the host system and to the PC.
4. Turn on an external power supply (if used).
5. Check that two green LEDs on the reference design are lit.
6. Continue to Section 6.

5.3 **Resolver Wiring Errors**

Changing a resolver wiring directly impacts the PGA411-Q1 readout value. The change can be also intentional to customize a system behavior. The effect of the wiring change is described in the following subsections.

**NOTE:**

The original angle in the following tables is set to 10° to reduce confusion and to understand counting up, down, and quadrants mirroring.

- CW: Clockwise
- CCW: Counter clockwise
5.3.1 Signal Polarity Reversal

Signal polarity reversal is swapping two wires within the same pair. The effects of such a reversal are listed in Table 13.

Table 13. Effects of Signal Polarity Reversal

<table>
<thead>
<tr>
<th>CASE</th>
<th>SIGNAL PAIRS CONNECTION</th>
<th>OUTPUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>polarity: normal</td>
<td>EXC</td>
</tr>
<tr>
<td></td>
<td>SYSTEM</td>
<td>RESOLVER</td>
</tr>
<tr>
<td>2</td>
<td>polarity: normal</td>
<td>EXC</td>
</tr>
<tr>
<td>3</td>
<td>polarity: reversed</td>
<td>EXC</td>
</tr>
<tr>
<td>4</td>
<td>polarity: reversed</td>
<td>EXC</td>
</tr>
<tr>
<td>5</td>
<td>polarity: reversed</td>
<td>EXC</td>
</tr>
<tr>
<td>6</td>
<td>polarity: reversed</td>
<td>EXC</td>
</tr>
<tr>
<td>7</td>
<td>polarity: reversed</td>
<td>EXC</td>
</tr>
<tr>
<td>8</td>
<td>polarity: reversed</td>
<td>EXC</td>
</tr>
</tbody>
</table>

5.3.2 COS-SIN Pairs Swap With Possible Polarity Reversal

Table 14 describes complex wiring errors when SIN and COS input are swapped while single wires within the pair are also swapped.

Table 14. COS-SIN Wire Pairs Swap With Possible Polarity Reversal

<table>
<thead>
<tr>
<th>CASE</th>
<th>SIGNAL PAIRS CONNECTION</th>
<th>OUTPUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>9</td>
<td>polarity: normal</td>
<td>EXC</td>
</tr>
<tr>
<td></td>
<td>SYSTEM</td>
<td>RESOLVER</td>
</tr>
<tr>
<td>10</td>
<td>polarity: normal</td>
<td>EXC</td>
</tr>
<tr>
<td>11</td>
<td>polarity: normal</td>
<td>EXC</td>
</tr>
<tr>
<td>12</td>
<td>polarity: normal</td>
<td>EXC</td>
</tr>
<tr>
<td>13</td>
<td>polarity: reversed</td>
<td>EXC</td>
</tr>
<tr>
<td>14</td>
<td>polarity: reversed</td>
<td>EXC</td>
</tr>
<tr>
<td>15</td>
<td>polarity: reversed</td>
<td>EXC</td>
</tr>
<tr>
<td>16</td>
<td>polarity: reversed</td>
<td>EXC</td>
</tr>
</tbody>
</table>
5.3.3 Industry Standard Resolver Wires Color Coding

Table 15 shows colors of typical resolver wires.

Table 15. Color Coding of Resolver Wires

<table>
<thead>
<tr>
<th>WIRE</th>
<th>COLOR</th>
</tr>
</thead>
<tbody>
<tr>
<td>Excitation +</td>
<td>Red – White</td>
</tr>
<tr>
<td>Excitation –</td>
<td>Black – White</td>
</tr>
<tr>
<td>Cos +</td>
<td>Red</td>
</tr>
<tr>
<td>Cos –</td>
<td>Black</td>
</tr>
<tr>
<td>Sin +</td>
<td>Yellow</td>
</tr>
<tr>
<td>Sin –</td>
<td>Blue</td>
</tr>
</tbody>
</table>

NOTE: Always verify wire color with the resolver documentation.
6 Getting Started Firmware

The TIDA-00796 reference design can be used with two different firmware packages written in C programming language:

- Attached TIDA-00796 firmware for controlSTICK
- Reusing TIDA-00363 firmware for C2000 LaunchPad XL (adapter needed)

6.1 TIDA-00796 Firmware Package

The provided example code is easy to understand, module oriented, and lightweight with a small memory footprint.

The package contains a whole Code Composer Studio™ (CCS) project folder, binary file, and the source code. The project folder contains a pre-built output file, which can be directly programmed to the C28069 controlSTICK microcontroller FLASH memory without additional compiling.

6.1.1 TIDA-00796 Firmware Description

The firmware uses a virtual serial port to periodically print read out angle and velocity on the PC.

There are three basic modules that communicate together with defined interface or macros:

- main (main.c, main.h) – main program loop, which calculates readout values and prints them on the PCB using VT100 terminal.
- pga411 (pga411.c, pga411.h) – a hardware independent device driver for the PGA411-Q1. The driver contains registers definition, default configuration, CRC-6 calculation, unlock routines, and so on.
- hal (hal.c, hal.h) – Hardware Abstraction Layer for the C2000 F28069 controller. This is the lowest level source code for interfacing with the controller registers and peripheries. The code must be rewritten while keeping the interface functions if a different microcontroller is intended to be used.

The project folder contains also additional files with register definitions (lib_v150 folder), delay functions F2806x_usDelay.asm, or linker script files. A simplified flowchart for TIDA-00796 firmware is shown on Figure 38.
NOTE: The CCS project contains two build configurations. "DEBUG" is for code execution from RAM memory while "Release" is configured for code execution from FLASH memory.
6.1.2 F28069 controlSTICK FLASH With TIDA-00796 Firmware

The source code package contains a pre-built binary file for the C28069 controlSTICK with standalone TIDA-00796 application firmware.

The easiest way to program the controlSTICK with the TIDA-00796 firmware is using the CCS UniFlash utility from TI (http://www.ti.com/tool/uniflash). Follow these steps:

1. Install CCS UniFlash from TI's webpage.
2. Download the TIDA-00796 CCS project and extract the ZIP file to a location.
3. Plug in the controlSTICK with the TIDA-00796 connected to the USB connector.
4. Open CCS UniFlash.
5. In CCS UniFlash, go to File → Open Configuration → browse for the file "F28069_ctrlSTK.ccxml" from the location previously used. Then, confirm the selection by clicking OK.
6. In the Programs section, add the TIDA-00796-LIGHT.out file from the “Release” folder as shown in Figure 39.
7. Click on the Program button.
8. Wait until programming is finished and then unplug and plug back in the controlSTICK to the USB port.
9. Wait for the red LED to blink on the controlSTICK board, which signals a successful programming.

Troubleshooting tips:
• Check that the resistor R9 is removed from the controlSTICK.
• Check in device manager that all device drivers are installed.
• Use only high quality USB cables.
• Check that the TIDA-00794 is properly connected with the controlSTICK board.

Figure 39. Programming controlSTICK With TIDA-00796 Firmware
6.1.3 PC Terminal Interfacing

A serial terminal supporting VT100 commands is used to interface the TIDA-00796. An open-source Tera Term project is used as an example (http://ttssh2.osdn.jp).

To connect the TIDA-00796 to the PC:
1. Check that the controlSTICK is successfully programmed and the red LED is blinking.
2. Identify the virtual serial port number in the device manager as shown in Figure 40.

3. Open Tera Term, go to Setup → Serial Port. Ensure that the settings correspond to Figure 41 where "Port" has the number from Step 2.

Figure 40. Identifying Virtual Serial Port Number in Device Manager (Windows 7®)

Figure 41. Serial Port Settings in Tera Term
4. In Tera Term, go to Setup → Terminal to check the terminal settings as shown in Figure 42.

![Terminal Settings in Tera Term](image)

**Figure 42. Terminal Settings in Tera Term**

5. If Tera Term is set up properly, a window displays angle and velocity as shown in Figure 43. The refresh rate is approximately 10 Hz.

![Angle and Velocity Display Using Tera Term](image)

**Figure 43. Angle and Velocity Display Using Tera Term**
6.1.4 Software Packages Used

There are several software packages recommended for the TIDA-00796. The following list shows packages and their versions used while developing the TIDA-00796:

- CCS (6.1.1.00022) is an integrated development environment for TI microcontrollers. This package is needed to change the source code.
- C2000 Compiler (TI v6.4.9) is TI’s proprietary C2000 C compiler. This package comes with Code Composer Studio.
- controlSUITE™ provides information, libraries examples for C2000 microcontrollers, and circuit diagrams for development tools. This package is needed when I2 math library is used.
- CCS UniFlash is a free standalone tool used to program on-chip flash memory on TI MCUs and on-board flash memory for Sitara processors. Use this tool if you want to run standalone application only.
- Tera Term is an open source serial port terminal that supports VT100. This tool is recommended to interface with the PC.

6.2 TIDA-00363 Firmware Description

See the TIDA-00363 project folder and documentation to use it with the reference design (http://www.ti.com/tool/TIDA-00363).
7 Test Setup and Reference Design Evaluation

Exposed copper on the QGND signal can be effectively used for oscilloscope measurements as shown in Figure 44. Eliminating the long ground lead connection from a typical oscilloscope probe reduces noise pickup.

![Figure 44. Probing the AFE Using an Oscilloscope Probe](image)

A vast majority of oscilloscopes share ground connection with all channels and power network grounding. Ignoring the proper measurement technique can short circuit the PGA411-Q1 and damage the chip.

The best solution to avoid the grounding problem is to use low-voltage differential oscilloscope probes. These probes allow simultaneous measurements at the exciter output and sin / cos inputs. DC bias resistors on the AFE inputs avoid exceeding maximal common-mode voltage for the probes.

An alternate method is using a four-channel oscilloscope referenced to QGND and math subtraction for the channels. Differential voltage is then automatically calculated. The resolution is usually satisfactory for such device. However, only two differential channels can be displayed at the same time.

Also use the benefit of a USB powered design and perform all measurements from a laptop running from battery to avoid any grounding loops.

Two different test setups are used to evaluate the accuracy of the TIDA-00796:

- Test Setup A: with an optical encoder and Tyco Resolver
- Test Setup B: with the TIDA-00176 and a sin/cos encoder for a reference and LTN R58 resolver

**NOTE:** It is important to have the reference angular sensor and the resolver concentric. Any deviation is transferred in the sinusoidal-shape error in the static accuracy plot.
7.1 Test Setup A

Figure 45 shows the first test bench used for static accuracy measurements. The 19b optical encoder COH58S-00021 with a significantly higher resolution and accuracy is a reference angular sensor. The stepper motor is used for automated testing. Table 16 shows selected parameters of the resolver used in test setup A.

Table 16. TYCO V23401-D1001-B102 Resolver Specification

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SPECIFICATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>p</td>
<td>Pairs of poles (speed)</td>
</tr>
<tr>
<td>p = 1</td>
<td></td>
</tr>
<tr>
<td>$V_{\text{RESIDUAL}}$</td>
<td>Residual voltage</td>
</tr>
<tr>
<td>25 mV at $V_{\text{EXC}} = 7$ V</td>
<td></td>
</tr>
<tr>
<td>$\Delta \phi$</td>
<td>Angle error spread</td>
</tr>
<tr>
<td>± 7°</td>
<td></td>
</tr>
<tr>
<td>$R_{\text{R1-R2}}$</td>
<td>Input DC resistance</td>
</tr>
<tr>
<td>46 $\Omega$ at 22°C</td>
<td></td>
</tr>
<tr>
<td>$R_{\text{S1-S3}}$</td>
<td>Output DC resistance</td>
</tr>
<tr>
<td>63 $\Omega$ at 22°C</td>
<td></td>
</tr>
<tr>
<td>$Z_{\text{RO}}$</td>
<td>Input impedance magnitude (open outputs)</td>
</tr>
<tr>
<td>300 $\Omega$ at 10 kHz</td>
<td></td>
</tr>
<tr>
<td>$Z_{\text{RS}}$</td>
<td>Input impedance magnitude (short circuit outputs)</td>
</tr>
<tr>
<td>220 $\Omega$ at 10 kHz</td>
<td></td>
</tr>
<tr>
<td>$Z_{\text{SO}}$</td>
<td>Output impedance magnitude (open input)</td>
</tr>
<tr>
<td>210 $\Omega$ at 10 kHz</td>
<td></td>
</tr>
<tr>
<td>$Z_{\text{SS}}$</td>
<td>Output impedance magnitude (short circuit input)</td>
</tr>
<tr>
<td>300 $\Omega$ at 10 kHz</td>
<td></td>
</tr>
<tr>
<td>$L_{\text{R1-R2}}$</td>
<td>Input inductance (open outputs)</td>
</tr>
<tr>
<td>4.4 mH</td>
<td></td>
</tr>
<tr>
<td>$\psi$</td>
<td>Phase shift</td>
</tr>
<tr>
<td>typ. 3° at 10 kHz</td>
<td></td>
</tr>
<tr>
<td>$r_T$</td>
<td>Transformation ratio</td>
</tr>
<tr>
<td>0.5 ± 10% within 4 to 20 kHz</td>
<td></td>
</tr>
<tr>
<td>0.5 ± 5% at 5 kHz</td>
<td></td>
</tr>
<tr>
<td>$L_{\text{S1-S3}}$</td>
<td>Output inductance (R1-R2 short circuit)</td>
</tr>
<tr>
<td>4.1 mH</td>
<td></td>
</tr>
<tr>
<td>$V_{\text{EXC}}$</td>
<td>Excitation voltage</td>
</tr>
<tr>
<td>2 to 10 $V_{\text{RMS}}$</td>
<td></td>
</tr>
<tr>
<td>$f$</td>
<td>Excitation frequency</td>
</tr>
<tr>
<td>4 to 20 kHz</td>
<td></td>
</tr>
</tbody>
</table>

Figure 45. Test Bench With Optical Encoder to Measure Absolute Accuracy
7.2 Test Setup B

Figure 46 shows an alternate test bench using the standard industrial resolver LTN R58. A list of selected parameters for the 10-kHz excitation frequency for the resolver is in Table 17.

The ROD 480 1024 Sin/Cos angular sensor with another TI reference design TIDA-00176 (http://www.ti.com/tool/tida-00176) is used as the reference.

Table 17. R58CURE151B04-021-07AX Resolver Specification

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SPECIFICATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>p</td>
<td>Pairs of poles (speed)</td>
</tr>
<tr>
<td>( V_{\text{RESIDUAL}} )</td>
<td>Residual voltage</td>
</tr>
<tr>
<td>( \Delta \phi )</td>
<td>Angle error spread</td>
</tr>
<tr>
<td>( R_{\text{R1-R2}} )</td>
<td>Input DC resistance</td>
</tr>
<tr>
<td>( R_{\text{S1-S3}} )</td>
<td>Output DC resistance</td>
</tr>
<tr>
<td>( Z_{\text{RO}} )</td>
<td>Input impedance (open outputs)</td>
</tr>
<tr>
<td>( Z_{\text{RS}} )</td>
<td>Input impedance (short circuit outputs)</td>
</tr>
<tr>
<td>( Z_{\text{SO}} )</td>
<td>Output impedance (open input)</td>
</tr>
<tr>
<td>( Z_{\text{SS}} )</td>
<td>Output impedance (short circuit input)</td>
</tr>
<tr>
<td>( \psi )</td>
<td>Phase shift</td>
</tr>
<tr>
<td>( r_{T} )</td>
<td>Transformation ratio</td>
</tr>
<tr>
<td>( V_{\text{EXC}} )</td>
<td>Excitation voltage</td>
</tr>
<tr>
<td>( f )</td>
<td>Excitation frequency</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>max. 30 mV</th>
</tr>
</thead>
<tbody>
<tr>
<td>( p )</td>
<td>( 1 )</td>
</tr>
<tr>
<td>( \Delta \phi )</td>
<td>( \pm 10^\circ )</td>
</tr>
<tr>
<td>( R_{\text{R1-R2}} )</td>
<td>( 40 \Omega \pm 10 % ) at 20°C</td>
</tr>
<tr>
<td>( R_{\text{S1-S3}} )</td>
<td>( 102 \Omega \pm 10 % ) at 20°C</td>
</tr>
<tr>
<td>( Z_{\text{RO}} )</td>
<td>( 110 \Omega + j 159 \Omega )</td>
</tr>
<tr>
<td>( Z_{\text{RS}} )</td>
<td>( 96 \Omega + j 150 \Omega )</td>
</tr>
<tr>
<td>( Z_{\text{SO}} )</td>
<td>( 245 \Omega + j 400 \Omega )</td>
</tr>
<tr>
<td>( Z_{\text{SS}} )</td>
<td>( 216 \Omega + j 370 \Omega )</td>
</tr>
<tr>
<td>( \psi )</td>
<td>( -6^\circ \pm 3^\circ )</td>
</tr>
<tr>
<td>( r_{T} )</td>
<td>( 0.5 \pm 10% )</td>
</tr>
<tr>
<td>( V_{\text{EXC}} )</td>
<td>( 7 , \text{V}_{\text{RMS}} )</td>
</tr>
<tr>
<td>( f )</td>
<td>specified at 5, 7, and 10 kHz</td>
</tr>
</tbody>
</table>

Figure 46. Test Bench with Sin/Cos Sensor to Measure Absolute Accuracy
8 Test Data

This section summarizes measurement data for the TIDA-00796. Table 18 shows the default configuration of the PGA411-Q1. The exciter default frequency is 10 kHz and the excitation voltage is $4 \, \text{V}_{\text{RMS}}$.

**NOTE:** The default configuration of the PGA411-Q1 is subject to change. See the latest datasheet revision for the most current data (SLASE76).

**Table 18. Default PGA411-Q1 Configuration Used for TIDA-00796**

<table>
<thead>
<tr>
<th>REGISTER</th>
<th>VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>DEV_OVUV1</td>
<td>0x8FC0</td>
</tr>
<tr>
<td>DEV_OVUV2</td>
<td>0x00C0</td>
</tr>
<tr>
<td>DEV_OVUV3</td>
<td>0xFCFF</td>
</tr>
<tr>
<td>DEV_OVUV4</td>
<td>0x07F2</td>
</tr>
<tr>
<td>DEV_OVUV5</td>
<td>0x1C00</td>
</tr>
<tr>
<td>DEV_OVUV6</td>
<td>0x038F</td>
</tr>
<tr>
<td>DEV_TLOOP_CFG</td>
<td>0x0517</td>
</tr>
<tr>
<td>DEV_AFE_CFG</td>
<td>0x0005</td>
</tr>
<tr>
<td>DEV_PHASE_CFG</td>
<td>0x1400</td>
</tr>
<tr>
<td>DEV_CONFIG1</td>
<td>0x0002</td>
</tr>
<tr>
<td>DEV_CONTROL1</td>
<td>0x0000</td>
</tr>
<tr>
<td>DEV_CONTROL2</td>
<td>0x0000</td>
</tr>
<tr>
<td>DEV_CONTROL3</td>
<td>0x0003</td>
</tr>
<tr>
<td>DEV_STAT1</td>
<td>0x0000</td>
</tr>
<tr>
<td>DEV_STAT2</td>
<td>0x0000</td>
</tr>
<tr>
<td>DEV_STAT3</td>
<td>0x0000</td>
</tr>
<tr>
<td>DEV_STAT4</td>
<td>0x0006</td>
</tr>
<tr>
<td>DEV_STAT5</td>
<td>0x0275</td>
</tr>
<tr>
<td>DEV_STAT6</td>
<td>0x3FFF</td>
</tr>
<tr>
<td>DEV_STAT7</td>
<td>0x004A</td>
</tr>
<tr>
<td>DEV_CLCRC</td>
<td>0x0003</td>
</tr>
<tr>
<td>DEV_CRC</td>
<td>0x0000</td>
</tr>
<tr>
<td>CRCCALC</td>
<td>0x00FF</td>
</tr>
<tr>
<td>DEV_EE_CTRL1</td>
<td>0x0000</td>
</tr>
<tr>
<td>DEV_CRC_CTRL1</td>
<td>0x0000</td>
</tr>
<tr>
<td>DEV_EE_CTRL4</td>
<td>0x0000</td>
</tr>
<tr>
<td>DEV_UNLK_CTRL1</td>
<td>0x00F0</td>
</tr>
</tbody>
</table>

**NOTE:** Table 18 corresponds to the register dump of the PGA411-Q1, including read only registers.
8.1 PGA411-Q1 Boost Converter

8.1.1 Switching Node Waveforms

Figure 47 and Figure 48 show voltage waveforms at the switching node of the integrated boost converter. Ringing during the turn-off phase in discontinuous conduction mode (DCM), when current through the inductor drops to zero, is normal. The ringing is caused by a tank circuit formed by the inductor L2 and parasitic capacitance of the switching node.

Figure 47. Boost Converter Switching Node Waveform (DCM)

Figure 48. Boost Converter Switching Node Waveform (CCM)

The transition point from DCM to CCM is approximately at $I_{\text{OUT}} = 30$ mA load current, $V_{\text{CCSW}} = 5$-V input voltage, and 12-V output voltage.
8.1.2 Boost Converter Efficiency

*Figure 49* shows the measured step-up converter efficiency.

![Step-up Converter Efficiency](image)

**Figure 49. Step-up Converter Efficiency**

8.1.3 Exciter Amplifier

*Figure 50* shows exciter amplifier output OE1, OE2 waveforms with reference to QGND. The default configuration with 4 V\textsubscript{RMS} and 10-kHz excitation signal is used.

![OE1 and OE2 Signals](image)

**Figure 50. OE1 and OE2 Signals for Default Settings**
8.1.4 Exciter Feedback

Figure 51 shows IE1 and IE2 waveforms with respect to the ground in 4-V<sub>RMS</sub> mode and 10-kHz excitation signal. Note that input voltage on the IE1 and IE2 pins must be within 0.5 to 4.5 V.

![Figure 51. IE1 and IE2 Signals for Default Setting](image)

8.2 AFE

Figure 52 shows input voltages on IZ1 (orange) and IZ3 (teal) pins taken at the angle corresponding to the maximal amplitude. The red trace is a calculated differential signal corresponding to the resolver output.

![Figure 52. IE1 and IE3 Signals for Default Configuration](image)

NOTE: Different IZ1 and IZ2 signal amplitudes are explained in Section 4.3.1.
8.3 Absolute Static Accuracy

8.3.1 Static Accuracy Comparison for Test Setsups A and B

Figure 53 shows performance comparison of Test Setups A and B. Both plots are taken using the same configuration, thus LTN R58 resolver excitation voltage is below the specification. As shown in Figure 53, there is not any significant difference in performance between the setups. Shielded construction of the LTN R58 seems to have slightly better noise immunity.

![Figure 53. Test Setup A and B Performance Comparison (Default Configuration)](image)

8.3.2 Static Accuracy versus Excitation Voltage

Figure 54 shows the influence of the exciter signal voltage on overall static accuracy for the TIDA-00796 in Test Setup A.

![Figure 54. TIDA-00796 Static Accuracy for Different Excitation Voltages in Test Setup A](image)
8.3.3 Static Accuracy versus Excitation Frequency

Figure 55 shows the relationship between overall static accuracy and exciter signal frequency in Test Setup A.

![Graph showing static accuracy versus excitation frequency](image)

Figure 55. TIDA-00796 Static Accuracy for Different Excitation Frequencies in Test Setup A

8.3.4 Static Accuracy versus AFE Component Tolerance

Figure 56 shows the result of an experiment where all 1% tolerance resistors in the TIDA-00796 the AFE are replaced by 0.1% tolerance ones. Effect of the change is negligible.

![Graph showing passive components tolerance analysis](image)

Figure 56. TIDA-00796 Passive Components Tolerance Analysis
8.4 Radio Emissions Approximation

8.4.1 Test Setup

Figure 57 shows the test setup for EMC measurements using EMSCAN tool (http://www.emscan.com/). The highlighted part on the figure is being investigated. The TIDA-00796 reference design is connected to the controlSTICK and then to the laptop running from a battery. All measurement results are coming from a standard laboratory environment without any RF shielding.

Note that the board is upside down, so the PGA411-Q1 circuitry is as close to the measurement pad as possible.

![Figure 57. Test Setup for EMSCAN Measurements](image)

Three different measurement sets are taken:
1. Range from 150 kHz to 30 MHz
2. Range from 30 MHz to 200 MHz
3. Range from 200 MHz to 1 GHz

Every measurement set contains a background scan (when the TIDA-00796 is powered off), and the final board scan is when the TIDA-00796 is fully operational.

**NOTE:** EMSCAN results are for information only.
8.4.2 150-kHz to 30-MHz Range

Figure 58 shows a radiation heat map for the 150-kHz to 30-MHz frequency range. As expected, the boost converter has the highest radiated emissions intensity.
Figure 59 shows a background scan. However, the configuration of the measurement setup is different. The Y-axis scale does not correspond to the final scan.

Figure 59. Background Spectrum Scan for 150-kHz to 30-MHz Range
Figure 60 shows the final scan for the 150-kHz to 30-MHz range. Note the boost converter spread spectrum modulation.

Figure 60. Radiation Spectrum for 150-kHz to 30-MHz Range
8.4.3 30 to 200-MHz Range

Figure 61. Background Spectrum Scan for 30- to 200-MHz Range
Figure 62. Radiation Spectrum for 30- to 200-MHz Range
8.4.4 200-MHz to 1-GHz Range

Figure 63. Background Spectrum Scan for 200-MHz to 1-GHz Range
Figure 64. Radiation Spectrum for 200-MHz to 1-GHz Range
8.5 **Thermal Image**

A picture from a thermal imaging camera is shown in Figure 65. For better visualization, the mechanical overlay has been added during picture post processing. The USB-powered TIDA-00796 reference design runs on default configuration (4 V_{RMS}, 10-kHz excitation signal) with the boost converter enabled. Velocity and angular data are being transferred to the PC using the JTAG transport layer at the maximum speed.

Figure 65 also shows the effect of the analog and digital plane separation. Heat from the PGA411-Q1 distributed through thermal pads spread over the digital plane only while the analog plane remains significantly cooler. Note that in this particular example, the USB bridge FT2232D and C2000 controller on the controlSTICK are warmer than the PGA411-Q1 with the integrated DC-DC boost converter.

![Figure 65. Thermal Image of TIDA-00796 During Operation (USB Powered)](image-url)
9 Design Files

9.1 Schematics
To download the schematics, see the design files at TIDA-00796.

9.2 Bill of Materials
To download the bill of materials (BOM), see the design files at TIDA-00796.

9.3 PCB Layout Recommendations
Follow the PCB layout recommendations found in the detailed application report “PGA411-Q1 PCB Design Guidelines” (SLAA697).

9.3.1 Layout Prints
To download the layer plots, see the design files at TIDA-00796.

9.4 Altium Project
To download the Altium project files, see the design files at TIDA-00796.

9.5 Gerber Files
To download the Gerber files, see the design files at TIDA-00796.

9.6 Assembly Drawings
To download the assembly drawings, see the design files at TIDA-00796.

9.7 Software Files
To download the software files, see the design files at TIDA-00796.

10 References
1. Texas Instruments, PGA411-Q1 Resolver Sensor Interface, PGA411-Q1 Datasheet (SLASE76)
2. Texas Instruments, PGA411-Q1 PCB Design Guidelines, PGA411-Q1 Application Report (SLAA697)
3. Texas Instruments, PGA411-Q1 Step-by-Step Initialization With Any Host System, PGA411-Q1 Application Report (SLAA688)
4. Texas Instruments, Interface to Sin/Cos Encoders With High-Resolution Position Interpolation, TIDA-00176 Design Guide (TIDUA05)


11 Terminology

AEC—Automotive Electronics Council
BOM—Bill of Material
CAN—Controller Area Network
CCM—Constant Conduction Mode
CCS—Code Composer Studio
CDM—Charge Device Model
DCM—Discontinuous Conduction Mode
ECU—Electronic Control Unit
EMC—Electromagnetic Compatibility
ESD—Electrostatic Discharge
EV—Electric Vehicle
EVM—Evaluation Module
FPGA—Field Programmable Gate Array
GPIO—General Purpose Input Output
HBM—Human Body Model
HEV—Hybrid Electric Vehicle
IGBT—Insulated Gate Bipolar Transistor
ISO—International Organization for Standardization
PCB—Printed Circuit Board
PSSR—Power Supply Rejection Ratio
PWM—Pulse Width Modulation
RDC—Resolver-to-Digital Converter
RF—Radio Frequency
SBC—System Basis Chip
SoC—System on Chip
SPI—Serial Peripheral Interface
TIDA—Texas Instruments Reference Design
USB—Universal Serial Bus

12 About the Author

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Revision A History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (April 2016) to A Revision

• Changed from preview page........................................................................................................ 1
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