TI Designs

100-V to 450-V DC, 5-W, 80% Efficiency at 1 W, Auxiliary Supply Reference Design for AC-DC Power Converters

TI Designs

The TIDA-00708 is a 5-W, multiple output, auxiliary power supply designed for use in power converters targeted for applications in industrial, server, telecom, and consumer systems. This reference design is a flyback converter implemented using the UCC28881, which integrates the controller, a 700-V power MOSFET, and internal current sense into one monolithic device. The design is simple, compact, and affordable due to a minimal component count with all the necessary protections such as output overcurrent, output short circuit, and over-temperature conditions built in. Hardware is designed and tested to pass EFT requirements and meets the low-power efficiency performance of Department of Energy (DoE) Level VI.

Design Features

- Designed for Wide Operating Input Voltage Range From 100-V to 450-V DC
- Very Low Standby Power of < 50 mW
- High Efficiency > 82% at 165-V DC and > 84% at 400-V DC for Loads > 75%
- Efficiency of ~80% at 20% Load (1 W)
- Multiple Outputs: 12 V/0.20 A, 3.3 V/0.25 A, 12 V/0.15 A (Isolated)
- Robust Supply Protected for Output Short Circuit, Overload, and Undervoltage Lockout
- Ultra-Simple Circuit With Low-Cost Shelf Components
- Compact Form Factor (32 mm × 25 mm) and Simple Plug-in Card

Featured Applications

- AC-DC Power Supplies
- Server, Telecom, and Industrial Power Converters
- Battery Chargers
- Bias Power for MCU, RF, and IoT Enabled Devices
- Aux Power for Inverter-fed Motor Drives

Design Resources

- TIDA-00708 Design Folder
- UCC28881 Product Folder
- TLV70233 Product Folder

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## 1 Key System Specifications

### Table 1. Key System Specifications

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<td></td>
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<td>W</td>
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<td>Brownout voltage ($V_{\text{IN_UVLO}}$)</td>
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<tr>
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<td>0.25</td>
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<td>A</td>
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<td>11.4</td>
<td>12</td>
<td>13.2</td>
<td>V</td>
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<td>Output current 3</td>
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<td></td>
<td>0.15</td>
<td></td>
<td>A</td>
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<td>Line regulation</td>
<td>At full load</td>
<td>12-V output</td>
<td>–0.2</td>
<td>0.2</td>
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<td>4-V output (without LDO)</td>
<td>–0.5</td>
<td>0.5</td>
<td>%</td>
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<td>12-V_ISO output</td>
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<td>4-V output (without LDO)</td>
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<td>%</td>
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<td></td>
<td></td>
<td>12-V_ISO output</td>
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<td>2</td>
<td></td>
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<td>Output voltage ripple</td>
<td>At full load</td>
<td>12-V output</td>
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<td></td>
<td></td>
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<td>6</td>
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<td>Primary-to-secondary insulation system characteristics</td>
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<td>Efficiency ($\eta$)</td>
<td>$V_{\text{IN}} = V_{\text{NOM}}$, $I_{\text{OUT}} = 20%, 40%, 60%, 80%, \text{and } 100% \text{ full load}$</td>
<td>79</td>
<td></td>
<td>86</td>
<td>%</td>
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<td>Protections</td>
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<td>Undervoltage lockout</td>
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<tr>
<td>Operating ambient</td>
<td>Open frame</td>
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<td>25</td>
<td>60</td>
<td>°C</td>
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<td>EFT</td>
<td>As per IEC 61000-4-4</td>
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<tr>
<td>Dimensions</td>
<td>Length × Breadth × Height</td>
<td>32 × 25 × 16</td>
<td></td>
<td></td>
<td>mm</td>
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</table>
## System Description

High-power converters used in server, telecom, and industrial systems need auxiliary power supplies to support the housekeeping needs of the power supply unit (PSU). An auxiliary power supply is commonly used to power the internal control and sensing electronics for voltage and current feedback of the PSU. It is an isolated DC-DC converter generating multiple isolated outputs to power primary and secondary-side control devices. The typical usage of an auxiliary power supply is shown in Figure 1.

Auxiliary power supplies are independent isolated DC-DC converters as power converters have an EMI filter, diode-bridge rectifier, and bulk capacitor present in the system, generating a rectified DC bus. These operate over a wide input range from 100-V to 450-VDC and keep system electronics powered under all conditions to detect faults such as undervoltage, overvoltage, and overcurrent. Typically, auxiliary power supplies generate three or more outputs, delivering a power of 3 to 5 W.

These supplies need to have very low standby power to meet the stringent norms of, for example, the DoE and Code of Conduct (CoC). In addition, these supplies need to have a high efficiency from 10% to 100% loads to ensure low system power loss under all operating conditions.

![Figure 1. Typical System Block Diagram of High-Power Converter](image-url)

This reference design is a 5-W auxiliary power supply, designed specifically to meet very low standby power needs of < 100 mW and high efficiency of > 80% for a wide load range from 20% to 100% and over the entire input operating voltage range. This reference design is a simple, low-component, low-cost flyback converter implemented using the UCC28881, which integrates the controller, the 700-V power MOSFET, and internal current sense into one monolithic device. The design operates over a wide input range of 100-V to 450-V DC, delivering total power of 5 W from three outputs (12 V, 3.3 V, and isolated 12 V).

The design meets the key challenges of the appliance auxiliary power supply to provide safe and reliable power while delivering a high performance with low power consumption and low bill-of-material (BOM) cost.
3 Block Diagram

![Block Diagram of 5-W, Multiple Output Auxiliary Power Supply](image)

3.1 Highlighted Products and Key Advantages

The following highlighted products are used in this reference design. This section presents the key features for selecting the devices for this reference design. Find complete details of the highlighted devices in their respective product datasheets.

3.1.1 UCC28881 700-V, 225-mA Low Quiescent Current Offline Converter

To implement the high performance, small form factor flyback design of 5-W power, the UCC28881 is the preferred controller as it has a built-in HV-startup FET, 700-V power FET, and primary current sensing, which aids in a reduced component count design. In addition, the low quiescent power consumption and robust protection for faults make it a right fit for this TI Design.

The UCC28881 integrates the controller and a 700-V power MOSFET into one monolithic device. The device also integrates a high-voltage current source, enabling start up and operation directly from the rectified mains voltage. The low quiescent current ($I_Q$) of the device enables excellent efficiency. The UCC28881 incorporates a soft-start feature for controlled startup of the power stage, which minimizes the stress on the power-stage components. The UCC28880 is low-current version of the UCC28881.

The key features that make this device unique are:
- Integrated 700-V MOSFET and startup current source in SOIC-7 package
- Internal current sense, thus reducing total BOM cost
- Lower $I_Q$ (< 100 µA)
- Self-biased switcher, thus no aux winding required on inductor or transformer to bias the controller
- Low short circuit and inductor current run away protection
- Protection features such as current limiter, overload and output short circuit, and undervoltage lockout
3.1.2 TLV702 300-mA, Low-I_{\text{Q}}, Low-Dropout Regulator

The TLV702 series of low-dropout (LDO) linear regulators are low I_{\text{Q}} devices with excellent line and load transient performance. A precision bandgap and error amplifier provides an overall 2% accuracy. Low output noise, very high power supply rejection ratio (PSRR), and low-dropout voltage make this series of devices ideal for a wide selection of battery-operated handheld equipment. All versions of the device have thermal shutdown and current limit for safety. These devices are stable with an effective output capacitance of only 0.1 \mu F. This enables the use of cost-effective capacitors that have higher bias voltages and temperature derating. The devices regulate to specified accuracy with no output load. This series also provides an active pulldown circuit to quickly discharge the outputs.

The key features that make this device unique are:

- I_{\text{OUT}}: 300 mA
- Low-power I_{\text{Q}}: 31 \mu A
- V_{\text{OUT}}: 2% accurate
- Low output noise: 48 mV_{\text{RMS}} (no bypass capacitor required)
- High PSRR: 68 dB at 1 kHz
4 System Design Theory

This reference design is a multiple isolated output 5-W auxiliary power supply, operating over a wide DC input range from 100-V to 450-V DC. The design has a flyback power stage implemented using the UCC28881 with a 700-V integrated FET offline converter to deliver three different outputs: 12 V/0.2 A, 3.3 V/0.25 A regulated with post LDO (4-V unregulated output), and an isolated 12 V/0.15 A. The overall system efficiency is over 80% with a 165-V DC input and over 84% with a 325-V DC input under full load conditions. The design has protection built-in for output overload, output short circuit, and undervoltage lockout.

In addition, the design manifests a very low standby power and high efficiency even at light load conditions. The design is tested and validated for all voltage and load conditions and tested for EFT as per IEC 61000-4-4 norms.

4.1 Flyback Circuit Component Design

The section details the design process and component selection a designer must follow to complete a flyback converter using the UCC28881.

4.1.1 Design Goal Parameters

Table 2 states the design goal parameters for this design. These parameters are used in further calculations to select components.

<table>
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<th>Table 2. Design Goal Parameters</th>
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<tr>
<td>F&lt;sub&gt;MAX&lt;/sub&gt;</td>
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<tr>
<td>η</td>
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4.1.2 Transformer Parameter Calculations: Turns Ratio, Primary Inductance, and Peak Primary Current

First determine the turns ratio of the transformer, limiting the voltage and current stress across the switching devices. The UCC28881 has a 700-V integrated FET, and to operate input voltages up to 450-V DC, the flyback reflected voltage \( V_R \) and the maximum \( V_{DS} \) MOSFET voltage stress are decided accordingly.

\( V_R \) is the voltage across the primary winding when the switch Q1 is turned off. This also affects the maximum \( V_{DS} \) rating of Q1. The maximum drain-to-source voltage is given by Equation 1.

\[
V_{DS(max)} = V_{DC_IN(max)} + V_R + V_{CLAMP}
\]  

(1)

where:

- \( V_{CLAMP} \) is the voltage spike caused by the leakage inductance of the transformer and clamped by the snubber
- \( V_R \) is the reflected voltage across transformer primary
- \( V_{DC_IN(max)} \) is the maximum DC input voltage (450 V)

Assuming a spike of 20\% of \( V_{DS(max)} \) over a reflected voltage, \( V_{CLAMP} \) is calculated to be about 90 V. With a safety margin of around 5\%, \( V_R \) is calculated as:

\[
660 \text{ V} = 450 + V_R + 90
\]

\( V_R = 120 \text{ V} \)

Choosing the \( V_R \) is a compromise between the primary MOSFET and the secondary rectifier voltage stress. Setting it too high, by means of a higher turns ratio, would mean a higher \( V_{DS(max)} \) but lower voltage stress on the secondary diode. Setting it too low, by means of a lower turns ratio, would lower \( V_{DS(max)} \) but increase the secondary diode stress. A good starting point is to limit \( V_R \leq 100 \text{ V} \) for this wide range of input voltage.

With the highest output voltage being 12 V, the minimum turns ratio required is determined by Equation 2.

\[
N_{PS} = \frac{V_R}{(V_{OUT1} + V_{DIODE})}
\]  

(2)

where:

- \( N_{PS} \) is the turns ratio of transformer for a 12-V output
- \( V_{OUT1} \) is the 12-V output
- \( V_{DIODE} \) is the drop across the secondary rectifier diode, assuming 0.7 V

\[
N_{PS1} = \frac{100 \text{ V}}{(12 \text{ V} + 0.7 \text{ V})} = 7.87
\]

The actual value of the turns ratio is chosen as 8 for further calculations. Similarly, the turns ratio for other output rails are also calculated using Equation 2 with the same value of \( V_R \) where \( V_{OUT2} \) is 4 V and \( V_{OUT3} \) is 12 V (isolated):

\[
N_{PS2} = \frac{100 \text{ V}}{(4 \text{ V} + 0.7 \text{ V})} = 21.3
\]

\[
N_{PS3} = \frac{100 \text{ V}}{(12 \text{ V}_\text{ISO} + 0.7 \text{ V})} = 7.87
\]

Round the turns ratio off to the next higher integer. The actual values of the turns ratios are chosen as 22 and 8 for 4-V and isolated 12-V outputs, respectively.
The maximum duty cycle ($D_{\text{MAX}}$) is also based on $V_r$ and the minimum DC input ($V_{\text{DC\_MIN}}$). The maximum duty cycle appears during $V_{\text{DC\_MIN}}$. At this condition, the transformer is designed to operate at the boundary of the DCM and CCM. The maximum duty cycle is given by Equation 3.

$$D_{\text{MAX}} = \frac{V_r}{V_r + V_{\text{DC\_MIN}}} \quad (3)$$

$$D_{\text{MAX}} = \frac{100 \text{ V}}{100 \text{ V} + 100 \text{ V}} = 0.5$$

The UCC28881 has a maximum duty cycle limit ranging between 0.45 and 0.55. Therefore, the calculations are done considering a maximum duty cycle operation of 0.43.

For power output of 5 W and desired efficiency of 82%, input power is

$$P_{\text{OUT}} = \frac{P_{\text{IN}}}{\eta} = \frac{5 \text{ W}}{0.82} = 6.1 \text{ W} \quad (4)$$

$I_{\text{AVG}}$ is the average input current to the system given by Equation 5.

$$I_{\text{AVG}} = \frac{P_{\text{OUT}}}{\eta \times V_{\text{DC\_MIN}}} \quad (5)$$

$$I_{\text{AVG}} = \frac{5}{0.82 \times 100} = 0.061 \text{ A}$$

The primary peak current ($I_{\text{PEAK}}$) of the transformer is then calculated with Equation 6.

$$I_{\text{PEAK}} = \frac{2 \times I_{\text{AVG}}}{D_{\text{MAX}}} \quad (6)$$

$$I_{\text{PEAK}} = \frac{2 \times 0.061}{0.43} = 0.284 \text{ A}$$

The maximum switching frequency ($F_{\text{MAX}}$) of the controller is 62 kHz and the unit is designed to operate at this maximum frequency. Considering $F_{\text{MAX}}$, the primary inductance of transformer is calculated using Equation 7.

$$L_{\text{PRI}} = \frac{V_{\text{DC\_MIN}} \times D_{\text{MAX}}}{I_{\text{PEAK}} \times f} \quad (7)$$

$$L_{\text{PRI}} = \frac{100 \text{ V} \times 0.43}{0.284 \text{ A} \times 62 \text{ kHz}} = 2.442 \text{ mH}$$

The transformer is designed with a primary inductance of 2.5 mH.
4.1.3 Transformer Parameter Calculations: Primary and Secondary RMS Currents

The transformer primary RMS current \( I_{PRMS} \) is calculated using Equation 8.

\[
I_{PRMS} = I_{PEAK} \times \sqrt{\frac{D_{MAX}}{3}}
\]

Equation 8

\[
I_{PRMS} = 0.284 \text{ A} \times \sqrt{\frac{0.43}{3}} = 0.108 \text{ A}
\]

The secondary peak current and RMS current for each of the three outputs need to be calculated separately as follows:

The transformer secondary peak current for the 12-V output \( I_{SPK1} \) can be calculated using Equation 9.

\[
I_{SPK1} = \frac{2 \times I_{OUT1}}{1 - D_{MAX}}
\]

Equation 9

\[
I_{SPK1} = \frac{2 \times 0.2}{1 - 0.43} = 0.7 \text{ A}
\]

Equation 10 calculates the value of the secondary RMS current for the 12-V rail:

\[
I_{RMS1} = I_{SPK1} \times \sqrt{\frac{1 - D_{MAX}}{3}}
\]

Equation 10

\[
I_{RMS1} = 0.7 \text{ A} \times \sqrt{\frac{1 - 0.43}{3}} = 0.305
\]

Similarly, the secondary peak current and RMS current for the 4-V rail and 12-V isolated rail can be calculated using Equation 9 and Equation 10 by substituting \( I_{OUT1} \) with \( I_{OUT2} \) and \( I_{OUT3} \) with values of 0.25 A and 0.15 A, respectively:

\[
I_{SPK2} = \frac{2 \times 0.25}{1 - 0.43} = 0.877 \text{ A}
\]

\[
I_{RMS2} = 0.877 \text{ A} \times \sqrt{\frac{1 - 0.43}{3}} = 0.382 \text{ A}
\]

\[
I_{SPK3} = \frac{2 \times 0.15}{1 - 0.43} = 0.526 \text{ A}
\]

\[
I_{RMS3} = 0.526 \text{ A} \times \sqrt{\frac{1 - 0.43}{3}} = 0.23 \text{ A}
\]

4.1.4 Feedback Component Selection

The feedback threshold for the UCC28881 is 1.03 V (SLUSC36). This design uses the 12-V rail as the reference for feedback voltage. Thus, the value for feedback resistors can be calculated using Equation 11.

\[
1.03 \text{ V} = \frac{R_{PULL\_DN} \times 12.7}{R_{PULL\_DN} + R_{PULL\_UP}}
\]

Equation 11

\[
\frac{R_{PULL\_DN}}{R_{PULL\_UP}} = 11.3
\]

To limit the feedback current through \( R_{PULL\_UP} \), select a value greater than 100k. The value chosen for \( R_{PULL\_UP} \) is 110 kΩ. With this value of \( R_{PULL\_UP} \), the calculated value of \( R_{PULL\_DN} \) is 9.73 kΩ. The final selected value for \( R_{PULL\_DN} \) is 10 kΩ.
4.1.5 **VDD Supply and Biasing Capacitor**

The supply for operation of the UCC28881 is generated internally and there is no need for an external voltage source (for example, the auxiliary winding of a flyback converter). Use a capacitance of 100 nF on the VDD pin to ensure a high-phase margin of the internal 5-V regulator; place this capacitor close to the VDD pin and GND pins to minimize the series resistance and inductance.

4.1.6 **Rectifying Diode Selection**

Calculate the secondary output diode reverse voltage or blocking voltage needed \( (V_{\text{DIODE\_BLOCKING}}) \) using Equation 12.

\[
V_{\text{DIODE\_BLOCKING}} = \frac{V_{\text{IN\_MAX}}}{N_{PS}} + V_{\text{OUT}} + V_{\text{DIODE}}
\]  

(12)

For 12-V and 12-V ISO output rails, the blocking voltage for diode is calculated as:

\[
V_{\text{DIODE\_BLOCKING}} = \frac{450 \, V}{8} + 12 \, V + 0.7 \, V = 68.95 \, V
\]

Thus, a 100-V diode is recommended to rectify the 12-V and 12-V ISO rails. For a 4-V output, the blocking voltage for diode is calculated as:

\[
V_{\text{DIODE\_BLOCKING}} = \frac{450 \, V}{22} + 4 \, V + 0.7 \, V = 25.15 \, V
\]

Thus, a 50-V diode can be used. For this design, a 100-V, 2-A diode is used for all three rails (part number: PMEG10020AELRX). A high-current part is used to reduce the voltage drop across the diode.

4.1.7 **Select Output Capacitors**

For this design, the output capacitor \( (C_{\text{OUT}}) \) was selected to have a maximum output voltage ripple of 250 mV with an operating frequency of 62 kHz. The value of output capacitors for all three outputs can be calculated using Equation 13.

\[
C_{\text{OUT}} \gg \frac{I_{\text{OUT}}}{f \times V_{\text{RIPPLE}}}
\]

(13)

\[
C_{\text{OUT1}} \gg \frac{0.2}{62 \times 10^{-3} \times 0.250} \implies 12.9 \, \mu F
\]

\[
I_{\text{COUT1\_RMS}} = \sqrt{(I_{\text{RMS1}})^2 - (I_{\text{OUT1}})^2}
\]

\[
I_{\text{COUT1\_RMS}} = \sqrt{(0.306)^2 - (0.2)^2} = 0.232 \, A
\]

Similarly, the value of output capacitor for other outputs can be found out:

\[
C_{\text{OUT2}} \gg \frac{0.25}{62 \times 10^{-3} \times 0.250} \implies 16.13 \, \mu F
\]

\[
I_{\text{COUT2\_RMS}} = \sqrt{(I_{\text{RMS2}})^2 - (I_{\text{OUT2}})^2}
\]

\[
I_{\text{COUT2\_RMS}} = \sqrt{(0.382)^2 - (0.25)^2} = 0.288 \, A
\]

\[
C_{\text{OUT3}} \gg \frac{0.1}{62 \times 10^{-3} \times 0.250} \implies 6.45 \, \mu F
\]

\[
I_{\text{COUT3\_RMS}} = \sqrt{(I_{\text{RMS3}})^2 - (I_{\text{OUT3}})^2}
\]

\[
I_{\text{COUT3\_RMS}} = \sqrt{(0.153)^2 - (0.1)^2} = 0.116 \, A
\]

For this design, a 100-\( \mu \)F, 25-V capacitor (part number: 25YXJ100M5X11) is selected for all the three outputs.
5 Getting Started Hardware

5.1 Test Equipment to Validate Board

- DC source: 0- to 500-V rated
- Digital oscilloscope
- 6½ digit multi-meter (×3)
- Electronic or resistive load

5.2 Test Conditions

Input voltage range
The DC source must be capable of varying between $V_{\text{INDC}}$ of 100-V to 450-V DC. Set the input current limit to 0.4 A.

Output
Connect an electronic load capable of 30 V and load variable in range from 0 to 0.3 A to all the three outputs. A rheostat or resistive decade box can be used in place of an electronic load.

5.3 Test Procedure

1. Connect the DC source at the input terminals (Pin-1 and Pin-3 of connector J1) of the reference board.
2. Connect output terminals (Pin-4, 5 and Pin-6, 5 of connector J1) to the electronic load or rheostat, maintaining correct polarity. Pin-4,6 are output terminal pins for 12 V and 4 V, respectively, and Pin-3,5 are GND terminal pins.
3. Set and maintain a minimum load of about 10 mA.
4. Gradually increase the input voltage from 0 V to a turn-on voltage of 100-V DC.
5. Turn on the load to draw current from the output terminals of the converter.
6. Observe the startup conditions and smooth switching waveforms.
6 Test Results

The test results are divided into multiple sections that cover the steady state performance measurements, functional performance waveforms and test data, transient performance waveforms, and thermal measurements.

6.1 Performance Data

6.1.1 Efficiency and Regulation With Load Variation

Table 3 shows the efficiency and regulation performance data at a 120-V DC input.

<table>
<thead>
<tr>
<th>LOAD (%)</th>
<th>( I_{\text{INDC}} ) (mA)</th>
<th>( P_{\text{INDC}} ) (W)</th>
<th>( V_{\text{OUT1}} ) (V)</th>
<th>( I_{\text{OUT1}} ) (mA)</th>
<th>( V_{\text{OUT2}} ) (V)</th>
<th>( I_{\text{OUT2}} ) (mA)</th>
<th>( V_{\text{OUT3}} ) (V)</th>
<th>( I_{\text{OUT3}} ) (mA)</th>
<th>( P_{\text{OUT}} ) (W)</th>
<th>EFF (%)</th>
<th>% REG ( V_{\text{OUT1}} )</th>
<th>% REG ( V_{\text{OUT2}} )</th>
<th>% REG ( V_{\text{OUT3}} )</th>
<th>POWER LOSS (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0.08</td>
<td>0.01</td>
<td>12.60</td>
<td>—</td>
<td>4.33</td>
<td>—</td>
<td>12.55</td>
<td>—</td>
<td>0</td>
<td>0</td>
<td>0.10</td>
<td>5.10</td>
<td>1.57</td>
<td>0.01</td>
</tr>
<tr>
<td>10</td>
<td>5.55</td>
<td>0.67</td>
<td>12.59</td>
<td>21</td>
<td>4.17</td>
<td>26</td>
<td>12.82</td>
<td>10</td>
<td>0.51</td>
<td>75.9</td>
<td>0.06</td>
<td>1.12</td>
<td>0.60</td>
<td>0.16</td>
</tr>
<tr>
<td>25</td>
<td>12.93</td>
<td>1.55</td>
<td>12.59</td>
<td>52</td>
<td>4.15</td>
<td>58</td>
<td>12.77</td>
<td>26</td>
<td>1.22</td>
<td>78.9</td>
<td>0.03</td>
<td>0.59</td>
<td>0.16</td>
<td>0.33</td>
</tr>
<tr>
<td>50</td>
<td>24.76</td>
<td>2.97</td>
<td>12.59</td>
<td>101</td>
<td>4.13</td>
<td>110</td>
<td>12.74</td>
<td>51</td>
<td>2.37</td>
<td>79.8</td>
<td>0.01</td>
<td>0.03</td>
<td>0.03</td>
<td>0.60</td>
</tr>
<tr>
<td>75</td>
<td>38.56</td>
<td>4.63</td>
<td>12.58</td>
<td>158</td>
<td>4.11</td>
<td>185</td>
<td>12.73</td>
<td>78</td>
<td>3.74</td>
<td>80.9</td>
<td>−0.01</td>
<td>−0.36</td>
<td>−0.09</td>
<td>0.88</td>
</tr>
<tr>
<td>100</td>
<td>50.60</td>
<td>6.07</td>
<td>12.58</td>
<td>211</td>
<td>4.10</td>
<td>245</td>
<td>12.71</td>
<td>102</td>
<td>4.96</td>
<td>81.6</td>
<td>−0.02</td>
<td>−0.63</td>
<td>−0.24</td>
<td>1.12</td>
</tr>
<tr>
<td>120</td>
<td>60.95</td>
<td>7.31</td>
<td>12.58</td>
<td>252</td>
<td>4.09</td>
<td>298</td>
<td>12.70</td>
<td>127</td>
<td>6.01</td>
<td>82.1</td>
<td>−0.07</td>
<td>−0.75</td>
<td>−0.38</td>
<td>1.31</td>
</tr>
</tbody>
</table>

Table 4 shows the efficiency and regulation performance data at a 165-V DC input.

<table>
<thead>
<tr>
<th>LOAD (%)</th>
<th>( I_{\text{INDC}} ) (mA)</th>
<th>( P_{\text{INDC}} ) (W)</th>
<th>( V_{\text{OUT1}} ) (V)</th>
<th>( I_{\text{OUT1}} ) (mA)</th>
<th>( V_{\text{OUT2}} ) (V)</th>
<th>( I_{\text{OUT2}} ) (mA)</th>
<th>( V_{\text{OUT3}} ) (V)</th>
<th>( I_{\text{OUT3}} ) (mA)</th>
<th>( P_{\text{OUT}} ) (W)</th>
<th>EFF (%)</th>
<th>% REG ( V_{\text{OUT1}} )</th>
<th>% REG ( V_{\text{OUT2}} )</th>
<th>% REG ( V_{\text{OUT3}} )</th>
<th>POWER LOSS (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0.08</td>
<td>0.01</td>
<td>12.61</td>
<td>—</td>
<td>4.36</td>
<td>—</td>
<td>12.55</td>
<td>—</td>
<td>0</td>
<td>0</td>
<td>0.17</td>
<td>6.31</td>
<td>−1.99</td>
<td>0.01</td>
</tr>
<tr>
<td>10</td>
<td>4.14</td>
<td>0.68</td>
<td>12.62</td>
<td>21</td>
<td>4.15</td>
<td>26</td>
<td>12.97</td>
<td>11</td>
<td>0.51</td>
<td>75.1</td>
<td>0.18</td>
<td>1.09</td>
<td>1.27</td>
<td>0.17</td>
</tr>
<tr>
<td>25</td>
<td>9.52</td>
<td>1.57</td>
<td>12.61</td>
<td>53</td>
<td>4.12</td>
<td>60</td>
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<td>1.25</td>
<td>79.6</td>
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<td>0.41</td>
<td>0.55</td>
<td>0.32</td>
</tr>
<tr>
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<td>2.95</td>
<td>12.60</td>
<td>101</td>
<td>4.10</td>
<td>110</td>
<td>12.80</td>
<td>51</td>
<td>2.38</td>
<td>80.5</td>
<td>0.03</td>
<td>−0.08</td>
<td>−0.06</td>
<td>0.57</td>
</tr>
<tr>
<td>75</td>
<td>27.67</td>
<td>4.57</td>
<td>12.58</td>
<td>158</td>
<td>4.08</td>
<td>184</td>
<td>12.76</td>
<td>78</td>
<td>3.74</td>
<td>81.8</td>
<td>−0.09</td>
<td>−0.54</td>
<td>−0.35</td>
<td>0.83</td>
</tr>
<tr>
<td>100</td>
<td>36.38</td>
<td>6.00</td>
<td>12.57</td>
<td>211</td>
<td>4.08</td>
<td>244</td>
<td>12.74</td>
<td>102</td>
<td>4.95</td>
<td>82.5</td>
<td>−0.17</td>
<td>−0.56</td>
<td>−0.57</td>
<td>1.05</td>
</tr>
<tr>
<td>120</td>
<td>43.86</td>
<td>7.24</td>
<td>12.58</td>
<td>252</td>
<td>4.09</td>
<td>297</td>
<td>12.70</td>
<td>127</td>
<td>6.01</td>
<td>83.0</td>
<td>−0.09</td>
<td>−0.32</td>
<td>−0.83</td>
<td>1.23</td>
</tr>
</tbody>
</table>
Table 5 shows the efficiency and regulation performance data at a 325-V DC input.

### Table 5. Efficiency and Load Regulation at 325-V DC Input

<table>
<thead>
<tr>
<th>LOAD (%)</th>
<th>I&lt;sub&gt;INDC&lt;/sub&gt; (mA)</th>
<th>P&lt;sub&gt;INDC&lt;/sub&gt; (W)</th>
<th>V&lt;sub&gt;OUT1&lt;/sub&gt; (V)</th>
<th>I&lt;sub&gt;OUT1&lt;/sub&gt; (mA)</th>
<th>V&lt;sub&gt;OUT2&lt;/sub&gt; (V)</th>
<th>I&lt;sub&gt;OUT2&lt;/sub&gt; (mA)</th>
<th>V&lt;sub&gt;OUT3&lt;/sub&gt; (V)</th>
<th>I&lt;sub&gt;OUT3&lt;/sub&gt; (mA)</th>
<th>P&lt;sub&gt;OUT&lt;/sub&gt; (W)</th>
<th>EFF (%)</th>
<th>% REG V&lt;sub&gt;OUT1&lt;/sub&gt;</th>
<th>% REG V&lt;sub&gt;OUT2&lt;/sub&gt;</th>
<th>% REG V&lt;sub&gt;OUT3&lt;/sub&gt;</th>
<th>POWER LOSS (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0.07</td>
<td>0.02</td>
<td>12.6</td>
<td>—</td>
<td>4.4</td>
<td>—</td>
<td>12.6</td>
<td>—</td>
<td>0</td>
<td>0</td>
<td>0.14</td>
<td>6.66</td>
<td>—2.24</td>
<td>0.02</td>
</tr>
<tr>
<td>10</td>
<td>2.11</td>
<td>0.69</td>
<td>12.6</td>
<td>21</td>
<td>4.2</td>
<td>26</td>
<td>13.0</td>
<td>10</td>
<td>0.51</td>
<td>74.3</td>
<td>0.16</td>
<td>1.25</td>
<td>1.07</td>
<td>0.18</td>
</tr>
<tr>
<td>25</td>
<td>4.79</td>
<td>1.56</td>
<td>12.6</td>
<td>52</td>
<td>4.1</td>
<td>58</td>
<td>12.9</td>
<td>26</td>
<td>1.23</td>
<td>79.1</td>
<td>0.10</td>
<td>0.64</td>
<td>0.63</td>
<td>0.32</td>
</tr>
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<td>9.00</td>
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<td>12.6</td>
<td>101</td>
<td>4.1</td>
<td>110</td>
<td>12.8</td>
<td>51</td>
<td>2.38</td>
<td>81.4</td>
<td>0.01</td>
<td>—0.13</td>
<td>—0.06</td>
<td>0.54</td>
</tr>
<tr>
<td>75</td>
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<td>4.48</td>
<td>12.6</td>
<td>159</td>
<td>4.1</td>
<td>184</td>
<td>12.8</td>
<td>78</td>
<td>3.74</td>
<td>83.5</td>
<td>—0.06</td>
<td>—0.68</td>
<td>—0.29</td>
<td>0.74</td>
</tr>
<tr>
<td>100</td>
<td>18.08</td>
<td>5.88</td>
<td>12.6</td>
<td>211</td>
<td>4.1</td>
<td>242</td>
<td>12.8</td>
<td>102</td>
<td>4.96</td>
<td>84.3</td>
<td>—0.08</td>
<td>—0.85</td>
<td>—0.56</td>
<td>0.92</td>
</tr>
<tr>
<td>120</td>
<td>21.78</td>
<td>7.08</td>
<td>12.6</td>
<td>253</td>
<td>4.1</td>
<td>298</td>
<td>12.7</td>
<td>127</td>
<td>6.02</td>
<td>85.1</td>
<td>—0.13</td>
<td>—0.24</td>
<td>—0.79</td>
<td>1.06</td>
</tr>
</tbody>
</table>

Table 6 shows the efficiency and regulation performance data at a 400-V DC input.

### Table 6. Efficiency and Load Regulation at 400-V DC Input

<table>
<thead>
<tr>
<th>LOAD (%)</th>
<th>I&lt;sub&gt;INDC&lt;/sub&gt; (mA)</th>
<th>P&lt;sub&gt;INDC&lt;/sub&gt; (W)</th>
<th>V&lt;sub&gt;OUT1&lt;/sub&gt; (V)</th>
<th>I&lt;sub&gt;OUT1&lt;/sub&gt; (mA)</th>
<th>V&lt;sub&gt;OUT2&lt;/sub&gt; (V)</th>
<th>I&lt;sub&gt;OUT2&lt;/sub&gt; (mA)</th>
<th>V&lt;sub&gt;OUT3&lt;/sub&gt; (V)</th>
<th>I&lt;sub&gt;OUT3&lt;/sub&gt; (mA)</th>
<th>P&lt;sub&gt;OUT&lt;/sub&gt; (W)</th>
<th>EFF (%)</th>
<th>% REG V&lt;sub&gt;OUT1&lt;/sub&gt;</th>
<th>% REG V&lt;sub&gt;OUT2&lt;/sub&gt;</th>
<th>% REG V&lt;sub&gt;OUT3&lt;/sub&gt;</th>
<th>POWER LOSS (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0.07</td>
<td>0.03</td>
<td>12.6</td>
<td>—</td>
<td>4.4</td>
<td>—</td>
<td>12.6</td>
<td>—</td>
<td>0</td>
<td>0</td>
<td>0.14</td>
<td>7.01</td>
<td>—2.20</td>
<td>0.03</td>
</tr>
<tr>
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<td>1.72</td>
<td>0.69</td>
<td>12.6</td>
<td>21</td>
<td>4.1</td>
<td>26</td>
<td>13.0</td>
<td>10</td>
<td>0.51</td>
<td>74.0</td>
<td>0.16</td>
<td>0.95</td>
<td>1.25</td>
<td>0.18</td>
</tr>
<tr>
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<td>3.87</td>
<td>1.55</td>
<td>12.6</td>
<td>52</td>
<td>4.1</td>
<td>58</td>
<td>12.9</td>
<td>26</td>
<td>1.23</td>
<td>79.4</td>
<td>0.10</td>
<td>0.36</td>
<td>0.50</td>
<td>0.32</td>
</tr>
<tr>
<td>50</td>
<td>7.26</td>
<td>2.90</td>
<td>12.6</td>
<td>101</td>
<td>4.1</td>
<td>110</td>
<td>12.8</td>
<td>51</td>
<td>2.38</td>
<td>82.0</td>
<td>0.04</td>
<td>—0.03</td>
<td>—0.06</td>
<td>0.52</td>
</tr>
<tr>
<td>75</td>
<td>11.09</td>
<td>4.43</td>
<td>12.6</td>
<td>159</td>
<td>4.1</td>
<td>184</td>
<td>12.8</td>
<td>78</td>
<td>3.74</td>
<td>84.4</td>
<td>—0.06</td>
<td>—0.43</td>
<td>—0.37</td>
<td>0.69</td>
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<tr>
<td>100</td>
<td>14.55</td>
<td>5.82</td>
<td>12.6</td>
<td>211</td>
<td>4.1</td>
<td>243</td>
<td>12.8</td>
<td>102</td>
<td>4.96</td>
<td>85.2</td>
<td>—0.08</td>
<td>—0.66</td>
<td>—0.46</td>
<td>0.86</td>
</tr>
<tr>
<td>120</td>
<td>17.47</td>
<td>6.99</td>
<td>12.6</td>
<td>253</td>
<td>4.1</td>
<td>297</td>
<td>12.7</td>
<td>127</td>
<td>6.01</td>
<td>86.0</td>
<td>—0.16</td>
<td>—0.20</td>
<td>—0.86</td>
<td>0.98</td>
</tr>
</tbody>
</table>
Table 7 shows the efficiency and regulation performance data at a 450-V DC input.

**Table 7. Efficiency and Load Regulation at 450-V DC Input**

<table>
<thead>
<tr>
<th>LOAD (%)</th>
<th>$I_{INDC}$ (mA)</th>
<th>$P_{INDC}$ (W)</th>
<th>$V_{OUT1}$ (V)</th>
<th>$I_{OUT1}$ (mA)</th>
<th>$V_{OUT2}$ (V)</th>
<th>$I_{OUT2}$ (mA)</th>
<th>$V_{OUT3}$ (V)</th>
<th>$I_{OUT3}$ (mA)</th>
<th>$P_{OUT}$ (W)</th>
<th>EFF (%)</th>
<th>% REG $V_{OUT1}$</th>
<th>% REG $V_{OUT2}$</th>
<th>% REG $V_{OUT3}$</th>
<th>POWER LOSS (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0.07</td>
<td>0.03</td>
<td>12.6</td>
<td>—</td>
<td>4.40</td>
<td>—</td>
<td>12.5</td>
<td>—</td>
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<td>0</td>
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<td>6.75</td>
<td>-2.22</td>
<td>0.03</td>
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<tr>
<td>10</td>
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<td>21</td>
<td>4.20</td>
<td>26</td>
<td>13.0</td>
<td>10</td>
<td>0.51</td>
<td>73.9</td>
<td>0.16</td>
<td>1.10</td>
<td>1.06</td>
<td>0.18</td>
</tr>
<tr>
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<td>3.45</td>
<td>1.55</td>
<td>12.6</td>
<td>52</td>
<td>4.10</td>
<td>58</td>
<td>12.9</td>
<td>26</td>
<td>1.23</td>
<td>79.4</td>
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<td>0.49</td>
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</tr>
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<td>12.6</td>
<td>101</td>
<td>4.10</td>
<td>110</td>
<td>12.8</td>
<td>51</td>
<td>2.38</td>
<td>82.5</td>
<td>0.04</td>
<td>-0.16</td>
<td>0.04</td>
<td>0.51</td>
</tr>
<tr>
<td>75</td>
<td>9.80</td>
<td>4.41</td>
<td>12.6</td>
<td>159</td>
<td>4.10</td>
<td>184</td>
<td>12.8</td>
<td>78</td>
<td>3.75</td>
<td>85.0</td>
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<td>-0.28</td>
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<tr>
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<td>243</td>
<td>12.8</td>
<td>102</td>
<td>4.96</td>
<td>85.8</td>
<td>-0.08</td>
<td>-0.75</td>
<td>-0.50</td>
<td>0.82</td>
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<tr>
<td>120</td>
<td>15.47</td>
<td>6.96</td>
<td>12.6</td>
<td>253</td>
<td>4.11</td>
<td>297</td>
<td>12.7</td>
<td>127</td>
<td>6.02</td>
<td>86.5</td>
<td>-0.19</td>
<td>0.03</td>
<td>-0.80</td>
<td>0.94</td>
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</table>

Table 8 shows the regulation of all three outputs over the input voltage range for full load.

**Table 8. Line Regulation at Full Load**

<table>
<thead>
<tr>
<th>$V_{INPUT}$</th>
<th>12-V OUTPUT</th>
<th>4-V OUTPUT</th>
<th>12-V_ISO OUTPUT</th>
<th>% REG 12 V</th>
<th>% REG 4 V</th>
<th>% REG 12 V_ISO</th>
</tr>
</thead>
<tbody>
<tr>
<td>120 V</td>
<td>12.582</td>
<td>4.098</td>
<td>12.714</td>
<td>-0.032</td>
<td>0.476</td>
<td>-0.304</td>
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<tr>
<td>165 V</td>
<td>12.572</td>
<td>4.082</td>
<td>12.736</td>
<td>-0.111</td>
<td>0.083</td>
<td>-0.132</td>
</tr>
<tr>
<td>325 V</td>
<td>12.591</td>
<td>4.068</td>
<td>12.769</td>
<td>0.040</td>
<td>-0.260</td>
<td>0.127</td>
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<tr>
<td>400 V</td>
<td>12.593</td>
<td>4.067</td>
<td>12.775</td>
<td>0.056</td>
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<td>0.174</td>
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<tr>
<td>450 V</td>
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<td>4.078</td>
<td>12.770</td>
<td>0.048</td>
<td>-0.015</td>
<td>0.135</td>
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6.1.2 Standby Power

The standby power was noted at multiple DC input voltages with no load on the output DC bus. The results are shown in Table 9:

Table 9. No Load Power Across Input Voltage

<table>
<thead>
<tr>
<th>$V_{\text{INDC}}$ (VDC)</th>
<th>$I_{\text{INDC}}$ (mA)</th>
<th>$P_{\text{INDC}}$ (mW)</th>
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<tr>
<td>120</td>
<td>0.08</td>
<td>10.08</td>
</tr>
<tr>
<td>165</td>
<td>0.08</td>
<td>13.20</td>
</tr>
<tr>
<td>325</td>
<td>0.07</td>
<td>23.40</td>
</tr>
<tr>
<td>400</td>
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<td>28.40</td>
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<tr>
<td>450</td>
<td>0.07</td>
<td>31.50</td>
</tr>
</tbody>
</table>
6.2 Performance Curves

6.2.1 Efficiency With Load Variation

Figure 3 shows the measured efficiency of the system with DC input voltage variation.

![Image of Figure 3: Efficiency versus Output Power](image)

6.2.2 Load Regulation in Constant Voltage (CV) Mode

Figure 4 shows the measured load regulation of the 12-V output. The load regulation for all the outputs is measured with equal percentage of full load on each of the rails.

![Image of Figure 4: Output Voltage Variation With Load Current in CV Mode](image)
Figure 5 shows the measured load regulation of the 4-V output:

Figure 6 shows the measured load regulation of the 12-V_ISO output:

Figure 5. Output Voltage Variation With Load Current in CV Mode

Figure 6. Output Voltage Variation With Load Current in CV Mode
6.3 **Functional Waveforms**

6.3.1 **Flyback MOSFET Switching Node Waveforms**

The waveforms at the flyback switching node (SW) was observed along with the MOSFET current for 165-V DC and 400-V DC under full load conditions.

**NOTE:** Red trace: Drain voltage, 200 V/div; Green trace: Drain current, 500 mA/div

---

**Figure 7.** SW Node Waveform and MOSFET Current at $V_{\text{INDC}} = 165$-V DC, Full Load

---

**Figure 8.** SW Node Waveform and MOSFET Current at $V_{\text{INDC}} = 400$-V DC, Full Load
6.3.2 Output Rectifier Diode Voltage (VD) Waveforms

Waveforms at all the secondary output rectifier diodes were observed at 400-V DC under full load conditions. The maximum voltage across the diode is well within their breakdown voltage. Figure 9, Figure 10, and Figure 11 show the voltage waveforms at the 12-V, 4-V, and 12-V_ISO rectifier diodes, respectively.

NOTE: Red trace: Drain-to-source voltage, 10 V/div

Figure 9. Rectifier Diode for 12-V Output (V_{D1}) Waveform at \( V_{INDC} = 400-V \) DC, Full Load

Figure 10. Rectifier Diode for 4-V Output (V_{D2}) Waveform at \( V_{INDC} = 400-V \) DC, Full Load

Figure 11. Rectifier Diode for 12-V_ISO Output (V_{D3}) Waveform at \( V_{INDC} = 400-V \) DC, Full Load
6.3.3 Output Ripple

Ripple is observed at all three outputs at full load for both 165-V and 400-V DC inputs. Peak-to-peak ripple voltage is less than 300 mV. Figure 12 and Figure 13 show the ripple for 12-V output at the 165-V DC input and 400-V DC input, respectively.

Figure 12. 12-V Output Voltage Ripple at $V_{\text{INDC}} = 165$-V DC, Full Load

Figure 13. 12-V Output Voltage Ripple at $V_{\text{INDC}} = 400$-V DC, Full Load

Figure 14 and Figure 15 show the ripple for the 4-V output at the 165-V DC input and 400-V DC input, respectively.

Figure 14. 4-V Output Voltage Ripple at $V_{\text{INDC}} = 165$-V DC, Full Load

Figure 15. 4-V Output Voltage Ripple at $V_{\text{INDC}} = 400$-V DC, Full Load
Figure 16 and Figure 17 show the ripple for the 12-V_ISO output at the 165-V DC input and 400-V DC input, respectively.

Figure 16. 12-V_ISO Output Voltage Ripple at $V_{INDC} = 165$-V DC, Full Load

Figure 17. 12-V_ISO Output Voltage Ripple at $V_{INDC} = 400$-V DC, Full Load

6.4 Transient Waveforms

6.4.1 Turn-on Characteristics

The output turn on of all the rails at full load were recorded with a resistive load. Figure 18 and Figure 19 show the turn-on waveforms for the 12-V output at 165-V and 400-V DC inputs at full load (0.2 A).

NOTE: Red trace: Output voltage, 5 V/div; Green trace: Output current, 100 mA/div

Figure 18. Output Turn-on Waveform for 12-V Output at 165-V DC Input

Figure 19. Output Turn-on Waveform for 12-V Output at 400-V DC Input
Figure 20 and Figure 21 show the turn on waveforms for the 4-V output at 165-V and 400-V DC inputs at full load (0.25 A).

NOTE: Red trace: Output voltage, 2 V/div; Green trace: Output current, 100 mA/div

Figure 22 and Figure 23 show the turn-on waveforms for 12-V_ISO output at the 165-V and 400-V DC inputs at full load (0.1 A).

NOTE: Red trace: Output voltage, 5 V/div; Green trace: Output current, 50 mA/div
6.4.2 Transient Load Response

Load transient performance was observed for primary referred ground outputs (12 V, 4 V) with the load switched at a 0.2-m wire length. The output load is switched using an electronic load.

Figure 24 gives the transient load response of the 12-V output at \( V_{IN} = 400 \text{V} \) DC with a load transient from 20 to 200 mA and Figure 25 depicts a load transient from 200 to 20 mA.

**NOTE:** Red trace: Output voltage, 1 V/div, AC coupling; Green trace: Output current, 100 mA/div.

Figure 24. 12-V Output Voltage Waveform, Load Transient From 20 to 200 mA

Figure 25. 12-V Output Voltage Waveform, Load Transient From 200 to 20 mA

Figure 26 gives the transient load response of the 4-V output at \( V_{IN} = 400 \text{V} \) DC with a load transient from 25 to 250 mA and Figure 27 depicts a load transient from 250 to 25 mA.

Figure 26. 4-V Output Voltage Waveform, Load Transient From 25 to 250 mA

Figure 27. 4-V Output Voltage Waveform, Load Transient From 250 to 25 mA
6.4.3 Short Circuit Response

A short was applied and removed to observe the output turn-off and auto-recovery cycle. When short is applied, the converter detects it and reduces Ton time significantly until it detects that the problem has been resolved. Once the short is removed, the converter recovers back to normal operation. Figure 28 shows the output current and voltage waveform for the main 12-V output, which clearly shows the behavior of the controller during short circuit and its recovery; the short was applied a number of times to make sure the controller behaves as expected even in case of multiple shorts.

NOTE: Red trace: Output voltage, 10 V/div; Green trace: Output current, 2 A/div.

Figure 28. Response During Short Circuit and Auto-Recovery When Short is Removed

6.4.4 Overvoltage Response

The overvoltage response was observed by applying an external voltage source to one of the outputs (12-V/0.2-A rail in this case) that is approximately 20% higher than the regulated $V_{OUT}$ with the other two rails loaded. The observation in this waveform suggests that the IC stops switching when it detects overvoltage, thus protecting the system. Figure 29 shows the overvoltage response.

Figure 29. Overvoltage Response
6.5 Thermal Measurements

Thermal images are plotted at room temperature (25°C) with a closed enclosure, no airflow with full load conditions, and after keeping the board continuously switched on for 30 minutes before capturing the image.

6.5.1 Thermal Image for Lo-Line (115-V AC) Operation

Figure 30 and Figure 31 show the top and bottom thermal images, respectively, with an input voltage of 400-V DC and a full load at 5 W.

![Figure 30. Top Side Temperatures at 400-V DC Input](image)
The temperatures are kept low and have higher margins from its respective device’s junction temperatures.
7 Design Files

7.1 Schematics

To download the schematics, see the design files at TIDA-00708.

Figure 32. TIDA-00708 Schematics

*Short Pin U2-1 and Pin U2-5 to Bypass LDO.*
### 7.2 Bill of Materials

To download the bill of materials (BOM), see the design files at [TIDA-00708](https://www.ti.com).

**Table 11. BOM**

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<th>DESIGNATOR</th>
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<td>Any</td>
<td>Printed Circuit Board</td>
<td></td>
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<td>13x5x11mm</td>
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<td>0603</td>
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<td>Rubycon</td>
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<td>Kemet</td>
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<td>S1J</td>
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<td>BZT52C5V1-G3-08</td>
<td>Vishay-Semiconductor</td>
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<td>Panasonic</td>
<td>RES, 10.0 k, 1%, 0.1 W, 0603</td>
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<td>Transformer, 9-LEAD, TH</td>
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<td>U2</td>
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<td>TLV70233DBVR</td>
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<td>Single Output LDO, 300 mA, Fixed 3.3 V Output, 2 to 5.5 V Input, with Low IQ, 5-pin SOT-23 (DBV), -40 to 125 degC, Green (RoHS &amp; no Sb/Br)</td>
<td>DBV0005A</td>
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7.3 PCB Layout Guidelines

A careful PCB layout is critical and extremely important in a fast-switching circuit involving magnetics to provide appropriate device operation and design robustness.

7.3.1 Power Stage Specific Guidelines

Follow these key guidelines to route power stage components:

- Minimize the loop area and trace length of the power path circuits, which contain high frequency switching currents. This helps to reduce EMI and improve converter overall performance.
- Keep the switch node as short as possible. A short and optimal trace width helps to reduce induced ringing caused by parasitic inductance.
- Keep traces with high dV/dt potential and high di/dt capability away from or shielded from sensitive signal traces with adequate clearance and ground shielding.
- For each power supply stage, keep power ground and control ground separate. Tie them together (if they are electrically connected) in one point near DC input return or output return of the given stage correspondingly.
- Place protection devices such as TVS, snubbers, capacitors, or diodes physically close to the device they are intended to protect, and route them with short traces to reduce inductance.
- Choose the width of PCB traces based on acceptable temperature rise at the rated current as per IPC2152 as well as acceptable DC and AC impedances. Also, the traces should withstand the fault currents (such as short circuit current) before the activation of electronic protection such as fuse or circuit breaker.
- Determine the distances between various traces of the circuit according to the requirements of applicable standards. For this design, follow the UL 60950-1 safety standard to maintain the creepage and clearance from live line to neutral line and to safety ground as defined in the Tables 2K through 2N of this standard.
- Adapt thermal management to fit the end-equipment requirements.
- See the placement and routing guidelines and layout example present in the UCC28881 datasheet (SLUSC36).

7.3.2 Layout Prints

To download the layer plots, see the design files at TIDA-00708.

7.4 Altium Project

To download the Altium project files, see the design files at TIDA-00708.

7.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00708.

7.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00708.
8 References


9 About the Author

**NEHA NAIN** is a Systems Engineer at Texas Instruments where she is responsible for developing reference design solutions for the Power Delivery, Industrial Segment. Neha earned her bachelor of electrical and electronics engineering from the PES Institute of Technology (now PES University), Bangalore.
## Revision B History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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## Revision A History

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