

TI Designs

Multi-Phase Power Quality Measurement With Isolated Shunt Sensors



Design Overview

This reference design measures power quality parameters in a polyphase energy measurement system and calculates total harmonic distortion (THD), fundamental readings, and standard metrology parameters such as active and reactive energy and power. Phase-to-phase angles are also calculated to help prevent incorrect installation of the system. This design uses isolated shunt current sensors to maintain accuracy in harmonic analysis and also immunity from magnetic tamper attacks.

Design Resources

TIDA-01088	Design Folder
AMC1304M05	Product Folder
SN6501	Product Folder
MSP430F67641	Product Folder
TRS3232	Product Folder
ISO7321C	Product Folder
TPS76333	Product Folder
ISO7320C	Product Folder

Design Features

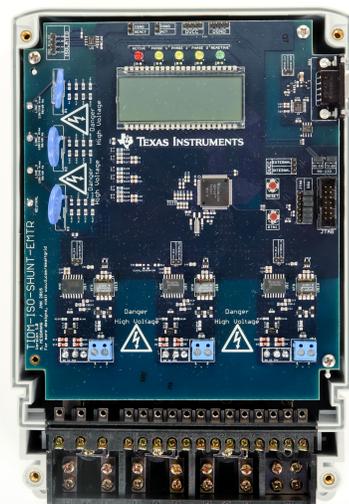
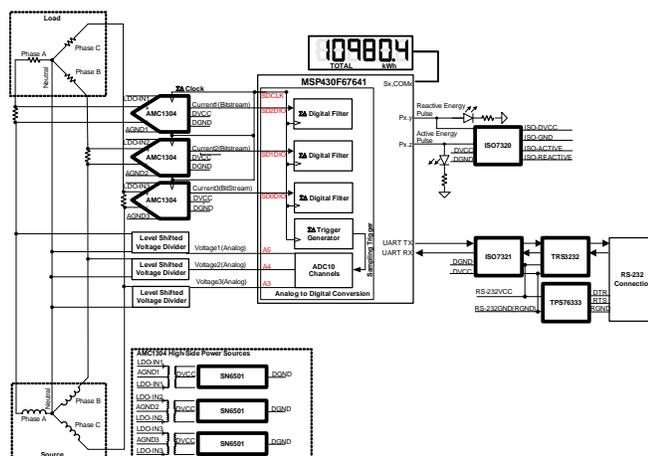
- Class 0.5% Three-Phase Metrology With Galvanically Isolated Shunt Current Sensors
- Isolation Performance of up to 1-kV AC (Working Voltage) and 7-kV (Peak) THD Calculated for Voltage and Current
- Voltage Sag and Swell Events Logged With Programmable Threshold Levels
- Phase-to-Phase Angle Measurement for Determining Phase Sequence to Help Prevent Incorrect Installation of System
- Complete Energy Library With Fundamental Voltage and Current, Fundamental Active and Reactive Power, Active and Reactive Energy, Root Mean Square (RMS) Current and Voltage, Power Factor, and Line Frequency

Featured Applications

- Power Quality Meters
- Power Quality Analyzers
- Power Distribution Unit
- Street Lighting
- Electricity Meters



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1 Key System Specifications

Table 1. Key System Specifications

FEATURES	DESCRIPTION
Number of phases	3
Accuracy class	Class 0.5
Current sensor	Shunt
Voltage ADC type	SAR (MSP430F67641)
Current ADC type	Delta-sigma modulator (AMC1304M05) + sinc ³ filter (MSP430F67641)
Delta-sigma (for current channels) modulation clock frequency	19,798,016 Hz
Delta-sigma (for current channels) OSR	1024
Delta-sigma (for current channels) output sample rate	19,334 samples per second
Ratio of skipped samples to total samples ⁽¹⁾	4 to 5
Effective sample rate (for both current and voltage) ⁽¹⁾	3866.8 samples per second
Phase compensation implementation	Software
Phase compensation resolution ⁽¹⁾	0.0182° at 50 Hz; 0.0218° at 60 Hz
Selected CPU clock frequency	19,798,016 Hz
System nominal frequency	50 or 60 Hz
Measured parameters ⁽¹⁾	<ul style="list-style-type: none"> • Voltage and current THD • Fundamental voltage, fundamental current, fundamental active power, and fundamental reactive power • Sag and swell • Phase-to-phase angle • Active power, reactive power, and apparent power and energy • Root mean square (RMS) current and voltage • Power factor • Line frequency
Utilized LEDs ⁽¹⁾	Total active energy and total reactive energy
Communication	LCD; PC GUI through isolated RS-232
Isolated modulator high-side power	<ul style="list-style-type: none"> • Option 1: Power derived from controller-side using transformer driver(SN6501) + transformer; 1 set per phase • Option 2: External power
Key devices	AMC1304M05, SN6501, MSP430F67641, TRS3232, ISO7321C, TPS76333, and ISO7320C

⁽¹⁾ Different from TIDA-00601 feature

2 System Description

The presence of harmonics can have a negative impact on both consumer loads and the electricity grid. This design implements a Class 0.5 three-phase shunt-based energy measurement system that measures the total harmonic distortion (THD), which can ensure that the current drawn by a customer's load does not significantly degrade the voltage delivered from the utility to other customers. For additional power quality information on the supply, voltage sags and swells are also logged. In addition, this design measures phase-to-phase angles, which can help in determining phase sequence and prevent accidentally swapping phases when installing an energy measurement system. This design supports four-quadrant energy measurement for logging energy consumption and generation in systems that could both provide electricity to the utility company or consume the energy generated from the utility companies.

Historically, current transformers have been used as current sensors for polyphase systems due to their inherent isolation. When compared to shunt current sensors, current transformers have the disadvantage of causing degradation in the results from harmonic analysis. This design is a polyphase system that uses shunt current sensors to prevent the degradation of the results from harmonic analysis. The shunts are isolated to address the shunt's lack of inherent isolation. This protection is achieved through the use of isolated delta-sigma modulators that use capacitive isolation to isolate the output circuitry from the input. An energy measurement system on chip (SoC) takes the bit-streams from the isolated modulators and uses integrated digital filters to produce ADC sample results. The energy measurement SoC is also used for sensing voltages, calculating metrology parameter values, driving the board's liquid crystal display (LCD), and communication to a PC GUI through the board's isolated RS-232 circuitry.

2.1 AMC1304M05

The AMC1304 is used to provide isolated current measurement for the designs shunt current sensors. This isolated current measurement is accomplished by the AMC1304 providing a modulation bit-stream output that is capacitively isolated from the analog signal fed from the shunts to the AMC1304, as [Figure 1](#) shows.

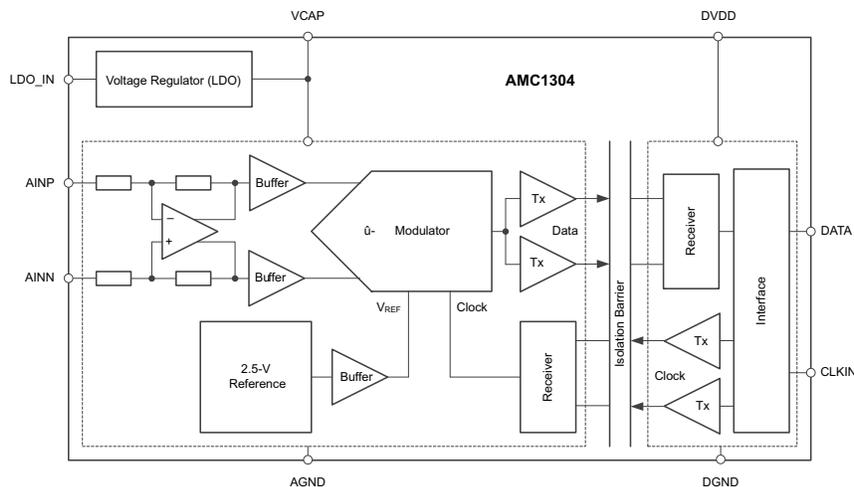


Figure 1. AMC1304 Simplified Block Diagram

In [Figure 1](#), the shunt current measurement is made across terminals AINP and AINN of the AMC1304. The third terminal of the shunt is then connected to AGND of the AMC1304. To perform measurements, 4 V to 18 V must be fed between LDO_IN and AGND. The AMC1304 then uses its integrated low dropout voltage (LDO) regulator to power the high-side of the chip, which includes the modulator.

To properly power the controller-side, pins DVDD and DGND on the AMC1304 must be connected to DVCC and DGND of the MSP430F67641. In addition, the modulation clock used by the MSP430F67641's SD24_B digital filters must be connected to CLKIN. This modulation clock must be between 5 MHz to 20 MHz for the AMC1304 to properly work and can either be generated from the clock output of the MSP430 SD24_B module or from an external clock generator that is fed to both the MSP430F67641 SD24_B and the AMC1304s. With a proper clock fed into CLKIN, the bit-stream is output from the AMC1304s DATA pin. This DATA pin must be connected to the MSP430F67641 digital bit-stream input.

For selecting an AMC1304 chip, there are four device variations. Two of these variations correspond to a CMOS digital interface option (denoted with an "M" in the part name) and the other two correspond to a low-voltage differential signaling (LVDS) digital interface option (denoted with an "L" in the part name). To properly interface to the MSP430F67641, select the CMOS options. From the CMOS options, there is an option to choose from having a ± 50 -mV input range (denoted with a "05" in the part name) or a ± 250 -mV input range (denoted with a "25" in the part name). For e-meter applications, typically shunts with small resistances are used to reduce the power dissipation of the shunt; therefore, to use the full input range of the AMC1304, the ± 50 -mV input range must be used instead of the ± 250 -mV input range. As a result, the AMC1304M05 is the AMC1304 device variation that is best suited for this design.

For the AMC1304M05 device variant, if the input voltage value exceeds ± 50 mV, there is degradation in the accuracy of readings. Also, to find out the density of ones that result from applying a certain differential input voltage (assuming it is not at the full-scale voltage or beyond this), use the following formula in

[Equation 1](#):

$$\%_{\text{HIGH}} = 100 \times \left(\frac{V_{\text{input}} + 0.625}{1.25} \right) \quad (1)$$

From this formula, a differential input voltage of 0 V corresponds to the associated bit-stream that has a stream of ones and zeros that are high 50% of the time, a differential input voltage of 50 mV has ones and zeros that are high 90% of the time, and a differential input of -50 mV produces a stream of ones and zeros that are high 10% of the time.

2.2 SN6501

Each AMC1304 needs 4 V to 18 V fed into its LDO_IN pin to power the high-side of the chip. In the design, this voltage can derive from an on-board isolated power supply. This isolated power supply uses DVCC as a voltage input, a transformer, and a transformer driver to provide the necessary isolated voltage that feeds into LDO_IN. The transformer driver functionality is done by using the SN6501.

2.3 MSP430F67641

For sensing and calculating the metrology parameters, the MSP430F67641 energy measurement SoC is used. This device is the latest metering SoC that belongs to the MSP430F67xx family of devices. This family of devices belongs to the powerful 16-bit MSP430F6xx platform, which brings in many new features and provides flexibility to support robust poly-phase metrology solutions. These chips are intended for energy measurement applications and have the necessary architecture to support this application.

The MSP430F67xx devices have a delta-sigma ADC module (SD24_B) with ADCs that have the capability to use their own internal modulator or an external modulator. In this design, the external modulator option is used so that the MSP430F67641's sinc³ digital filter can be used with the isolated delta-sigma modulators that measure the current. Figure 2 shows the block diagram of one of these SD24_B converters. In Figure 2, the items shaded red are used when the external modulation option is selected and the items that are unshaded are bypassed when using an external modulator.

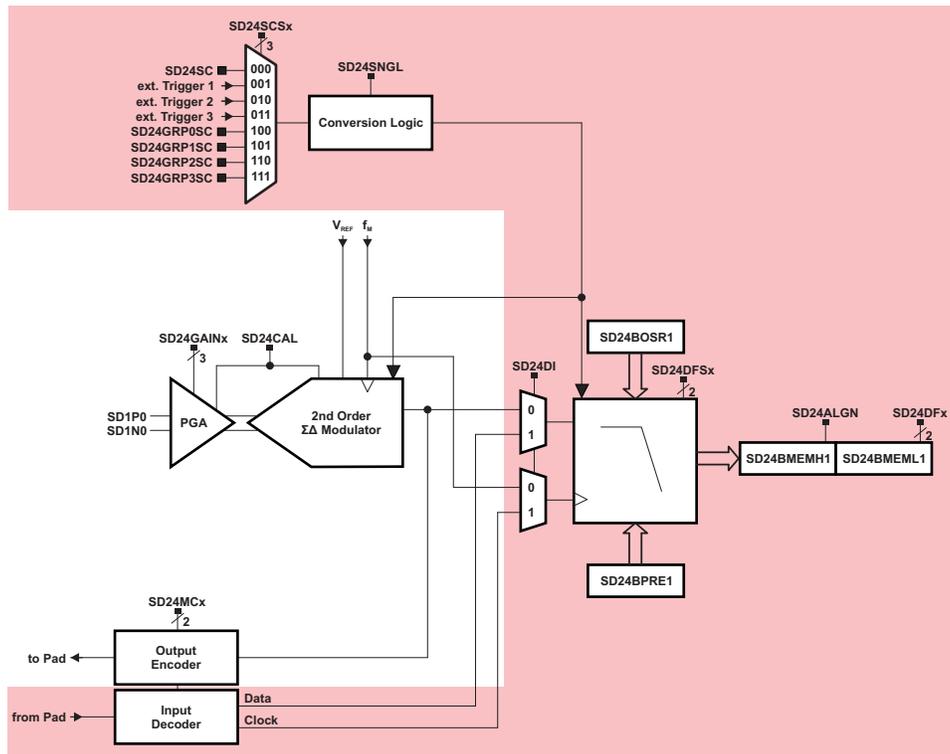


Figure 2. SD24_B Converter Block Diagram

To minimize the number of isolated delta-sigma modulators in the design, the modulators are only used for measuring current. As a result of using these modulators, the modulation clock frequency used in the SD24_B module is too high to be able to use the internal modulator of any extra SD24_B ADCs that are not already connected to the external modulators. Because of this constraint, the integrated 10-bit SAR ADCs of the MSP430F67641 are used for sensing phase voltages as is done in the following design: [TIDM-THREEPHASEMETER-F67641](#).

Using the MSP430F67641's SAR converters for measuring voltage has the advantage of not attenuating higher frequency components like what happens when using a delta sigma converter with a sinc³ filter. To synchronize these SAR ADCs and the SD24_B, all of the MSP430F67xx polyphase devices have a trigger generator that triggers the ADC10 to ensure that the timing between the ADC10 and SD24_B modules are grouped and synchronized. Figure 3 shows the block diagram of this trigger generator.

Trigger Generator

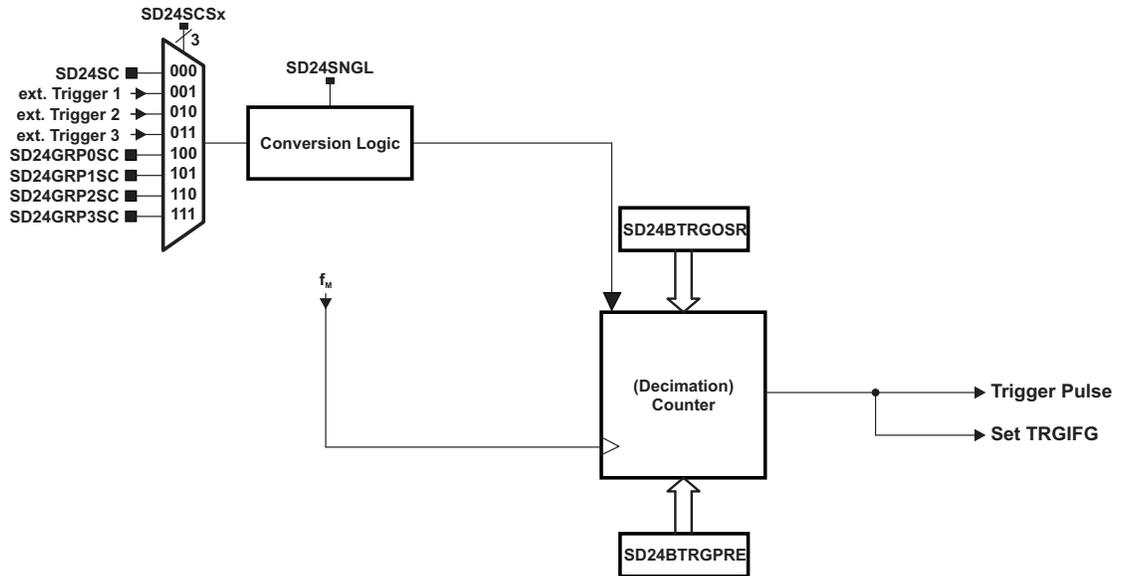


Figure 3. SD24_B Trigger Generator Block Diagram

2.4 TRS3232

To properly interface with the RS-232 standard, a voltage translation system is required to convert between the 3.3-V domain on the board and from the 12 V on the port itself. To facilitate the translation, the design uses a TRS3232 device. The TRS3232 device is capable of driving the higher voltage signals on the RS-232 port from only the 3.3-V DVCC through a charge pump system.

2.5 ISO7321

To add isolation to the RS-232 connection to a PC, the isolated RS-232 portion of this design uses capacitive galvanic isolation, which has an inherent lifespan advantage over an opto-isolator. In particular, industrial devices are usually pressed into service for much longer periods of time than consumer electronics; therefore, maintenance of effective isolation over a period of 15 years or longer is important.

The TI ISO7321 device is a simple dual-channel isolator that is capable of operating at 3.3 V or 5 V, enabling a wide range of devices that can connect to the data circuit-terminating equipment (DCE) side of the interface. The ISO7321 device can simply be inserted into a universal asynchronous receiver/transmitter (UART) signal path, with the appropriate power supplies on each side to enable operation. The ISO7321 device also maintains 3 kV of isolation in order to meet Underwriters Laboratories (UL) certification levels.

The ISO7321 is available as the ISO7321C and ISO7321FC variants, where the difference of these variants is in whether the default output is high or low. Although both variants can be used in the design, in this design, the ISO7321C is specifically used.

2.6 TPS76333

To power the data terminal equipment (DTE) side of the isolation boundary and the RS-232 charge pump, there are two choices. The interface can either implement an isolated power supply or harvest power from the RS-232 line. Integrating a power supply adds cost and complexity to the system, which is difficult to justify in low-cost sensing applications.

To implement the second option of harvesting power from the RS-232 port itself, this design utilizes the flow control lines that are ignored in most embedded applications. The RS-232 specification (when properly implemented on a host computer or adapter cable), keeps the request to send (RTS) and data terminal ready (DTR) lines high when the port is active. As long as the host has the COM port open, these two lines retain voltage on them. This voltage can vary from 5 to 12 V, depending on the driver implementation. The 5 to 12 V is sufficient for the use requirements in this design.

The voltage is put through a diode arrangement to block signals from entering back into the pins. The voltage charges a capacitor to store energy. The capacitor releases this energy when the barrier and charge pump pull more current than what is instantaneously allowed. The TPS76333 is used to bring the line voltage down to a working voltage for the charge pump and isolation device.

2.7 ISO7320

To test the active energy and reactive energy accuracy of a meter, pulses are output at a rate proportional to the amount of energy consumed. A reference meter can then determine the accuracy of a meter by calculating the error based on these pulses and how much energy is provided to the meter. In this design, pulses are output through headers for the cumulative active and reactive energy consumption. The use of the ISO7320 provides an isolated version of these headers for connection to non-isolated equipment. These isolated active and reactive signals can be set to have either a 3.3- or 5-V maximum voltage output by applying the selected maximum voltage output between the isolated sides VCC (ISO_VCC) and the isolated sides GND (ISO_GND).

The ISO7320 is available as the ISO7320C and ISO7320FC variants, where the difference of these variants is in whether the default output is high or low. Both variants can be used; however, in this design, the ISO7320C is specifically used.

3 System Design Theory

3.1 Design Hardware Implementation

3.1.1 Analog Inputs

The design of the front end consists of the three AMC1304 chips used for measuring current, the MSP430F67641s three digital filters that are connected to each AMC1304, a 10-bit SAR ADC (ADC10_A), and a mechanism to synchronize the digital filters with the SAR ADC.

For maximum accuracy, the AMC1304 requires that the input analog signal voltage does not exceed ± 50 mV. In addition, the AMC1304 has differential inputs; therefore, the AC current signal from mains can be directly interfaced without the requirement for level shifters.

In contrast, the ADC10_A module has single-ended inputs. Therefore, the ADC10_A requires that the sensed voltage is between $0-V_{REF}$ volts, with the option to select the V_{REF} source and voltage in the software. As a result, after the mains voltage is divided down for sensing, the voltage front-end circuitry requires a level shifter to properly interface to the ADC10_A module.

3.1.1.1 Voltage Analog Front-End

The voltage from the mains is usually 230 V or 120 V and must be brought down to within V_{REF} volts. The analog front-end for voltage consists of spike protection varistors followed by a voltage divider and shifter network, and a RC low-pass filter that functions like an anti-alias filter.

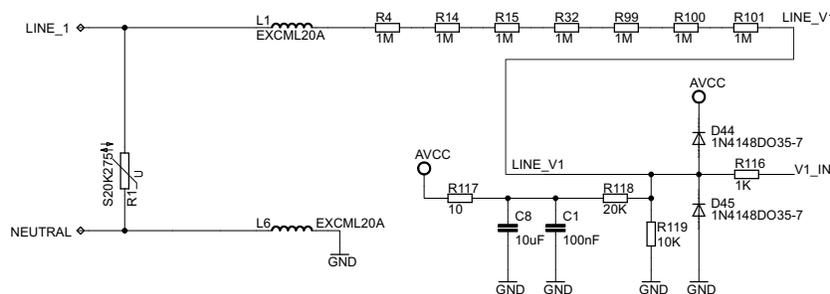


Figure 4. Analog Front-End for Voltage Inputs

Figure 4 shows the analog front-end for the voltage inputs for a mains voltage of 230 V. The voltage is brought down to a range within V_{REF} volts, where V_{REF} is selected to be the 2.0-V reference produced by the chips reference module. The maximum voltage that is fed to the ADC is usually a certain margin below the maximum V_{REF} voltage. As an example, when the 2.0-V reference is selected, the front end may be built to produce a maximum voltage of 1.4 to 1.6 V when the maximum mains voltage is applied. This margin helps prevent ADC clipping when the system is exposed to harmonics or an over-voltage condition.

3.1.1.2 Current Front-End

3.1.1.2.1 AMC1304 High-Side Power Supply

To sense the voltage across the shunt, the high-side of each AMC1304 device must be powered. Because each AMC1304 must be referenced from a different line voltage, a different power supply is required for each AMC1304. Figure 5 shows the designs different power options for the AMC1304.

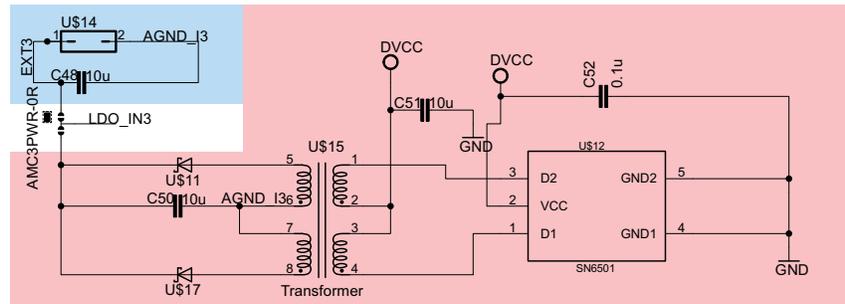


Figure 5. AMC1304 High-Side Power Options

In Figure 5, LDO_IN3 is fed directly into the AMC1304 to provide power to it. Because the AMC1304 has an integrated LDO, LDO_IN3 can be unregulated as long as the voltage fed into LDO_IN of the AMC1304 is within the 4- to 18-V operating range.

In this design, there are two options for powering the high side of the AMC1304. The first option (shaded blue in Figure 5), is to provide the necessary 4- to 18-V from an external isolated voltage supply to its associated terminal block (U\$14 in Figure 5). The second option (shaded red in Figure 5), is to use the on-board isolated power supply that uses DVCC as a voltage input, a transformer, and the SN6501 transformer driver to provide an unregulated voltage into the AMC1304s integrated LDO input. In this design, a ferromagnetic core transformer is used; however, the SN6501 can also be used with an air-core transformer instead.

For further details on this power supply implementation, see Section 3.6 of the *Isolated, Shunt-Based Current Sensing Reference Design (TIDU384)*.

3.1.1.2.2 Current Sensing

The analog front-end for current inputs is different from the analog front-end for the voltage inputs. Figure 6 shows the analog front-end used for a current channel.

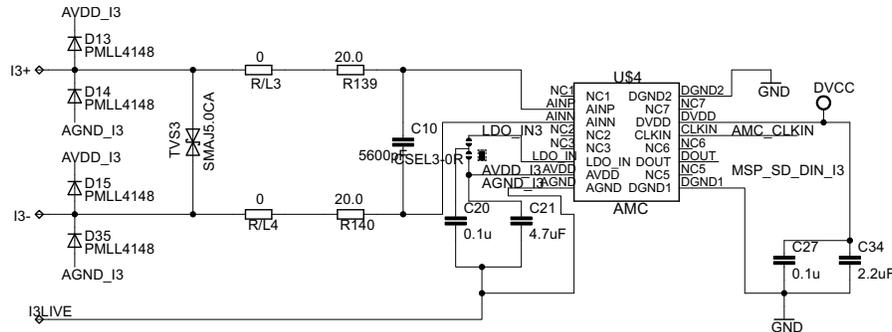


Figure 6. Analog Front-End for Current Inputs

The analog front-end for current consists of diodes and transorbs for any additional transient voltage suppression, footprints (R/L3 and R/L4) that could be replaced with inductors for EMI suppression (these footprints are populated with 0-Ω resistors by default), an anti-alias filter (R139, R140, and C10), and the AMC1304 isolated delta-sigma modulator.

In Figure 6, the three-terminal shunt used for current measurement is to be connected at I3+, I3-, and I3Live. The value of this shunt is selected based on balancing maximizing the peak analog voltage input into the AMC1304 with minimizing the power dissipation of the shunt. In particular, for optimal accuracy, the peak DC voltage fed into the AMC1304 must be as close as possible to 50 mV without surpassing this voltage. This peak voltage is dependent on the rated maximum current of the system and the resistance of the selected shunt. For example, this design uses 400-μΩ shunts (utilized shunts are shown here: <http://www.vishay.com/docs/30173/wsms3124.pdf>). With these 400-μΩ shunts and a maximum RMS current of 90 A, the maximum DC voltage fed into the AMC1304 is $90 \times \sqrt{2} \times (400 \times 10^{-6}) \approx 50$ mV. To minimize the power dissipation in the shunt, a smaller value shunt can also be used. In this design, 200-μΩ shunts are also used. However, by using smaller value shunts, the voltage fed into the AMC1304 is also reduced. As a result, there is a tradeoff in accuracy. Based on the requirements of the system, the tradeoff in accuracy from using a shunt with a small resistance and the reduced power dissipation from choosing the smaller shunt must be taken into account when selecting the proper shunt value.

3.2 Metrology Software Implementation

This section discusses the software for the implementation of three-phase metrology. The first subsection discusses the setup of various peripherals of the metrology and application processors. Subsequently, the metrology software is described as two major processes: the foreground process and background process.

3.2.1 Peripherals Setup

3.2.1.1 SD24_B Setup

The MSP430F67641 has three delta-sigma data converters, with each of them having the ability to bypass its internal modulator and accept an external bit-stream to be used with its associated digital filters. This feature is used to obtain ADC samples using the bit-stream input that is output from the AMC1304.

In addition, the SD24_B has a trigger generator module that is used to trigger the ADC10, which in turn is used to sense the corresponding three voltages of the three-phase system. In this application, all of the digital filters for the SD24_B ADCs and the trigger generator are grouped together for synchronization.

The modulation clock (f_M) to the trigger generator and the digital filters of the SD24_B ADCs is derived from system clock, which is configured to run at 19,798,016 Hz. Because the AMC1304 can support a clock from 5 MHz to 20 MHz, this clock can be used as the modulation clock for the AMC1304 without being further divided down. Similarly, the sinc^3 digital filters of the MSP430F67641s SD24_B ADC can also operate at this 20-MHz modulation clock frequency (unlike the internal modulators of the SD24_B ADC, which are bypassed in this application). In this design, the modulation clock used in the SD24_B is derived internally and output from the SD24_B module to the AMC1304 device.

To reduce the central processing unit (CPU) utilization, the effective sample rate is divided down to 3866.8 samples per second. This reduction is first accomplished by choosing the highest OSR setting for the digital filters and trigger generator, which is 1024. Because the sampling frequency is defined as $f_s = f_M / \text{OSR}$, this results in a sampling frequency of 19334. To further divide this sample rate, the software skips the ADC samples produced from the digital filter. In this design, four samples are skipped for every five samples, which results in an effective sample rate of 3866.8 samples per second for the ADC samples produced from the digital filter. For every sample that is not skipped, it is used for performing metrology calculations.

As an alternative, the modulation clock frequency could be brought down to 5 MHz instead of having to skip samples. However, in this design, this alternative method is not used for reducing the sample rate because the current method would allow a higher output data rate from the delta-sigma modulator + sinc^3 filter. As a result of the higher output data rate of the delta-sigma modulator + sinc^3 filter, at higher input frequencies there would be less attenuation from by the roll-off of the sinc^3 digital filters, thereby leading to more accurate measurement of current THD and RMS current.

In the software, the trigger generator is used to keep track of when to skip samples so the trigger generator has a triggering frequency of 19334 samples per second. Despite having a trigger frequency of 19334, the sample rate for the voltage samples is still 3866.8 because the ADC10_A used for sensing voltages is only re-enabled for conversions one time every five samples.

In the application, the following SD24_B channels associations are used:

- SD0DIO (Converter 0 digital filter) → Current I_A (Current I_A)
- SD1DIO (Converter 1 digital filter) → Current I_B (Current I_B)
- SD2DIO (Converter 2 digital filter) → Current I_C (Current I_C)

3.2.1.2 ADC10_A Setup

The ADC10 is used to sample the three mains voltages and is triggered by the SD24_Bs trigger generator once every five samples. When triggered by the $\Sigma\Delta$, the ADC10 enters autoscan mode and samples six of its channels once. In the software, the clock to the ADC10 is set to 4 MHz. The sample and hold time for each converter is 8 cycles and the conversion time is 12 cycles, which results in an approximate 20-cycle ($\approx 5 \mu\text{s}$) delay between conversion results of adjacent converters. In addition, the ADC10_A uses the 2.0-V reference from the REF module and is configured to output 10-bit results that are scaled to 16-bit twos complement numbers ($\text{ADC10DF} = 1$). This configuration allows the ADC results from the ADC10 to be treated as a 16-bit signed number when performing mathematical operations.

In this application, the following are the relevant ADC10 channel associations:

- A10 (internal channel) → Temperature sensor
- A5 → Voltage V1
- A4 → Voltage V2
- A3 → Voltage V3

3.2.1.3 Real Time Clock (RTC_C)

The RTC_C is a real-time clock module that is configured to give precise one second interrupts. Based off of these one-second interrupts, the time and date are updated in software as necessary.

3.2.1.4 LCD Controller (LCD_C)

The LCD controller on the MSP430F67641 can support up to 8-mux displays and 320 segments. The LCD controller is also equipped with an internal charge pump that can be used for good contrast. In the current design, the LCD controller is configured to work in 4-mux mode using 160 segments with a refresh rate set to $\text{ACLK}/64$, which is 512 Hz.

3.2.1.5 Port Map

The MSP430F67641 has a port mapping controller that allows a flexible mapping of digital functions to port pins. The set of digital functions that can be ported to other pins is dependent on the device. For the MSP430F67641 device in particular, the digital bit-stream inputs for the three SD24_B converters and the delta-sigma modulation clock output are all available options to port to ports P1, P2, and P3. In this design, this porting feature is used to provide flexibility in the PCB layout.

Using the port mapping controller, the following mappings are used:

- SDCLK (SD24_B modulation clock output) → Port P2.6
- SD0DIO (SD24_B Converter 0 digital filter input) → Port P3.1
- SD1DIO (SD24_B Converter 1 digital filter input) → Port P3.0
- SD2DIO (SD24_B Converter 2 digital filter input) → Port P2.7

3.2.1.6 DMA

The direct memory access (DMA) module is used to transfer all of the ADC10 conversion results automatically from the ADC10 to memory. Each time all of the six sampled ADC channels are converted and placed into memory, the DMAIFG flag is set; as a result, this flag can be used to determine the completion of each ADC10 autoscan sequence.

3.2.2 Foreground Process

The foreground process includes the initial setup of the MSP430 hardware and software immediately after a device RESET. Figure 7 shows the flowchart for this process.

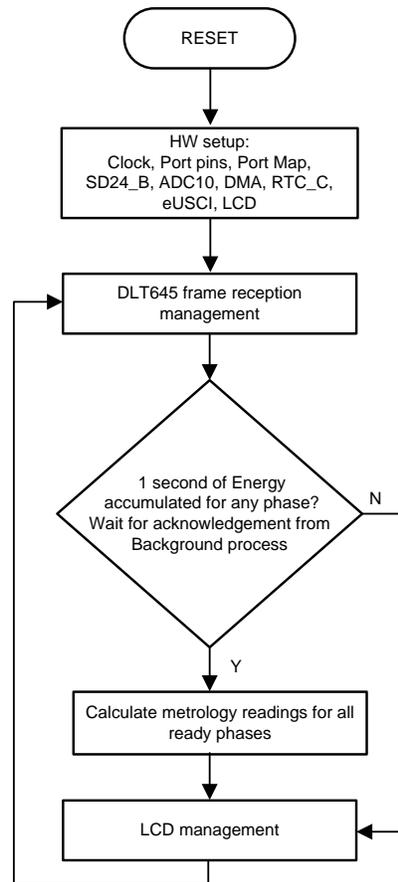


Figure 7. Foreground Process

The initialization routines involve the setup of the SD24_B module; ADC10_A module; DMA; clock system; general purpose input/output (GPIO) port pins and associated port map controller; RTC module for clock functionality; LCD; and the USCI_A0 for UART functionality.

After the hardware is setup, any received frames from the GUI are processed. Subsequently, the foreground process checks whether the background process has notified the foreground process to calculate new metering parameters. This notification is sent through the assertion of the "PHASE_STATUS_NEW_LOG" status flag whenever a frame of data is available for processing. The data frame consists of the processed dot products that were accumulated for one second in the background process. This is equivalent to an accumulation of 50 or 60 cycles of data synchronized to the incoming voltage signal. In addition, a sample counter keeps track of how many samples accumulate over this frame period. This count can vary as the software synchronizes with the incoming mains frequency.

The processed dot products include the V_{RMS} , I_{RMS} , active power, reactive power, fundamental voltage, fundamental active power, and fundamental reactive power. These dot products are used by the foreground process to calculate the corresponding metrology readings in real-world units. Processed voltage and fundamental voltage dot products are accumulated in 48-bit registers. In contrast, processed current dot products, active energy dot products, fundamental active energy dot products, reactive energy dot products, and fundamental reactive energy dot products are accumulated in separate 64-bit registers to further process and obtain the RMS and mean values. Using the foreground's calculated values of

active and reactive power, the apparent power is calculated. Similarly, using the foreground's calculated values for the fundamental voltage, fundamental reactive power, and fundamental active power, the fundamental current, voltage THD, and current THD are calculated. The frequency (in Hertz) and power factor are also calculated using parameters calculated by the background process using the formulas in [Section 3.2.2.1](#).

The foreground process also updates the LCD. The LCD display item is changed every two seconds. See [Section 8.1](#) for more information about the different items displayed on the LCD.

3.2.2.1 Formulae

3.2.2.1.1 Standard Metrology Parameters

This section briefly describes the formulas used for the voltage, current, and energy.

As previous sections describe, voltage and current samples are obtained at a sampling rate of 3866.8 Hz. All of the samples that are taken in one second are kept and used to obtain the RMS values for voltage and current for each phase. The RMS values are obtained by the following formulas:

$$V_{\text{RMS,ph}} = K_{v,\text{ph}} \times \sqrt{\frac{\sum_{n=1}^{\text{Sample count}} v_{\text{ph}}(n) \times v_{\text{ph}}(n)}{\text{Sample count}} - v_{\text{offset,ph}}} \quad (2)$$

$$I_{\text{RMS,ph}} = K_{i,\text{ph}} \times \sqrt{\frac{\sum_{n=1}^{\text{Sample count}} i_{\text{ph}}(n) \times i_{\text{ph}}(n)}{\text{Sample count}} - i_{\text{offset,ph}}} \quad (3)$$

where

- ph = Phase parameters that are being calculated [that is, Phase A(=1), B(=2), or C(=3)]
- $V_{\text{ph}}(n)$ = ADC sample from the ph phases voltage channel, taken at sample instant n
- $V_{\text{offset,ph}}$ = Offset used to subtract effects of the additive white Gaussian noise from the voltage converter
- $i_{\text{ph}}(n)$ = ADC sample from the ph phases current channel, taken at sample instant n
- $i_{\text{offset,ph}}$ = Offset used to subtract effects of the additive white Gaussian noise from the current converter
- Sample count = Number of samples in one second
- $K_{v,\text{ph}}$ = Scaling factor for voltage
- $K_{i,\text{ph}}$ = Scaling factor for each current

Power and energy are calculated for a frames worth of active and reactive energy samples. These samples are phase corrected and passed on to the foreground process, which uses the number of samples (sample count) to calculate phase active and reactive powers through the following formulas:

$$P_{ACT,ph} = K_{ACT,ph} \frac{\sum_{n=1}^{\text{Sample count}} v(n) \times i_{ph}(n)}{\text{Sample count}} \quad (4)$$

$$P_{REACT,ph} = K_{REACT,ph} \frac{\sum_{n=1}^{\text{Sample count}} v_{90}(n) \times i_{ph}(n)}{\text{Sample count}} \quad (5)$$

$$P_{APP,ph}^2 = \sqrt{P_{ACT,ph}^2 + P_{REACT,ph}^2} \quad (6)$$

where

- $V_{90_ph}(n)$ = Voltage sample of the waveform that results from shifting $v_{ph}(n)$ by 90° , taken at a sample instant n
- $K_{ACT,ph}$ = Scaling factor for active power
- $K_{REACT,ph}$ = Scaling factor for reactive power

Please note that for reactive energy, the 90° phase shift approach is used for two reasons:

1. This approach allows accurate measurement of the reactive power for very small currents.
2. This approach conforms to the measurement method specified by IEC and ANSI standards.

The calculated mains frequency is used to calculate the 90 degrees-shifted voltage sample. Because the frequency of the mains varies, it is important to first measure the mains frequency accurately to phase shift the voltage samples accordingly (see [Section 3.2.3.1.4](#) for details).

To get an exact 90° phase shift, interpolation is used between two samples. For these two samples, a voltage sample slightly more than 90° before the current sample is used and a voltage sample slightly less than 90° before the current sample is used. The application's phase shift implementation consists of an integer part and a fractional part. The integer part is realized by providing an N samples delay. The fractional part is realized by a one-tap FIR filter. In the software, a lookup table provides the filter coefficients that are used to create the fractional delays.

In addition to calculating the per-phase active and reactive powers, the cumulative sum of these parameters are also calculated by the below equations:

$$P_{ACT,Cumulative} = \sum_{ph=1}^3 P_{ACT,ph} \quad (7)$$

$$P_{REACT,Cumulative} = \sum_{ph=1}^3 P_{REACT,ph} \quad (8)$$

$$P_{APP,Cumulative} = \sum_{ph=1}^3 P_{APP,ph} \quad (9)$$

Using the calculated powers, energies are calculated by the following formulas in [Equation 10](#):

$$\begin{aligned} E_{ACT,ph} &= P_{ACT,ph} \times \text{Samplecount} \\ E_{REACT,ph} &= P_{REACT,ph} \times \text{Samplecount} \\ E_{APP,ph} &= P_{APP,ph} \times \text{Samplecount} \end{aligned} \quad (10)$$

From there, the energies are also accumulated to calculate the cumulative energies, by the following [Equation 11](#), [Equation 12](#), and [Equation 13](#):

$$E_{ACT,Cumulative} = \sum_{ph=1}^3 E_{ACT,ph} \quad (11)$$

$$E_{REACT,Cumulative} = \sum_{ph=1}^3 E_{REACT,ph} \quad (12)$$

$$E_{APP,Cumulative} = \sum_{ph=1}^3 E_{APP,ph} \quad (13)$$

The calculated energies are then accumulated into buffers that store the total amount of energy consumed since system reset. Note that these energies are different from the working variables used to accumulate energy for outputting energy pulses. There are four sets of buffers that are available: one for each phase and one for the cumulative of the phases. Within each set of buffers, the following energies are accumulated:

1. Active import energy (active energy when active energy ≥ 0)
2. Active export energy (active energy when active energy < 0)
3. React. Quad I energy (reactive energy when reactive energy ≥ 0 and active power ≥ 0 ; inductive load)
4. React. Quad II energy (reactive energy when reactive energy ≥ 0 and active power < 0 ; capacitive generator)
5. React. Quad III energy (reactive energy when reactive energy < 0 and active power < 0 ; inductive generator)
6. React. Quad IV energy (reactive energy when reactive energy < 0 and active power ≥ 0 ; capacitive load)
7. App. import energy (apparent energy when active energy ≥ 0)
8. App. export energy (apparent energy when active energy < 0)

The background process also calculates the frequency in terms of samples per mains cycle. The foreground process then converts this samples per mains cycle to Hertz by the following formula in [Equation 14](#):

$$\text{Frequency (Hz)} = \frac{\text{Sample Rate (samples / second)}}{\text{Frequency (samples / cycle)}} \quad (14)$$

After the active power and apparent power have been calculated, the absolute value of the power factor is calculated. In the system's internal representation of power factor, a positive power factor corresponds to a capacitive load; a negative power factor corresponds to an inductive load. The sign of the internal representation of power factor is determined by whether the current leads or lags voltage, which is determined in the background process. Therefore, the internal representation of power factor is calculated by the following formula:

$$\text{Internal Representation of Power Factor} = \begin{cases} \frac{P_{Act}}{P_{Apparent}}, & \text{if capacitive load} \\ -\frac{P_{Act}}{P_{Apparent}}, & \text{if inductive load} \end{cases} \quad (15)$$

3.2.2.1.2 Power Quality Formulas

To calculate the fundamental RMS voltage, a pure sine wave is generated and tightly locked to the fundamental of the incoming voltage waveform. Using the generated waveform, the fundamental voltage, fundamental active power, and fundamental reactive power are calculated by the following equations:

$$V_{\text{fund,ph}} = K_{V_fund,ph} \frac{\sum_{n=1}^{\text{Sample count}} v_{\text{pure,ph}}(n) \times v_{\text{ph}}(n)}{\text{Sample count}} \quad (16)$$

$$P_{\text{ACT_fund,ph}} = K_{\text{ACT_fund,ph}} \frac{\sum_{n=1}^{\text{Sample count}} v_{\text{pure,ph}}(n) \times i_{\text{ph}}(n)}{\text{Sample count}} \quad (17)$$

$$P_{\text{REACT_fund,ph}} = K_{\text{REACT_fund,ph}} \frac{\sum_{n=1}^{\text{Sample count}} v_{90_pure,ph}(n) \times i_{\text{ph}}(n)}{\text{Sample count}} \quad (18)$$

where

- $v_{\text{pure,ph}}(n)$ = Voltage sample of the pure sine wave generated, taken at a sample instant n
- $v_{90_pure,ph}(n)$ = Voltage sample of the waveform that results from shifting $v_{\text{pure,ph}}(n)$ by 90° , taken at a sample instant n
- $K_{V_fund,ph}$ = Scaling factor for fundamental voltage
- $K_{\text{ACT_fund,ph}}$ = Scaling factor for fundamental active power
- $K_{\text{REACT_fund,ph}}$ = Scaling factor for fundamental active power

After calculating the fundamental voltage, fundamental active power, and fundamental reactive power, the fundamental current is calculated by the following formula:

$$I_{\text{fund,ph}} = K_{i_fund,ph} * \frac{\sqrt{P_{\text{ACT_fund,ph}}^2 + P_{\text{REACT_fund,ph}}^2}}{V_{\text{fund,ph}}} \quad (19)$$

where $K_{i_fund,ph}$ = Scaling factor for fundamental current.

Once the fundamental current and fundamental voltage are calculated, the voltage THD and current THD can also be calculated. This software supports three different methods of calculating THD that are referred to as THDIEC_F, THDIEC_R, and THDIEEE. Use the following formulas to calculate voltage THD(V_THD) and current THD(I_THD) with these different methods:

$$V_THD_{\text{IEC_F,ph}} = \frac{\sqrt{V_{\text{RMS,ph}}^2 - V_{\text{fund,ph}}^2}}{V_{\text{fund,ph}}} \quad I_THD_{\text{IEC_F,ph}} = \frac{\sqrt{I_{\text{RMS,ph}}^2 - I_{\text{fund,ph}}^2}}{I_{\text{fund,ph}}} \quad (20)$$

$$V_THD_{\text{IEC_R,ph}} = \frac{\sqrt{V_{\text{RMS,ph}}^2 - V_{\text{fund,ph}}^2}}{V_{\text{RMS,ph}}} \quad I_THD_{\text{IEC_R,ph}} = \frac{\sqrt{I_{\text{RMS,ph}}^2 - I_{\text{fund,ph}}^2}}{I_{\text{RMS,ph}}} \quad (21)$$

$$V_THD_{\text{IEEE,ph}} = \frac{V_{\text{RMS,ph}}^2 - V_{\text{fund,ph}}^2}{V_{\text{fund,ph}}^2} \quad I_THD_{\text{IEEE,ph}} = \frac{I_{\text{RMS,ph}}^2 - I_{\text{fund,ph}}^2}{I_{\text{fund,ph}}^2} \quad (22)$$

To calculate THD correctly, select the proper method of THD calculation by defining the proper macro in the metrology-template.h file. Ensure that any reference meter used to measure THD uses the same THD method as the method selected in software. [Table 2](#) shows the different settings needed to select between the different methods of calculating THD.

Table 2. Macro Settings to Select THD Calculation Methods

THD METHOD	MACRO SETTINGS IN METROLOGY-TEMPLATE.H FILE
THD _{IEC_R}	Define "IEC_THD_R_SUPPORT" macro and undefine "IEC_THD_F_SUPPORT" macro
THD _{IEC_F}	Undefine "IEC_THD_R_SUPPORT" macro and define "IEC_THD_F_SUPPORT" macro
THD _{IEEE}	Undefine "IEC_THD_R_SUPPORT" macro and undefine "IEC_THD_F_SUPPORT" macro

3.2.3 Background Process

[Figure 8](#) shows the background process, which mainly deals with timing critical events in software. The background process uses the SD24_B trigger generation to collect voltage and current samples. The SD24_B provides a trigger 19334 times per second. For a certain number of these triggers, sample processing is done on the previously obtained voltage and current samples. This sample processing is done by the "per_sample_dsp ()" function. After sample processing, the background process uses the "per_sample_energy_pulse_processing ()" for the calculation and output of energy-proportional pulses. In the software, the "SAMPLES_SKIPPED" macro determines how many triggers to skip between successive calculations. Because the default value of this macro is 4, sample processing and energy pulse processing is done once every five SD24_B triggers. As a result, four out of five current samples are skipped and not used for calculations, which leads to an effective sample rate of 3866.8 samples per second for the current channels.

To keep track of when to skip samples, the "sample_number" variable is used to keep track of how many trigger pulses have been produced since the last time sample and energy pulse processing has occurred. Due to the high frequency of triggers, triggers may occur in the middle of sample processing within the SD24_B ISR. Because interrupts are disabled within the ISR, the trigger pulse flag (SD24TRGIFG) is checked in various places within the ISR code to keep track of triggers that occur during the SD24_B interrupt. These checks are done by calling the "update_sample_count()" function ([Figure 9](#)). The places where the update_sample_count is called are set so that the time between checks is less than the period of the triggers.

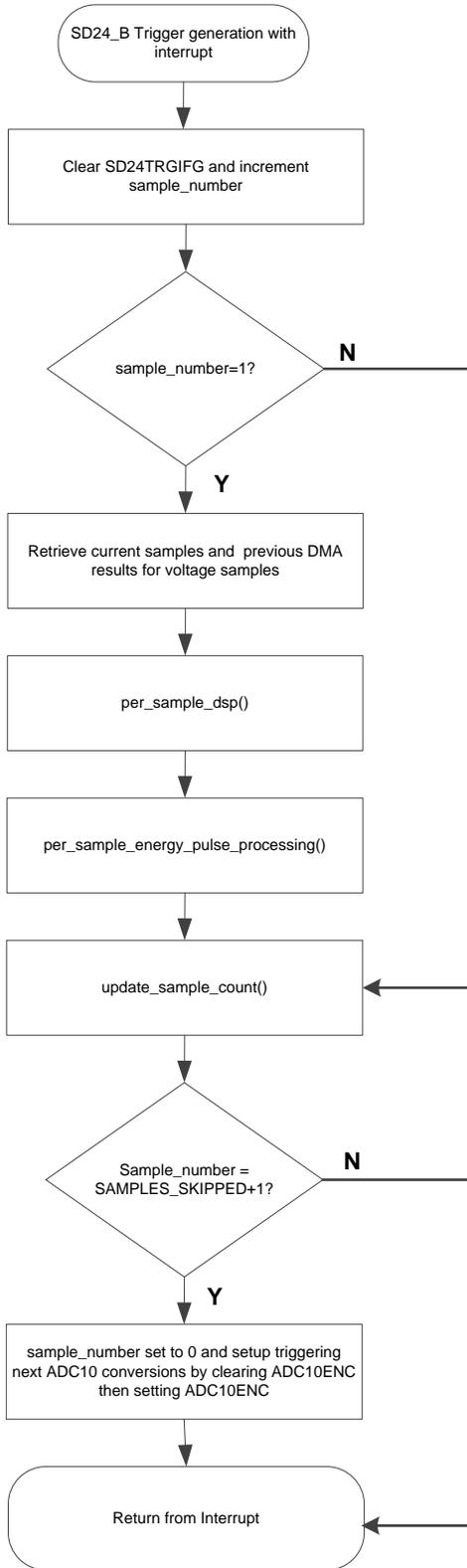


Figure 8. Background Process

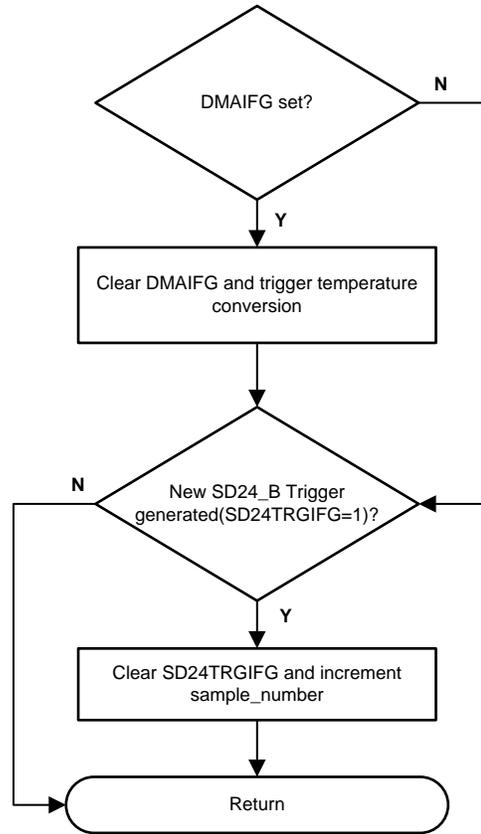


Figure 9. update_sample_count ()

Similar to the current samples, the sample rate for voltage samples is also 3866.8 samples per second; however, unlike the current samples, this sample rate is not achieved by skipping samples. Instead, the sample rate is caused by only re-enabling the ADC10 for conversions to measure the phase voltage channels only once every SAMPLES_SKIPPED+1 samples. Re-enabling the ADC10 for conversions is accomplished by clearing and then setting the ADC10ENC bit. As Figure 8 shows, this clearing and setting is done when the sample_number = (SAMPLES_SKIPPED+1). As a result, the ADC10 converts the voltage samples in parallel to the sample processing done in the background process. Figure 10 shows this parallel activity. In Figure 10, the shaded containers represent items that are automatically done by the configuration of the ADC10, DMA, and $\Sigma\Delta$ modules. For these shaded items, CPU intervention is not required.

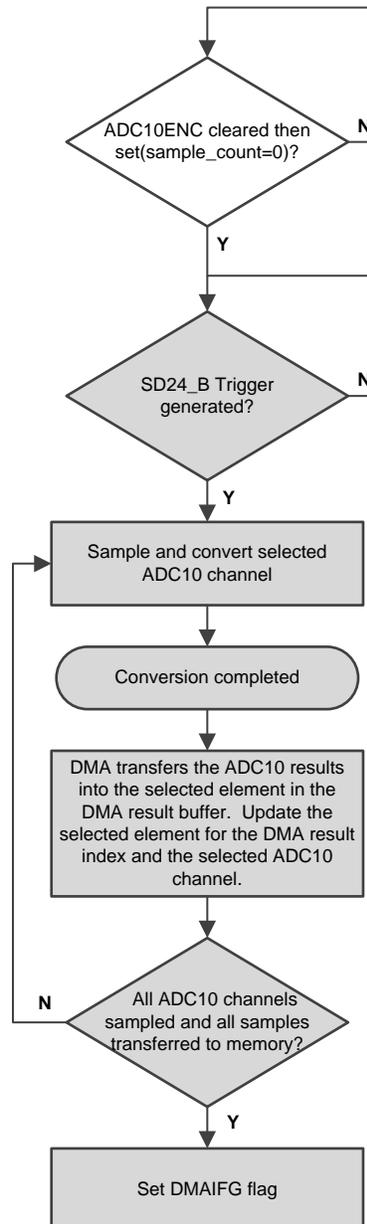


Figure 10. ADC10 Triggering Process

As Figure 10 represents, whenever the ADC10 is triggered, the ADC10 enters autoscan mode and samples six ADC channels once. After each channel has a conversion result, the DMA automatically places these results in memory and the next channels conversion is automatically started. For each converter, there is a memory location that stores the conversion results for that particular converter. The procedure of sampling a converter and storing the results in memory is repeated until the last converter (ADC10INCH = 0) is sampled. Because the clock to the ADC10 is set to 4 MHz, the sample and hold time for each converter is 8 cycles, and the conversion time is 12 cycles, there is an approximate 20-cycle (approximately 5- μ s) delay between the conversion results of adjacent converters.

Once all of the ADC10 channels are sampled and the samples are transferred to memory, the DMAIFG flag is set to indicate that the ADC10 has completed its operation and may be used for other conversions.

To sense the internal temperature sensor using the ADC10, a recommended sample period of at least 30 μ s must be used. As a result, the autoscan mode that is used to measure the phase voltages cannot be extended to also measure the temperature channel. To mitigate this loss of temperature channel measurement, a single conversion of the ADC10 temperature channel is triggered (see Figure 11). The temperature conversion is triggered when the DMAIFG flag is asserted (see Figure 10) to indicate that the phase voltages have just been completely converted and transferred to memory so that other conversions can be started. The check for the completion of the phase voltage sampling is done within the update_sample_count function (see Figure 9). Because the update_sample_count function is called multiple times within the SD24_B interrupt, this ensures that the temperature conversion can be started relatively quickly. After a temperature reading has been received and its associated ISR has been called, temperature reading is stored in memory and the ADC10 settings are then reset to support autoscan mode for the next conversion.

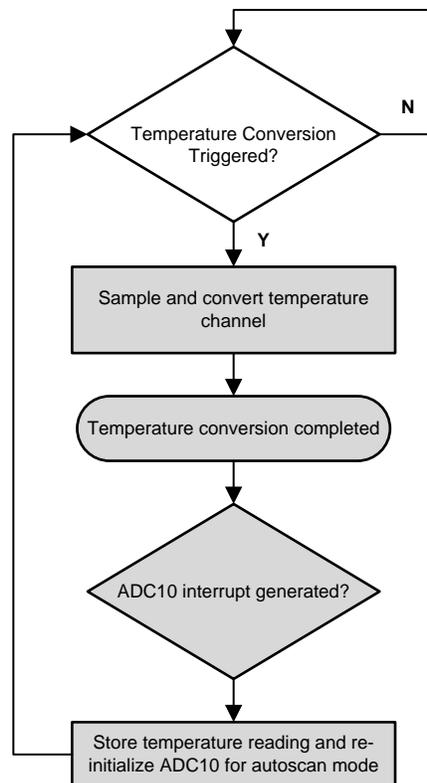


Figure 11. Temperature Triggering Mechanism

3.2.3.1 *per_sample_dsp()*

Figure 12 shows the flowchart for the `per_sample_dsp()` function. The `per_sample_dsp` function is used to calculate intermediate dot product results that are fed into the foreground process for the calculation of metrology readings. The ADC10 is configured to represent the 10-bit voltage results as a 16-bit signed result. Because 16-bit voltage samples are used, the voltage samples and fundamental voltage samples are further processed and accumulated in dedicated 48-bit registers. In contrast, since 24-bit current samples are used, the current samples are processed and accumulated in dedicated 64-bit registers. Per-phase active power, fundamental active power, fundamental reactive power, and reactive power are also accumulated in 64-bit registers.

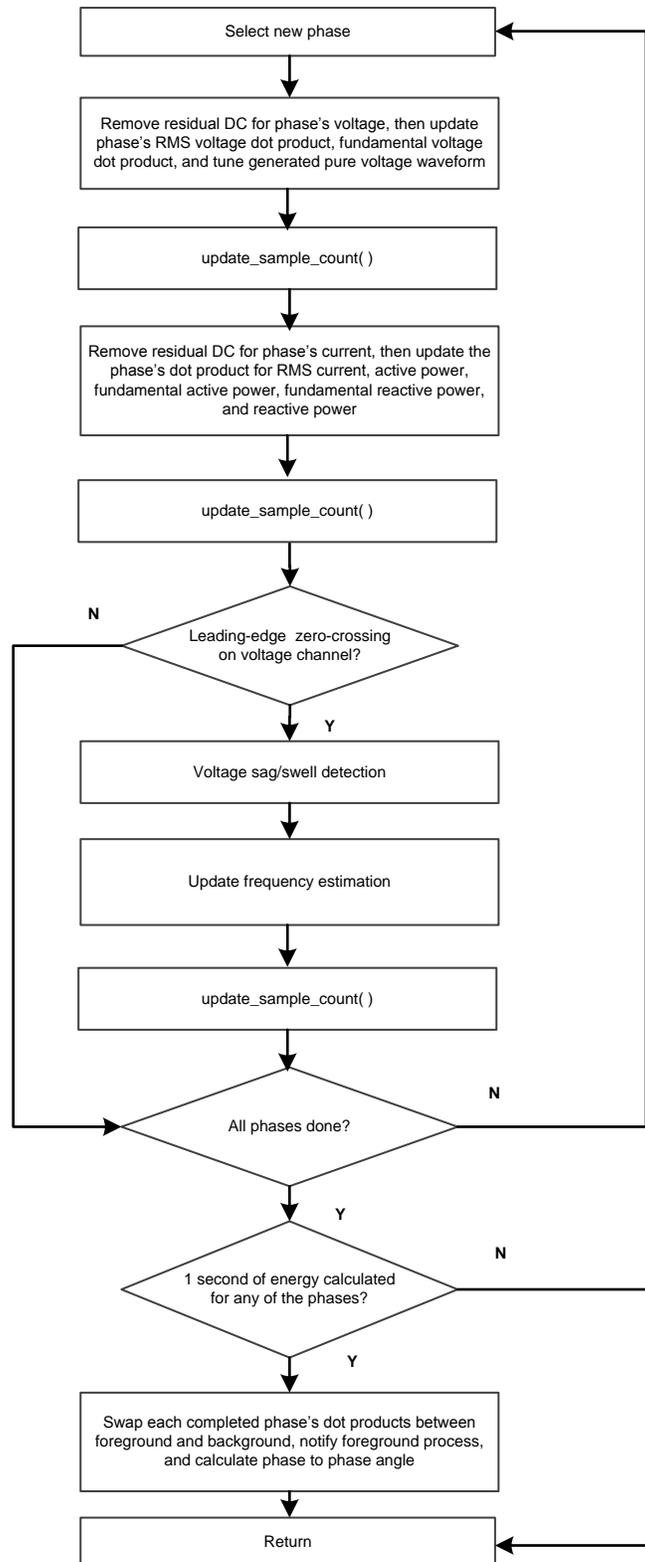


Figure 12. per_sample_dsp()

After sufficient samples (approximately one second's worth) have been accumulated, the background process triggers the foreground function to calculate the final values of RMS voltage; RMS current; active, reactive, and apparent powers; active, reactive, and apparent energy; frequency; power factor; fundamental voltage, fundamental current, fundamental active power, and fundamental reactive power; and voltage THD and current THD. In the software, there are two sets of dot products: at any given time, one is used by the foreground for calculation and the other used as the working set by the background. After the background process has sufficient samples, it swaps the two dot products so that the foreground uses the newly acquired dot products that the background process just calculated and the background process uses a new empty set to calculate the next set of dot products. In addition, after swapping the dot products for a particular phase, the angle between the previous phase voltage to that particular phase voltage is calculated.

Whenever there is a leading-edge zero-crossing (- to + voltage transition) on a voltage channel, the `per_sample_dsp()` function is also responsible for updating the corresponding phase's frequency (in samples per cycle) and voltage sag and swell conditions. For the sag and swell conditions, the RMS voltage is monitored over a rolling window of a certain number of mains cycles (this user-defined number of mains cycles is defined by the `SAG_SWELL_WINDOW_LEN` macro in the `metrology-template.h` file). Whenever the RMS voltage that is calculated over the duration of the current sag and swell window is less than the system's nominal voltage (as defined by the `MAINS_NOMINAL_VOLTAGE` macro in `metrology-template`) by a percentage larger than the sag threshold macro (defined as `SAG_THRESHOLD` in `metrology-template`), a sag event is defined as occurring. The number of mains cycles where this condition persists is logged as the sag duration and the number of sag condition occurrences is logged as the sag events count. Note that the sag duration corresponds to the total number of cycles in a sag condition since being reset and is therefore not cleared for every sag event. Similarly, for the case the measured RMS voltage is greater than the nominal voltage by a percentage larger than the swell threshold (defined as `SWELL_THRESHOLD` in `metrology-template.h`), a swell event is defined as occurring and the number of mains cycles where this condition persists is logged as the swell duration.

The following subsections describe the various elements of electricity measurement.

3.2.3.1.1 Voltage and Current Signals

The output of each `SD24_B` digital filter and `ADC10` converter is a signed integer and any stray DC or offset value on these converters are removed using a DC tracking filter. Separate DC estimates for all voltages and currents are obtained using the filter and voltage and current samples, respectively. These estimates are then subtracted from each voltage and current sample. The resulting instantaneous voltage and current samples are used to generate the following intermediate dot product results:

- Accumulated squared values of voltages and currents, which is used for V_{RMS} and I_{RMS} calculations, respectively.
- Accumulated energy samples to calculate active energies.
- Accumulated energy samples using current and 90° phase shifted voltage to calculate reactive energies.

These accumulated values are processed by the foreground process.

3.2.3.1.2 Pure Waveform Samples

To calculate the fundamental and THD readings, the software generates a pure sinusoid waveform for each phase and locks it to the fundamental of the incoming voltage waveform for that particular phase. Since the generated waveform is locked to the fundamental of the incoming voltage, the correlation of this pure waveform with the waveform from the voltage ADC can be used to find the amplitude of the fundamental component of the waveform sensed by the voltage ADC. Similarly, the correlation of the current and the pure voltage waveform can be used to calculate the fundamental active power. For fundamental reactive power, the correlation of the 90° shifted pure waveform and the current can be used for calculating this parameter.

To generate a sine wave, information on the amplitude, phase, and frequency of the desired waveform is necessary. For the generated pure waveform, the amplitude is set to full scale to maximize the value of the fundamental dot products, the frequency is set to the measured frequency (in units of cycles/sample) that is used to calculate the mains frequency in final real-world units of Hertz, and the phase of the generated waveform is iteratively adjusted so that it is locked to the phase of the fundamental voltage. After the frequency is correctly calculated and the generated waveform's phase is locked to the fundamental voltage's phase, the fundamental readings can then be correctly calculated.

3.2.3.1.3 Phase-to-Phase Angle Readings

The samples of the generated pure sine waves are obtained by indexing into a lookup table of sine wave samples. In the software, there is one lookup table but each phase has a different index into that same lookup table. Based on the value of the lookup table indexes of the different phases, the angle between the different fundamental voltage waveforms can be calculated. In the firmware, the phase-to-phase angle between a phase's voltage waveform and the previous phase's voltage waveform is calculated (that is, ϕ_{13} , ϕ_{21} , and ϕ_{32}). This phase-to-phase angle variable is internally represented in the firmware as a signed integer and is in units of $\frac{180^\circ}{2^{15}}$.

Based on the expected value of the phase-to-phase angle readings, it can be determined whether an incorrect phase sequence is being registered by a meter by comparing the expected values of the phase-to-phase readings to the actual measured value. As an example, if ϕ_{13} , ϕ_{21} , and ϕ_{33} are all expected to be 240° but are reading 120°, this may indicate that two of the voltage connections have been accidentally swapped.

3.2.3.1.4 Frequency Measurement and Cycle Tracking

The instantaneous voltage of each phase is accumulated in 48-bit registers. In contrast, the instantaneous currents, active powers, and reactive powers are accumulated in 64-bit registers. A cycle tracking counter and sample counter keep track of the number of samples accumulated. When approximately one second worth of samples has been accumulated, the background process switches the foreground and background and then notifies the foreground process to produce the average results such as RMS and power values. Cycle boundaries are used to trigger the foreground averaging process because this process produces very stable results.

For frequency measurements, a straight-line interpolation is used between the zero-crossing voltage samples. Figure 13 shows the samples near a zero cross and the process of linear interpolation.

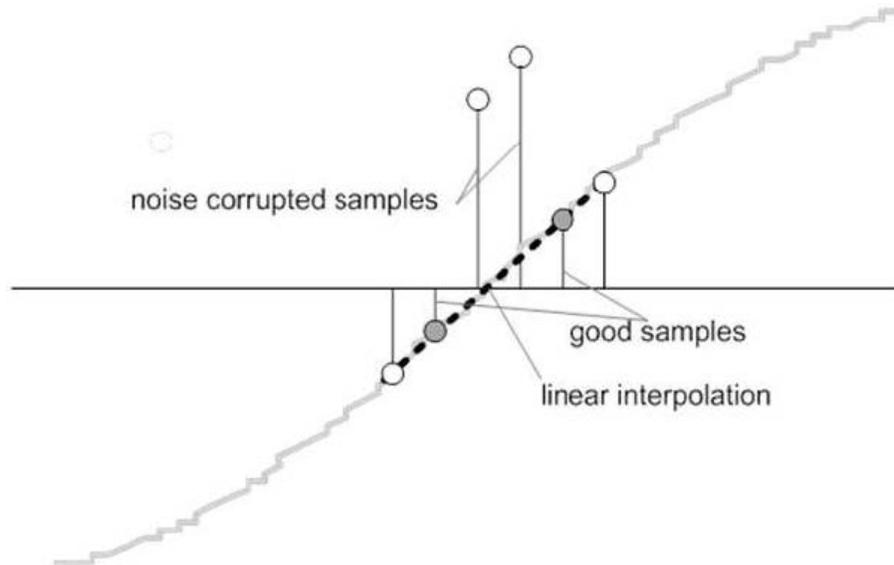


Figure 13. Frequency Measurement

Because noise spikes can also cause errors, the application uses a rate of change check to filter out the possible erroneous signals and make sure that the two points that are interpolated are from genuine zero crossing points. For example, with two negative samples, a noise spike can make one of the samples positive, thereby making the negative and positive pair look as if there is a zero crossing. The resultant cycle-to-cycle timing goes through a weak low-pass filter to further smooth out cycle-to-cycle variations. This filtering results in a stable and accurate frequency measurement that is tolerant of noise.

3.2.3.2 LED Pulse Generation (*per_sample_energy_pulse_processing*)

In electricity meters, the active energy consumed is normally measured in a fraction of kilowatt-hour (kWh) pulses. This information can be used to calibrate any meter for accurate measurement. Typically, the measuring element (the MSP430 microcontroller) is responsible for generating pulses proportional to the energy consumed. To serve both these tasks efficiently, pulse generation must be accurate with relatively little jitter. Although time jitters are not an indication of bad accuracy, they give a negative indication of the overall accuracy of the meter, which is why the jitter is averaged out.

This application uses average power to generate these energy pulses. The average power (calculated by the foreground process) accumulates every time the *per_sample_energy_pulse_processing* is called, thereby spreading the accumulated energy from the previous one second time frame evenly for each interrupt in the current one second time frame. This process is equivalent to converting it to energy. When the accumulated energy crosses a threshold, a pulse is generated. The amount of energy above this threshold is kept and a new energy value is added on top of it in the next interrupt cycle. Because the average power tends to be a stable value, this way of generating energy pulses is very steady and free of jitter.

The threshold determines the energy "tick" specified by meter manufacturers and is a constant. The "tick" is usually defined in pulses per kWh or just in kWh. One pulse is generated for every energy "tick". For example, in this application, the number of pulses generated per kWh is set to 6400 for active and reactive energies. The energy "tick" in this case is 1 kWh/6400. Energy pulses are generated and available on a header and also through light-emitting diodes (LEDs) on the board. GPIO (port) pins are used to produce the pulses.

In the design, the LED that is labeled "Active" corresponds to the active energy consumption for the cumulative three-phase sum, respectively. "Reactive" corresponds to the cumulative three-phase reactive energy sum. The number of pulses per kWh and each pulse duration can be configured in the software. [Figure 14](#) shows the flow diagram for pulse generation. This flow diagram is valid for pulse generation of accumulative active and reactive energy.

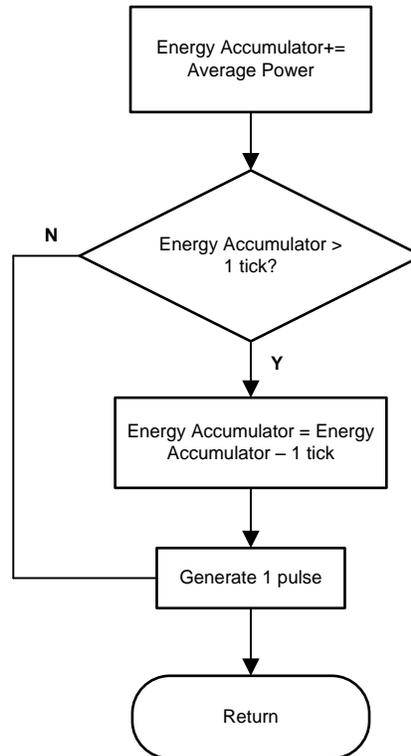


Figure 14. Pulse Generation for Energy Indication

The average power is in units of 0.001 W and the 1-kWh threshold is defined as:
 1 kWh threshold = $(1 / 0.001) \times 1 \text{ kW} \times (\text{number of interrupts per second}) \times (\text{number of seconds in one hour}) = 1000000 \times 3866.8 \times 3600 = 0x\text{CA91D43F800}$

3.2.3.3 Phase Compensation

In order to ensure accurate measurements, the relative phase shift between voltage and current samples must be compensated. This phase shift may be caused by the passive components of the voltage and current input circuit or even the sequential sampling on the voltage channel.

The implementation of the phase shift compensation consists of an integer part and a fractional part. The integer part is realized by providing an N-sample delay. The fractional part is realized by a one-tap finite impulse response (FIR) filter that interpolates between two samples, similar to the FIR filter used for providing 90°-shifted voltage samples for reactive energy measurements. In the software, a lookup table provides the filter coefficients that are used to create the fractional delays. The lookup table provides fractional phase shifts as small as 1/256th of a sample. The 3866.8 sample rate used in this application corresponds to a 0.0182° degree resolution at 50 Hz. In addition to the filter coefficients, the lookup table also has an associated gain variable for each set of filter coefficients. This gain variable is used to cancel out the resulting gain from using a certain set of filter coefficients.

4 Block Diagram

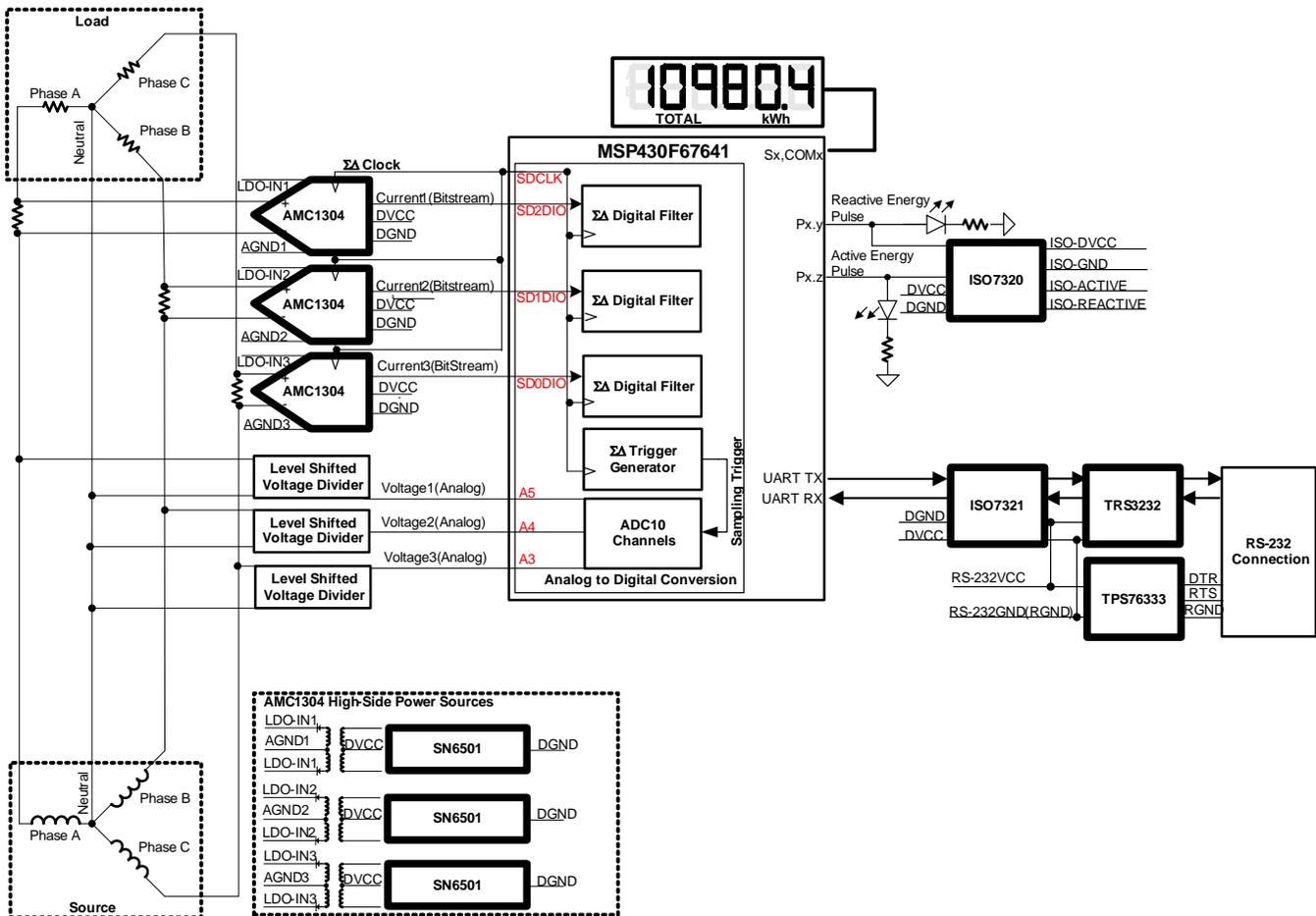


Figure 15. System Block Diagram

Figure 15 depicts a block diagram that shows the high-level interface used for an MSP430F67641-based three-phase energy measurement application with isolated shunts. Figure 15 shows a three-phase, four-wire star connection to the AC mains in this case. In this design, each phase has a shunt current sensor and an AMC1304 device for measuring the voltage across the shunt current sensor. The resistance of the shunt is selected based on the current range required for energy measurements and also the minimization of the maximum power dissipation of the shunt.

For powering the high-side of the AMC1304, each AMC1304 has an external isolated power supply. Please note that because each high-side of the AMC1304s must be referenced from a different line voltage, three isolated power supplies are used. Each implemented power supply provides power to the associated AMC1304 by using DVCC, a transformer, and the SN6501 transformer driver. In contrast, for powering the controller-side of the AMC1304 chips, all AMC1304s must be powered from the same source that powers the MSP430F67641 device.

To perform conversions, all AMC1304 chips must have the same external clock fed into them. In this design, the SD24_B module outputs its modulation clock, which is generated internally within the MSP430F67641, and feeds the modulation clock to all of the AMC1304 chips. The AMC1304 chips then output their corresponding bit-streams, which are isolated from the high-side part of the chips. Each of these bit-streams is fed into a different MSP430F67641 converters bit-stream input.

For the voltage sensor, a combination of a voltage divider and level shifter are used to ensure that the input voltage to the ADC fits within the single-ended voltage range of operation. The range of operation is determined by the chosen reference voltage source of the SAR ADCs. The choice of voltage divider resistors for the voltage channel is selected to ensure the mains voltage is divided down to the normal input ranges that are valid for the SAR ADC, based on the selected reference voltage. To synchronize the SAR ADCs with the SD24_B module, the trigger generator within the SD24_B triggers the ADC10 to ensure that the timing between the ADC10 and SD24_B modules are grouped and synchronized.

Other signals of interest in [Figure 15](#) are the active and reactive energy pulses used for accuracy measurement and calibration. The ISO7320 provides an isolated connection for these pulses for connecting to non-isolated equipment. In addition to isolated pulses, the design supports isolated RS-232 communication through the use of the TPS76333, ISO7321, and TRS3232 devices. For more information on the isolated RS-232 portion of the design, consult the following resource: <http://www.ti.com/tool/TIDA-00163>.

4.1 Highlighted Products

4.1.1 AMC1304M05

The AMC1304 devices are precision, delta-sigma ($\Delta\Sigma$) modulators with the output separated from the input circuitry by a capacitive isolation barrier that is highly resistant to magnetic interference. This barrier is certified to provide reinforced isolation of up to 7000 V_{PEAK} according to the UL 1577 standard, VDE V-0884-10 standards, and also a working insulation voltage over the life of the part of up to 1.0-kV AC_{RMS}. On the high-side of the AMC1304, the modulator is supplied with an integrated LDO regulator that allows an unregulated voltage between 4 and 18 V to power the high side of the chip.

4.1.2 SN6501

The SN6501 is a monolithic oscillator/power-driver, specifically designed for small-form factor, isolated power supplies in isolated interface applications. The device drives a low-profile, center-tapped transformer primary from a 3.3-V or 5-V DC power supply. The secondary can be wound to provide any isolated voltage based on the transformer turns ratio.

The SN6501 consists of an oscillator followed by a gate drive circuit that provides the complementary output signals to drive the ground-referenced N-channel power switches. The internal logic ensures break-before-make action between the two switches.

4.1.3 MSP430F67641

The MSP430F67641 poly-phase metering SoC is a powerful, highly-integrated energy measurement solution that offers accuracy and low system cost with few external components. The F67641 uses the low-power MSP430™ CPU with a 32-bit multiplier to perform all energy calculations, metering applications such as tariff rate management, and communications with automatic meter reading (AMR) or advanced metering infrastructure (AMI) modules. The chip has an LCD controller with support for up to 320 segments, a real-time clock (RTC) module with integrated offset and temperature calibration, and a separate auxiliary supply to power the RTC independently from the rest of the chip. Figure 16 shows these features as well as additional ones for the MSP430F67641 SoC.

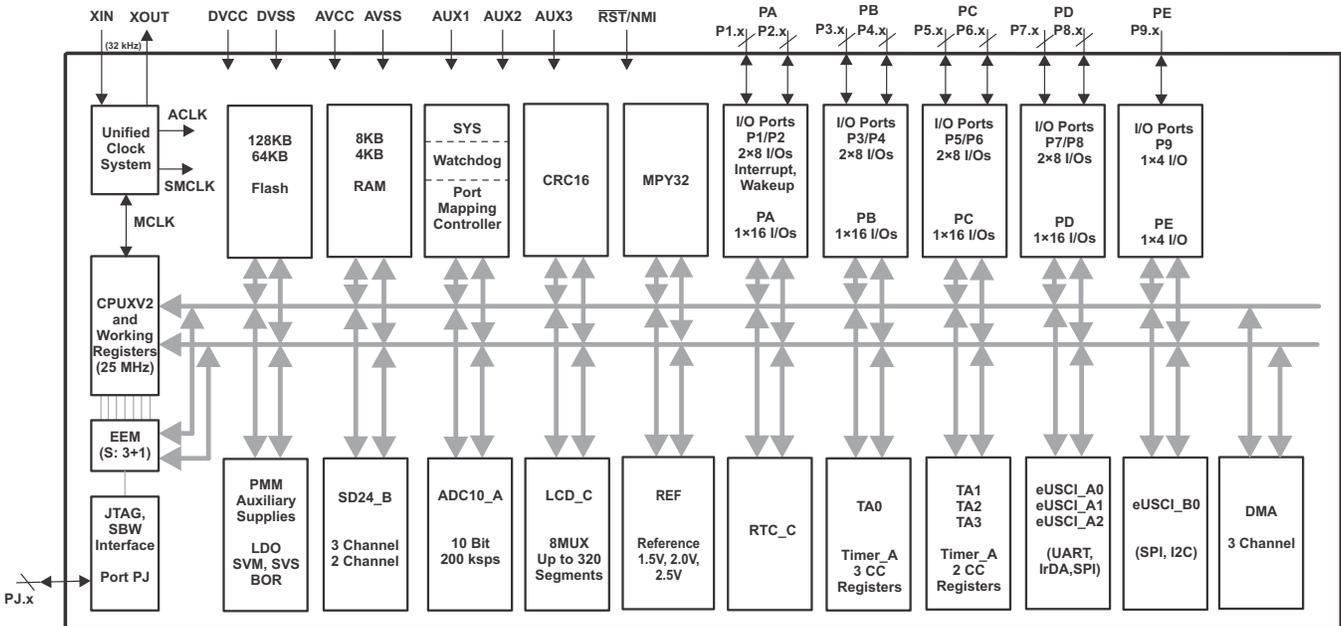


Figure 16. MSP430F67641 Block Diagram

4.1.4 TRS3232

The TRS3232 device consists of two line drivers, two line receivers, and a dual charge-pump circuit with ± 15 -kV electrostatic discharge (ESD) protection pin-to-pin (serial-port connection pins, including GND). The device meets the requirements of the Telecommunications Industry Association and Electronic Industries Alliance TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3- to 5.5-V supply. The devices operate at data signaling rates up to 250 kbit/s and a maximum of 30-V/ μ s driver output slew rate.

4.1.5 ISO7321

The ISO7321 provides galvanic isolation up to 3 kV_{RMS} for one minute per UL. This digital isolator has two isolated channels where one is a forward channel and the other is a reverse channel. Each isolation channel has a logic input and output buffer separated by a silicon dioxide (SiO₂) insulation barrier. This chip supports a signaling rate of 25 Mbps. The chips can operate from 3.3- and 5-V supply and logic levels. At the rated voltage, the ISO7321 has over a 25-year isolation integrity.

4.1.6 TPS76333

The TPS763xx family of LDO voltage regulators offers the benefits of low dropout voltage, low power operation, and miniaturized packaging. These regulators feature low dropout voltages and quiescent currents compared to conventional LDO regulators. A combination of new circuit design and process innovation has enabled the usual PNP pass transistor to be replaced by a PMOS pass element. Because the PMOS pass element functions as a low-value resistor, the dropout voltage is very low—typically 300 mV at 150 mA of load current (for the TPS76333)—and is directly proportional to the load current. Because the PMOS pass element is a voltage-driven device, the quiescent current is very low (140- μ A maximum) and is stable over the entire range of output load current (0 mA to 150 mA). The TPS763xx also features a logic-enabled sleep mode to shut down the regulator, reducing quiescent current to a 1- μ A maximum at $T_j = 25^\circ\text{C}$.

4.1.7 ISO7320

The ISO7320 provides galvanic isolation up to 3 kV_{RMS} for 1 minute per UL. This digital isolator has two isolated forward channels. Each isolation channel has a logic input and output buffer separated by a silicon dioxide (SiO₂) insulation barrier. This chip supports a signaling rate of 25 Mbps. The chips can operate from 3.3- and 5-V supply and logic levels. At the rated voltage, the ISO7320 device has over a 25-year isolation integrity.

5 Getting Started Hardware

The following figures of the EVM best describe the hardware: [Figure 17](#) is the top view of the energy measurement system and [Figure 18](#) shows the location of various pieces of the EVM based on functionality.

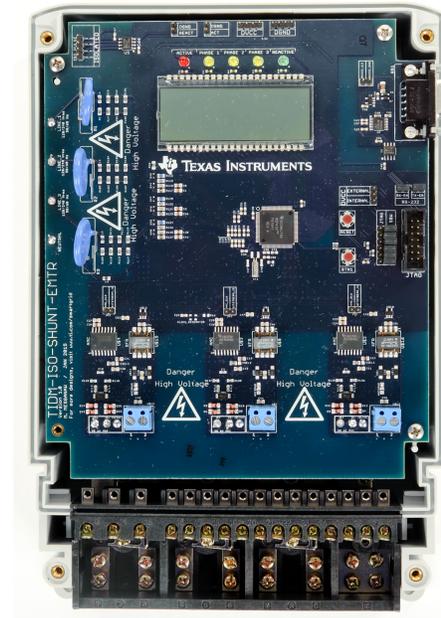


Figure 17. Top View TIDA-01088 Design

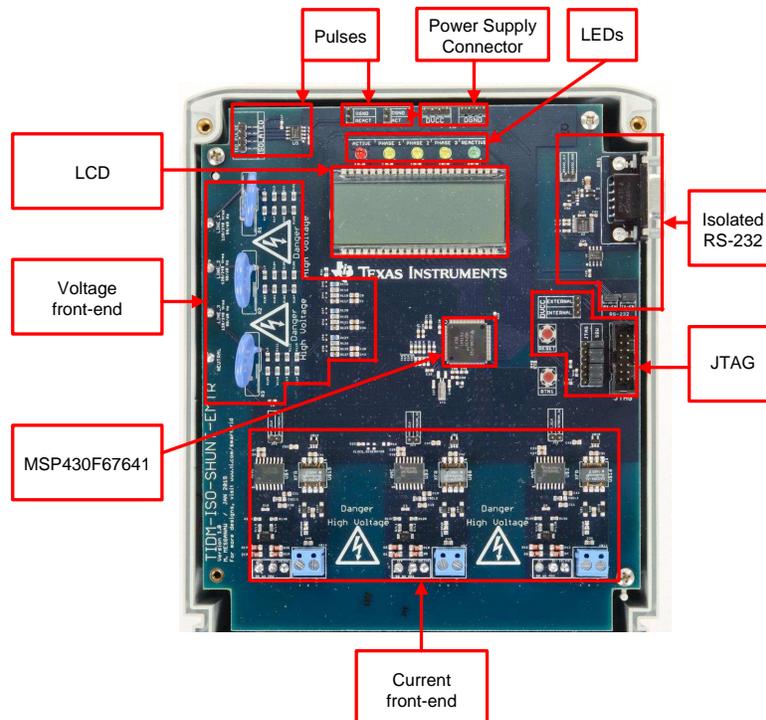


Figure 18. Top View of TIDA-01088 Design With Components Highlighted

5.1 Connections to the Test Setup for AC Voltages

AC voltages can be applied to the board for testing purposes at these points:

- Pad "LINE1" corresponds to the line connection for phase A.
- Pad "LINE2" corresponds to the line connection for phase B.
- Pad "LINE3" corresponds to the line connection for phase C.
- Pad "Neutral" corresponds to the neutral voltage. The voltage between any of the three line connections to the neutral connection must not exceed 230-V AC at 50 or 60 Hz.
- I1+, I1-, and I1Live are connected to the output terminals of the shunt that is used for measuring the current for phase A. When a shunt is selected, the differential voltage that is output across I1+ and I1- must not exceed 50 mV.
- I2+, I2-, and I2Live are connected to the output terminals of the shunt that is used for measuring the current for phase B. When a shunt is selected, the differential voltage that is output across I2+ and I2- must not exceed 50 mV.
- I3+, I3-, and I3Live are connected to the output terminals of the shunt that is used for measuring the current for phase C. When a shunt is selected, the differential voltage that is output across I3+ and I3- must not exceed 50 mV.

Figure 19 and Figure 20 show the various connections that must be made to the test setup for proper functionality of the EVM. When a test AC source must be connected, the connections have to be made according to the EVM design. Figure 19 shows the connections from the top view. VA+, VB+, and VC+ correspond to the line voltages for phases A, B, and C, respectively. VN corresponds to the neutral voltage from the test AC source.

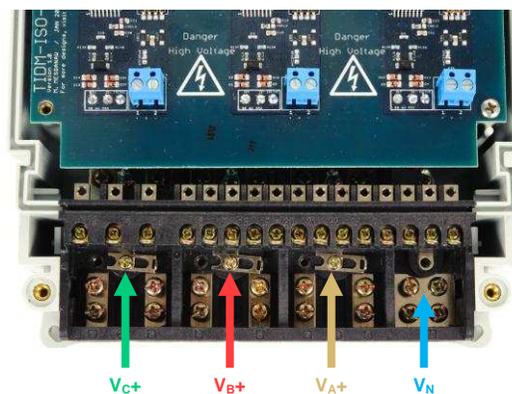


Figure 19. Top View of EVM With Test Setup Connections

Figure 20 shows the connections from the front view. IA+ and IA- correspond to the current inputs for phase A, IB+, and IB- correspond to the current inputs for phase B; IC+ and IC- correspond to the current inputs for phase C. VN corresponds to the neutral voltage from the test setup.

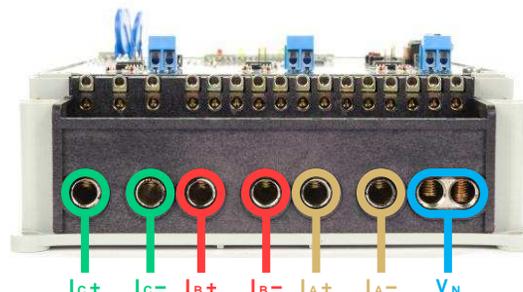


Figure 20. Front View of EVM With Test Setup Connections

5.2 Power Supply Options and Jumper Settings

The entire board is powered by a single DC voltage rail (DVCC), which can be derived either by JTAG or external power. Various jumper headers and jumper settings are present to add to the flexibility to the board. Some of these headers require that jumpers be placed appropriately for the board to correctly function. [Table 3](#) indicates the functionality of each jumper on the board.

Table 3. Header Names and Jumper Settings

HEADER/HEADER OPTION NAME	TYPE	MAIN FUNCTIONALITY	VALID USE-CASE	COMMENTS
ACT (Not isolated, do not probe)	1-pin header	Active energy pulses (WARNING)	Probe between here and ground for cumulative three-phase active energy pulses.	This header is not isolated from AC voltage, so do not connect measuring equipment unless isolators external to the EVM are available. See Isolated ACT instead.
AMC1PWR	3-pad jumper resistor footprint	Selection for the AMC1304 high-side power supply for Phase A	This header is used to select the power source for the AMC1304 associated with Phase A.	To enable powering the high-side using the on-board isolated power supply, place a 0-Ω resistor on the two top-most terminals (when the board is oriented as Figure 17 shows). To enable powering the high side by providing 4 V to 18 V directly to the U\$16-terminal block , place a 0-Ω resistor on the two bottom-most terminals (when the board is oriented as Figure 17 shows).
AMC2PWR	3-pad jumper resistor footprint	Selection for the AMC1304 high-side power supply for Phase B	This header is used to select the power source for the AMC1304 associated with Phase B.	To enable powering the high side using the on-board isolated power supply, place a 0-Ω resistor on the two top-most terminals (when the board is oriented as Figure 17 shows). To enable powering the high side by providing 4 V to 18 V directly to the U\$8-terminal block , place a 0-Ω resistor on the two bottom-most terminals (when the board is oriented as Figure 17 shows).
AMC3PWR	3-pad jumper resistor footprint	Selection for the AMC1304 high-side power supply for Phase C	This header is used to select the power source for the AMC1304 associated with Phase C.	To enable powering the high side using the on-board isolated power supply, place a 0-Ω resistor on the two top-most terminals (when the board is oriented as Figure 17 shows). To enable powering the high side by providing 4 V to 18 V directly to the U\$15-terminal block , place a 0-Ω resistor on the two bottom-most terminals (when the board is oriented as Figure 17 shows).

Table 3. Header Names and Jumper Settings (continued)

HEADER/HEADER OPTION NAME	TYPE	MAIN FUNCTIONALITY	VALID USE-CASE	COMMENTS
AMC_CLK (Not isolated, do not probe)	1-pin header	Modulation clock fed into the AMC1304	Probe between here and ground for the clock fed into the AMC1304 chips. An external clock can also be fed into this header to be used as the modulation clock; however, the software must be changed to accept a modulation clock input instead of providing one from the SD24_B.	Each AMC1304 has its own associated AMC_CLK header. However, all AMC_CLK headers are connected to each other.
BIT-STREAM_I1 (Not isolated, do not probe without isolated equipment)	1-pin header	Bit-stream output for the AMC associated with Phase A.	Probe between here and ground for the bit-stream output from the AMC1304 chip associated with Phase A.	
BIT-STREAM_I2 (Not isolated, do not probe without isolated equipment)	1-pin header	Bit-stream output for the AMC associated with Phase B.	Probe between here and ground for the bit-stream output from the AMC1304 chip associated with Phase B.	
BIT-STREAM_I3 (Not isolated, do not probe without isolated equipment)	1-pin header	Bit-stream output for the AMC associated with Phase C.	Probe between here and ground for the bit-stream output from the AMC1304 chip associated with Phase C.	
CSEL1	3-pad jumper resistor footprint	Capacitor Connection Select for the AMC1304 for Phase A	For this design, place a 0-Ω resistor on the two left-most terminals (when the board is oriented as Figure 17 shows).	
CSEL2	3-pad jumper resistor footprint	Capacitor Connection Select for the AMC1304 for Phase B	For this design, place a 0-Ω resistor on the two left-most terminals (when the board is oriented as Figure 17 shows).	
CSEL3	3-pad jumper resistor footprint	Capacitor Connection Select for the AMC1304 for Phase C	For this design, place a 0-Ω resistor on the two left-most terminals (when the board is oriented as Figure 17 shows).	
DGND (Not isolated, do not probe)	Header	Ground voltage header (WARNING)	Not a jumper header, probe here for GND voltage. Connect negative terminal of bench or external power supply when powering the board externally.	Do not probe if AC mains is not isolated.
DVCC (Not isolated, do not probe)	Header	VCC voltage header (WARNING)	Not a jumper header, probe here for VCC voltage. Connect positive terminal of bench or external power supply when powering the board externally.	Do not probe if AC mains is not isolated.
DVCC EXTERNAL (Do not connect JTAG if AC mains is not isolated)	Jumper header option	JTAG external power selection option (WARNING)	Place a jumper at this header option to select external voltage for JTAG programming.	This jumper option and the DVCC INTERNAL jumper option comprise one three-pin header used to select the voltage source for JTAG programming.

Table 3. Header Names and Jumper Settings (continued)

HEADER/HEADER OPTION NAME	TYPE	MAIN FUNCTIONALITY	VALID USE-CASE	COMMENTS
DVCC INTERNAL (Do not connect JTAG if AC mains is not isolated; isolated JTAG is fine)	Jumper header option	JTAG internal power selection option (WARNING)	Place a jumper at this header option to power the board using JTAG and to select the voltage from the USB FET for JTAG programming.	This jumper option and the DVCC EXTERNAL jumper option comprise one three-pin header used to select the voltage source for JTAG programming.
ISO_ACT	1-pin header	Isolated active energy pulses	Probe between here and ground for cumulative three-phase active energy pulses.	This header is isolated from AC voltage so it is safe to connect to scope or other measuring equipment because isolators are already present. However, either 3.3 V or 5 V must be applied between ISO_GND and ISO_VCC to produce pulses on this pin. The produced pulses have a logical high voltage that is equal to the voltage applied between ISO_GND and ISO_VCC.
ISO_GND	1-pin header	Isolated ground For energy pulses	Ground connection for the isolated active and reactive energy pulses.	
ISO_REACT	1-pin header	Isolate reactive energy pulses	Probe between here and ground for cumulative three-phase reactive energy pulses.	This header is isolated from AC voltage so it is safe to connect to scope or other measuring equipment since isolators are already present. However, either 3.3 V or 5 V must be applied between ISO_GND and ISO_VCC to produce pulses on this pin. The produced pulses have a logical high voltage that is equal to the voltage applied between ISO_GND and ISO_VCC.
ISO_VCC	1-pin header	Isolated VCC for energy pulses	VCC connection for the isolated active and reactive energy pulses.	Either 3.3 V or 5 V must be applied between ISO_GND and ISO_VCC to produce isolated active and reactive pulses on the respective isolated ISO_ACT and ISO_REACT pins. The produced pulses have a logical high voltage that is equal to the voltage applied between ISO_GND and ISO_VCC.
JTAG (Do not connect JTAG if AC mains is not isolated)	Jumper header option	4-wire JTAG programming option (WARNING)	Place jumpers at the JTAG header options of all of the six JTAG communication headers to select 4-wire JTAG.	There are six headers that jumpers must be placed at to select a JTAG communication option. Each of these six headers has a JTAG option and an SBW option to select either 4-wire JTAG or SBW. To enable 4-wire JTAG, all of these headers must be configured for the JTAG option. To enable SBW, all of the headers must be configured for the SBW option.

Table 3. Header Names and Jumper Settings (continued)

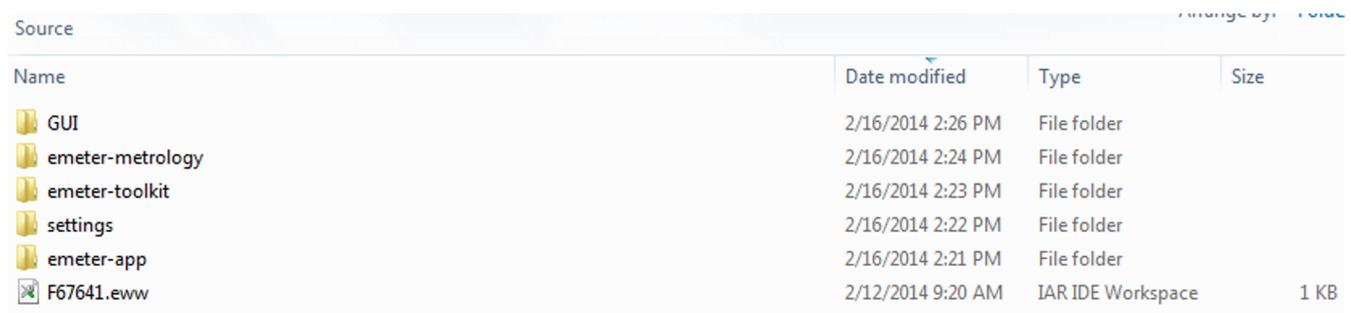
HEADER/HEADER OPTION NAME	TYPE	MAIN FUNCTIONALITY	VALID USE-CASE	COMMENTS
R16 Resistor	2-pad jumper resistor footprint	External clock generation selection	This design has a footprint that allows placing a clock generator (footprint is labeled CLOCK_GENERATOR on PCB) on the board so that it can be used for the modulation clock. When using this option, populating the clock generator footprint (not populated by default) and placing a 0-Ω resistor at R16 (also not populated by default) connects the clock generator to the AMC1304 and MSP430F67641.	If the external clock generator is used as the modulation clock of the AMC1304 and MSP430F67641, the software must be changed for the SD24_B to use an external clock and to prevent outputting the SD24_B clock.
REACT (Not isolated, do not probe)	1-pin header	Reactive energy pulses (WARNING)	Probe between here and ground for cumulative three-phase reactive energy pulses.	This header is not isolated from AC voltage so do not connect measuring equipment unless isolators external to the EVM are available. See isolated REACT instead.
RS232_3.3	1-pin header	Voltage source harvested from RS-232 line	Voltage source that is used to power the TRS3232 and ISO7321 for isolated RS-232 communication. This voltage source is harvested from the RS-232 line.	
RS232_GND	1-pin header	Ground connection for the isolated RS-232	Ground connection for the isolated RS-232 circuitry.	
RX_EN	Jumper header	RS-232 receive enable	Place a jumper here to enable receiving characters using RS-232.	
SBW (Do not connect JTAG if AC mains is not isolated)	Jumper header option	SBW JTAG programming option (WARNING)	Place jumpers at the SBW header options of all of the six JTAG communication headers to select SBW.	There are six headers that jumpers must be placed at to select a JTAG communication. Each of these six headers that have a JTAG option and a SBW option to select either 4-wire JTAG or SBW. To enable 4-wire JTAG, all of these headers must be configured for the JTAG option. To enable SBW, all of the headers must be configured for the SBW option.
TX_EN	Jumper header	RS-232 transmit enable	Place a jumper here to enable RS-232 transmissions.	

6 Getting Started Firmware

The source code is developed in the IAR™ environment using IAR compiler version 6.x. Earlier versions of IAR cannot open the project files. When the project is loaded in IAR version 6.x or later, the integrated development environment (IDE) prompts the user to create a backup. Click YES to proceed. There are four main parts to the energy metrology software:

- The toolkit that contains a library of mostly mathematics routines
- The metrology code that is used for calculating metrology parameters
- The application code that is used for the host-processor functionality of the system (that is, communication, LCD, RTC setup, and so forth)
- The GUI that is used for calibration

Figure 21 shows the contents of the source folder.



Name	Date modified	Type	Size
GUI	2/16/2014 2:26 PM	File folder	
emeter-metrology	2/16/2014 2:24 PM	File folder	
emeter-toolkit	2/16/2014 2:23 PM	File folder	
settings	2/16/2014 2:22 PM	File folder	
emeter-app	2/16/2014 2:21 PM	File folder	
F67641.eww	2/12/2014 9:20 AM	IAR IDE Workspace	1 KB

Figure 21. Source Folder Structure

Within the *emeter-app-67641* folder in the *emeter-app* folder, the *emeter-app-67641.ewp* project corresponds to the application code. Similarly, within the *emeter-metrology-67641* folder in the *emeter-metrology* folder, the *emeter-metrology-67641.ewp* project corresponds to the portion of the code for metrology. Additionally, the folder *emeter-toolkit-67641* within the *emeter-toolkit* has the corresponding toolkit project file *emeter-toolkit-67641.ewp*. For first-time use, TI recommends that all three projects be completely rebuilt by performing the following steps:

1. Open the IAR IDE.
2. Open the F67641 workspace, which is located in the *Source* folder.
3. Within IARs workspace window, click the *Overview* tab to have a list view of all the projects.
4. Right click the *emeter-toolkit-67641* option in the workspace window and select *Rebuild All*, as Figure 22 shows.
5. Right click the *emeter-metrology-67641* option in the workspace window and select *Rebuild All*, as Figure 23 shows.
6. Within IARs workspace window, click the *emeter-app-67641* tab.
7. Within the workspace window, select *emeter-app-67641*, click *Rebuild All* as Figure 24 shows, and then download this project onto the MSP430F67641 device.

Please note that if any changes are made to any of the files in the toolkit project and the project is compiled, the metrology project must be recompiled. After recompiling the metrology project, the application project must then be recompiled. Similarly, if any changes are made to any of the files in the metrology project and the project is compiled, the application project must then be recompiled.

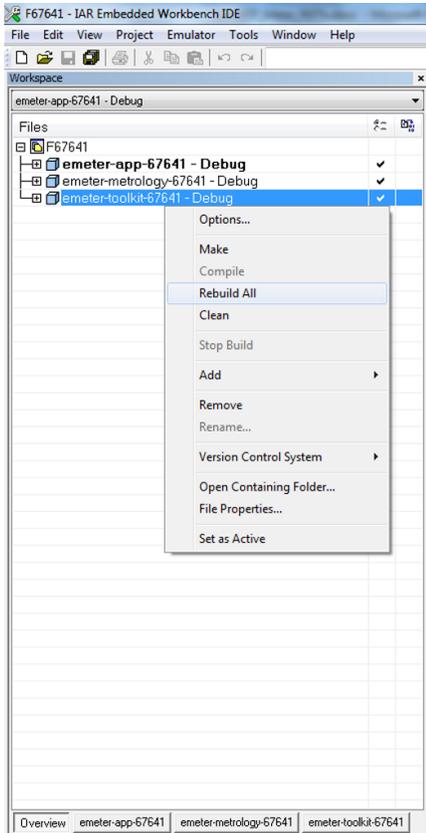


Figure 22. Toolkit Project Compilation

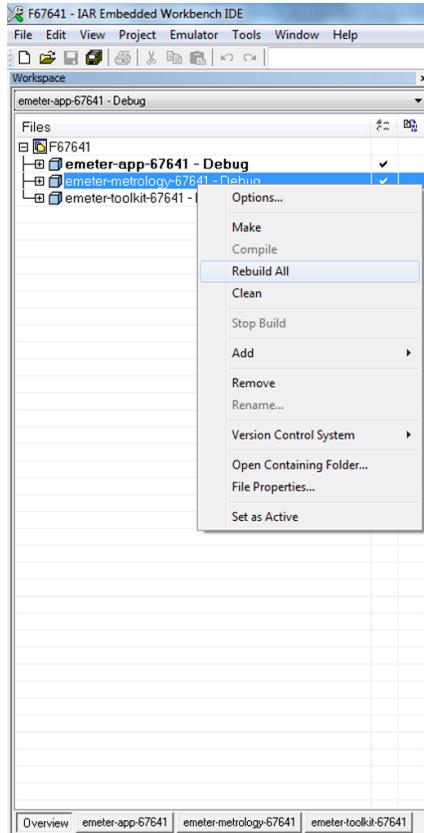


Figure 23. Metrology Project Compilation

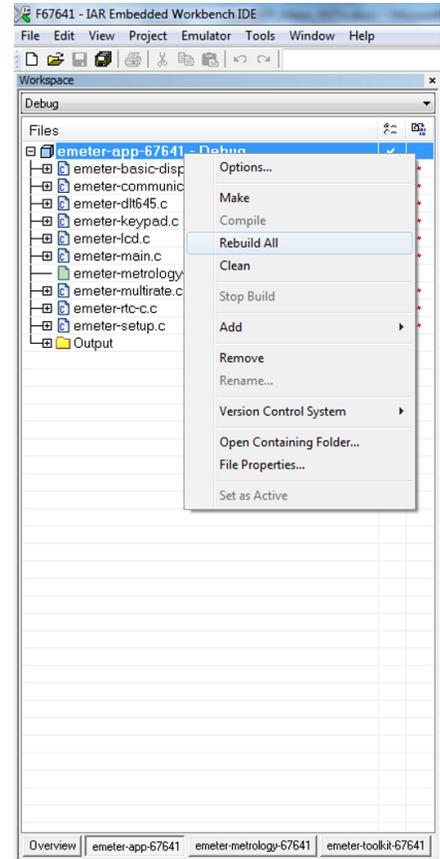


Figure 24. Application Project Compilation

7 Test Setup

For performing metrology testing, a source generator was used to provide the voltages and currents to the system at the proper locations mentioned in [Section 5.1](#). A nominal voltage of 230 V, calibration current of 10 A, nominal frequency of 50 Hz, power factor of 1, and shunt resistance value of 400 $\mu\Omega$ were used for each phase. In addition, for most test conditions, there is a fifth harmonic component added to both the fundamental voltage and current. For most tests, the fifth harmonic component of the current is set to 40% of the fundamental current and the fifth harmonic component of the voltage is set to 10% of the fundamental voltage. Also, since the used reference meter uses the THDR formula for calculating THD, the software is configured to also use this THDR formula for most of the test conditions. In the set of tests, eight different conditions were used for testing.

7.1 Condition 1: No Harmonics Present

In the first test condition, harmonics are not exposed to the system. Under this condition, active energy and reactive energy tests are conducted. For active and reactive energy testing, when the voltages and currents are applied to the system, the system outputs the cumulative active energy pulses at a rate of 6400 pulses/kWh. This pulse output is fed into a reference meter (in the test equipment, this is integrated in the same equipment used for the source generator) that determines the active energy % error based on the actual energy provided to the system and the measured energy as determined by the system's active energy output pulse. Based on this, a plot of active energy % error versus voltage is created. In addition, a plot of active energy % error versus current is created for 0°, 60°, and -60° phase shifts as shown in [Section 9.1](#). Using a similar procedure, a plot of reactive energy % error versus current is also created for 60° and -60°.

In addition to testing active and reactive energy % error, the phase to phase angle measurement is also tested. For this test, the phase to phase angle measurement on the GUI is compared to the reference meter's readings for these phase to phase angle readings. Also, the active energy error is recorded when the line frequency is varied from 50 Hz to 48 and 52 Hz.

7.2 Condition 2: Fifth Current Harmonic at 40%, Fifth Voltage Harmonic at 10%, 50 Hz

For the second test condition, a fifth harmonic component is added to both the voltage and current. The fifth harmonic component for voltage is set to 10% of the fundamental voltage and the fifth harmonic component for current is set to 40% of the fundamental current. The harmonic components are set so that they are aligned with the corresponding fundamental components. In addition, for this test the system uses a fundamental voltage of 230 V, frequency of 50 Hz, power factor of 1, and the THD_{IEC_R} formula for calculating the voltage and current THD.

Under these set of conditions, multiple current THD readings were taken from a fundamental current of 0.1 to 50 A. Over the same 0.1- to 50-A range, the % error of the fundamental active power is calculated using the measured fundamental active power and the fundamental active power reading from the reference meter. Similarly, for voltage THD calculations, multiple THD readings were taken from a fundamental voltage of 57.5 to 270 V at a current of 1 A. Over this same voltage range, the % error of the fundamental active power is calculated using the measured fundamental active power and the fundamental active power reading from the reference.

7.3 Condition 3: Fifth Current Harmonic at 40%, Fifth Voltage Harmonic at 10%, 60 Hz

Condition 3 is similar to condition 2 except the fundamental frequency is 60 Hz instead of 50 Hz. In addition, the nominal voltage was set to 120 V for the tests where current is varied with a fixed voltage.

7.4 Condition 4: Combination of Harmonics

Condition 4 is similar to condition 2 except there are multiple harmonic components added to both the voltage and current channels. For voltage, the third, fifth, seventh, and ninth harmonic components are added where each harmonic component is set to 2.5% of the fundamental voltage. For current, the third, fifth, seventh, and ninth harmonic components are each set to 10% of the fundamental current.

7.5 Condition 5: Fifth Current Harmonic at 4%, Fifth Voltage Harmonic at 2%

Condition 5 is similar to condition 2 except that instead of applying a fifth harmonic component at 40% for current, the fifth harmonic component is set to 4% of the fundamental. For voltage, the fifth harmonic component for this condition is set to 2% of the fundamental

7.6 Condition 6: Power Factor = 0, Reactive Power Testing

In this condition, the fundamental reactive power % error is tested by applying a power factor of 0. The other parameters for this test condition are set as it is done for condition 2.

7.7 Condition 7: THD_{IEC_F} Calculations

In this condition, condition 2 is tested but the THD_{IEC_F} formula is used instead of the THD_{IEC_R} formula. THD voltage values are obtained from a voltage range of 57.5 to 270 V at a current of 1 A. In addition, THD current values are obtained for a current range of 0.1 to 50 A at a voltage of 230 V.

Since the reference meter used for testing does not use this calculation formula for calculating THD, a THD_{IEC_F} calculation is calculated by looking at the reference meter's calculation of the amplitude of the fifth harmonic. Due to the source meter not being able to add a fifth harmonic component without adding a small portion of content at other harmonics, this measurement method would not be the most accurate because the system's THD reading would take into account the content at other harmonics while the calculation based on the reference meter's fifth harmonic content would not take this into account.

7.8 Condition 8: THD_{IEEE} Calculation

For condition 8, condition 2 is tested but the THD_{IEEE} is used instead of the THD_{IEC_R} formula. THD voltage values are obtained from a voltage range of 57.5 to 270 V at a current of 1 A. In addition, THD current values are obtained for a current range of 0.1 to 50 A at a voltage of 230 V.

For these sets of tests, the utilized reference meter does not use this formula for calculating THD but the reference meter's THD_{IEC_R} calculation can be converted to be in the form of this alternative THD calculation.

8 Viewing Metrology Readings and Calibration

8.1 Viewing Results From LCD

The LCD scrolls between metering parameters every two seconds. For each metering parameter that is displayed on the LCD, three items are usually displayed on the screen: a symbol used to denote the phase of the parameter, text to denote which parameter is being displayed, and the actual value of the parameter. The phase symbol is displayed at the top of the LCD and denoted by a triangle shape. The orientation of the symbol determines the corresponding phase. Figure 25, Figure 26, and Figure 27 show the mapping between the different orientations of the triangle and the phase descriptor:



Figure 25. Symbol for Phase A



Figure 26. Symbol for Phase B



Figure 27. Symbol for Phase C

Aggregate results (such as cumulative active and reactive power) and parameters that are independent of phase (such as time and date) are denoted by clearing all of the phase symbols on the LCD.

The bottom line of the LCD is used to denote the value of the parameter being displayed. The text to denote the parameter being shown displays on the top line of the LCD. Table 4 shows the different metering parameters that are displayed on the LCD and the associated units in which they are displayed. The designation column shows which characters correspond to which metering parameter.

Table 4. Displayed Parameters

PARAMETER NAME	DESIGNATION	UNITS	COMMENTS
Active power	AcPo	Watt (W)	This parameter is displayed for each phase. The aggregate active power is also displayed.
Reactive power	rePo	Volt-Ampere Reactive (var)	This parameter is displayed for each phase. The aggregate reactive power is also displayed.
Apparent power	APPo	Volt-Ampere (VA)	This parameter is displayed for each phase.
Power factor	PF	Constant between 0 and 1	This parameter is displayed for each phase.
Voltage	Urns	Volts (V)	This parameter is displayed for each phase.
Current	Inns	Amps (A)	This parameter is displayed for each phase.
Frequency	Frq	Hertz (Hz)	This parameter is displayed for each phase.
Total consumed active energy	AcEn	kWh	This parameter is displayed for each phase.
Total consumed reactive energy	reEn	kVarh	This parameter is displayed for each phase. This displays the sum of the reactive energy in quadrant 1 and quadrant 4.
Time	tine	Hour:minute:second	This parameter is only displayed when the sequence of aggregate readings are displayed. This parameter is not displayed once per phase.
Date	date	Year:month:day	This parameter is only displayed when the aggregate readings are displayed. This parameter is not displayed once per phase.

Figure 28 shows an example of phase Bs measured frequency of 49.99 Hz displayed on the LCD.

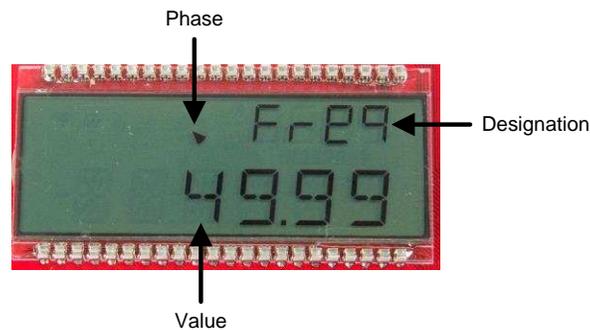


Figure 28. LCD Display

8.2 Calibrating and Viewing Results From PC

8.2.1 Viewing Results

To view the metrology parameter values from the GUI, perform the following steps:

1. Connect the EVM to a PC using an RS-232 cable.
2. Open the GUI folder and open *calibration-config.xml* in a text editor.
3. Change the *port name* field within the *meter* tag to the COM port connected to the system. As Figure 29 shows, this field is changed to *COM7*.

```

260     </correction>
261     </phase>
262     <temperature/>
263     <rtc/>
264 </cal-defaults>
265 <meter position="1">
266     <port name="com7" speed="9600"/>
267 </meter>
268 <reference-meter>
269     <port name="USB0::0x0A69::0x0835::A66200101281::INSTR"/>
270     <type id="chroma-66202"/>
271     <log requests="on" responses="on"/>
272     <scaling voltage="1.0" current="1.0"/>
273 </reference-meter>

```

Figure 29. GUI Configuration File Changed to Communicate With Energy Measurement System

- Run the *calibrator.exe* file, which is located in the GUI folder. If the COM port in the *calibration-config.xml* was changed in the previous step to the COM port connected to the EVM, the GUI opens (see [Figure 30](#)). If the GUI connects properly to the EVM, the top-left button is green. If there are problems with connections or if the code is not configured correctly, the button is red. Click the green button to view the results.

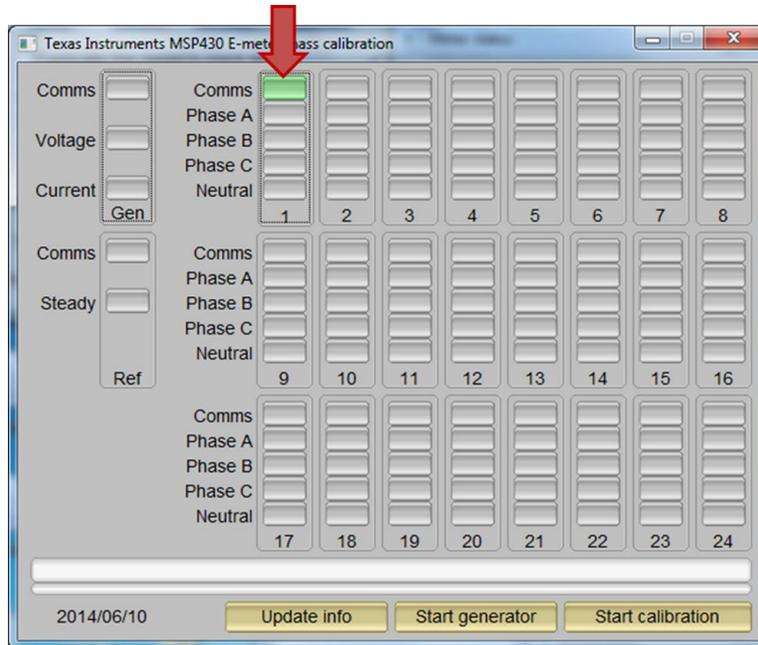


Figure 30. GUI Startup Window

Upon clicking on the green button, the results window opens (see [Figure 31](#)). In the figure, there is a trailing "L" or "C" on the *Power factor* values to indicate an inductive or capacitive load, respectively.



Figure 31. GUI Results Window

From the results window, the total-energy consumption readings and sag/swell logs can be viewed by clicking the *Meter Consumption* button. After the user clicks this button, the *Meter events and consumption* window pops up, as [Figure 32](#) shows.

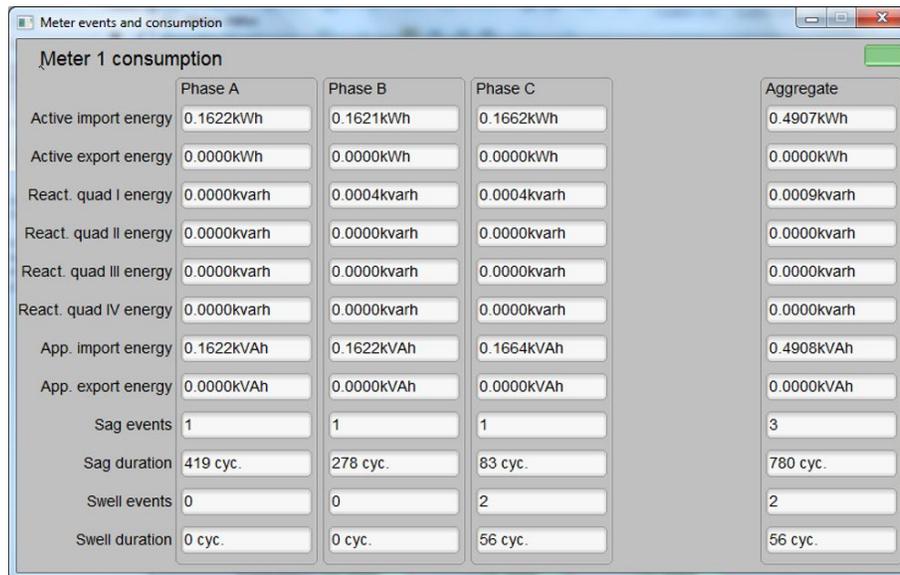


Figure 32. Meter Events and Consumption Window

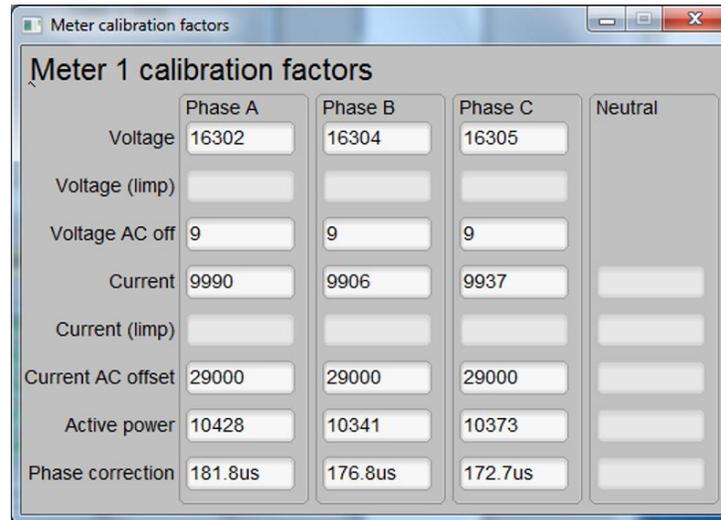
From this *Meter events and consumption* window, the user can view the meter settings by clicking the *Meter features* button, view the system calibration factors by clicking the *Meter calibration factors* button, or open the window used for calibrating the system by clicking the *Manual cal.* button.

8.2.2 Calibration

Calibration is key to any meter performance and it is absolutely necessary for every meter to go through this process. Initially, every meter exhibits different accuracies due to silicon-to-silicon differences, sensor accuracies, and other passive tolerances. To nullify their effects, every meter must be calibrated. To perform calibration accurately there should be an accurate AC test source and a reference meter available. The source must be able to generate any desired voltage, current, and phase shifts (between V and I). To calculate errors in measurement, the reference meter acts as an interface between the source and the meter being calibrated. This section discusses a simple and effective method of calibration of this three-phase EVM.

The GUI used for viewing results can easily be used to calibrate the EVM. During calibration, parameters called calibration factors are modified in software to give the least error in measurement. For this meter, there are six main calibration factors for each phase: voltage scaling factor, voltage AC offset, current scaling factor, current AC offset, power scaling factor, and the phase compensation factor. The voltage, current, and power scaling factors translate measured quantities in metrology software to real-world values represented in volts, amps, and watts, respectively. The voltage AC offset and current AC offset are used to eliminate the effect of additive white Gaussian noise (AWGN) associated with each channel. This noise is orthogonal to everything except itself; as a result, this noise is only present when calculating RMS voltages and currents. The last calibration factor is the phase compensation factor, which is used to compensate any phase shifts introduced by the current sensors and other passives. Please note that the voltage, current, and power calibration factors are independent of each other. Therefore, calibrating voltage does not affect the readings for RMS current or power.

When the meter software is flashed with the code (available in the *.zip file), default calibration factors are loaded into these calibration factors. These values are to be modified through the GUI during calibration. The calibration factors are stored in INFO_MEM, and therefore, remain the same if the meter is restarted. However, if the code is re-flashed during debugging, the calibration factors are replaced and the meter has to be recalibrated. One way to save the calibration values is by clicking on the *Meter calibration factors* button (see Figure 31). The *Meter calibration factors* window (see Figure 33) displays the latest values, which can be used to restore calibration values.



	Phase A	Phase B	Phase C	Neutral
Voltage	16302	16304	16305	
Voltage (imp)				
Voltage AC off	9	9	9	
Current	9990	9906	9937	
Current (imp)				
Current AC offset	29000	29000	29000	
Active power	10428	10341	10373	
Phase correction	181.8us	176.8us	172.7us	

Figure 33. Calibration Factors Window

Calibrating any of the scaling factors is referred to as gain correction. Calibrating the phase compensation factors is referred to as phase correction. For the entire calibration process, the AC test source must be ON, meter connections consistent with Section 5.1, and the energy pulses connected to the reference meter.

8.2.2.1 Active Power Calibration

When performing active power calibration for any given phase, the other two phases must be disabled. Typically, switching only the currents OFF is good enough for disabling a phase.

Also, unlike current and voltage gain calibration, the active power error value that is used for active power gain calibration must be obtained from the reference meter and must not be calculated. This error is obtained by feeding the meter's energy pulse outputs to the reference meter, which would use these pulses to calculate the error. Although, conceptually, performing active power gain calibration can be done as it is done for voltage or current, this method is not the most accurate. The best option to get the proper error % used for calibration is to get it directly from the reference meters measurement error of the active energy.

8.2.2.1.1 Active Power Gain Calibration

Note that this example is for one phase. Repeat these steps for other phases.

1. Make sure the test source is OFF.
2. Connect the energy pulse output of the system to the reference meter. Configure the reference meter to measure the active power error based on these pulse inputs.
3. Connect the GUI to view results for voltage, current, active power, and the other metering parameters.
4. Turn on the test source and configure it to supply desired voltage for all phases and the desired current for only the phase being calibrated. Ensure that there is a zero-degree phase shift between the calibrating phase's voltage and current. For example, an example voltage, current, and phase shift can be 230 V, 10 A, 0° (PF = 1).
5. Click on the *Manual cal.* button that [Figure 31](#) shows. The following screen pops up from [Figure 34](#):

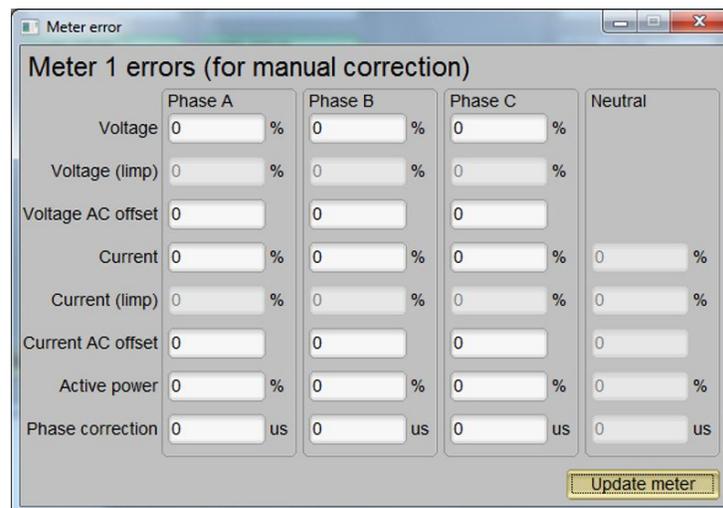


Figure 34. Manual Calibration Window

6. Obtain the % error in measurement from the reference meter. Note that this value may be negative.
7. Enter the error obtained in the previous Step 4 into the *Active Power* field under the corresponding phase in the [Figure 34](#) GUI window. This error is already the Correction (%) value and does not require calculation.
8. Click on *Update meter* button and the error values on the reference meter immediately settle to a value close to zero.

8.2.2.1.2 Active Power Phase Correction

After performing power gain correction, phase calibration must be performed. Similar to active power gain calibration, to perform phase correction on one phase, the other phases must be disabled. To perform phase correction calibration, perform the following steps:

1. If the AC test source has been turned OFF or reconfigured, perform Steps 2 through 4 from [Section 8.2.2.1.1](#) using the identical voltages and currents used in that section.
2. Disable all other phases that are not currently being calibrated by setting the current of these phases to 0 A.
3. Modify only the phase-shift to a non-zero value; typically, 60° is chosen. The reference meter now displays a different % error for active power measurement. Note that this value may be negative.

4. If this error from the previous Step 3 is not close to zero, or is unacceptable, perform phase correction by following these steps:
 - (a) In the [Figure 34](#) GUI window, enter a value as an update for the *Phase Correction* field for the phase that is being calibrated. Usually, a small \pm integer must be entered to bring the error closer to zero. Additionally, for a phase shift greater than 0 (for example: 60°), a positive (negative) error would require a positive (negative) number as correction.
 - (b) Click on the *Update meter* button and monitor the error values on the reference meter.
 - (c) If this measurement error (%) is not accurate enough, fine-tune by incrementing or decrementing by a value of 1 based on the previous Step 4a and Step 4b. Please note that after a certain point, the fine-tuning only results in the error oscillating on either side of zero. The value that has the smallest absolute error must be selected.
 - (d) Change the phase now to -60° and check if this error is still acceptable. Ideally, errors must be symmetric for same phase shift on lag and lead conditions.

After performing phase calibration, phase correction is complete for one phase. Repeat these steps to calibrate the other phases.

8.2.2.2 Voltage and Current Gain Calibration

After performing active power correction, gain correction must then be done for RMS voltage. When calibrating voltage, the voltages for all phases can be calibrated at the same time. Once voltage calibration has completed, RMS current must then be calibrated. Note that the calibration for RMS current must be done after active power and voltage are calibrated. Additionally, similar to RMS voltage, the currents for all phases can be calibrated at the same time. To perform either voltage or gain calibration, the following steps can be applied:

1. If the AC test source has been turned OFF or reconfigured, perform Steps 2 through 4 from [Section 8.2.2.1.1](#) using the identical voltages and currents used in that section.
2. Calculate the correction values for each voltage and current. The correction values that must be entered for the voltage and current fields are calculated by:

$$\text{Correction (\%)} = \left(\frac{\text{value}_{\text{observed}}}{\text{value}_{\text{desired}}} - 1 \right) \times 100 \quad (23)$$

where

- $\text{value}_{\text{observed}}$ is the value measured by the TI energy measurement system
 - $\text{value}_{\text{desired}}$ for calibrating voltage is the actual RMS voltage supplied to the meter. $\text{value}_{\text{desired}}$ for calibrating current is set to the fundamental current reading
3. After calculating for all voltages and currents, input these values as is (\pm) into the [Figure 34](#) window. This must be input into the fields *Voltage* and *Current* for the corresponding phases.
 4. Click on the *Update meter* button and the observed values for the voltages and currents on the GUI settle to the desired voltages and currents.

This completes calibration of voltage, current, and power for all three phases. The new calibration factors (see [Figure 35](#)) can be viewed by clicking the *Meter calibration factors* button of the GUI metering results window in [Figure 31](#).

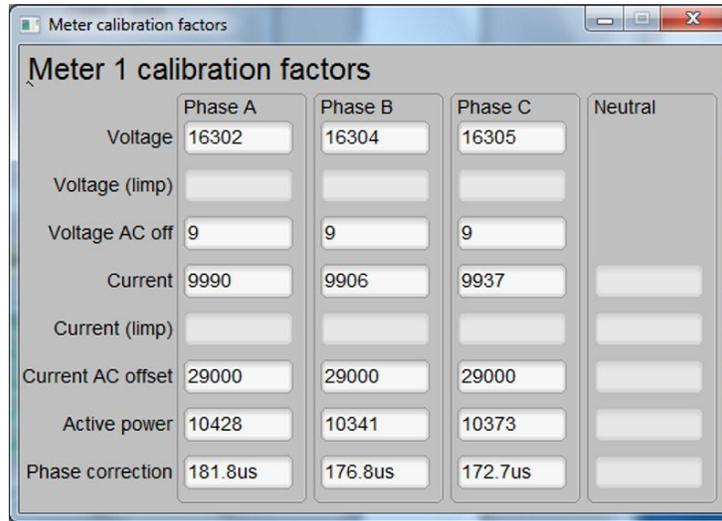


Figure 35. Calibration Factors Window

The configuration of the system can be viewed by clicking on the *Meter features* button in [Figure 31](#) to get to the window that [Figure 36](#) shows.

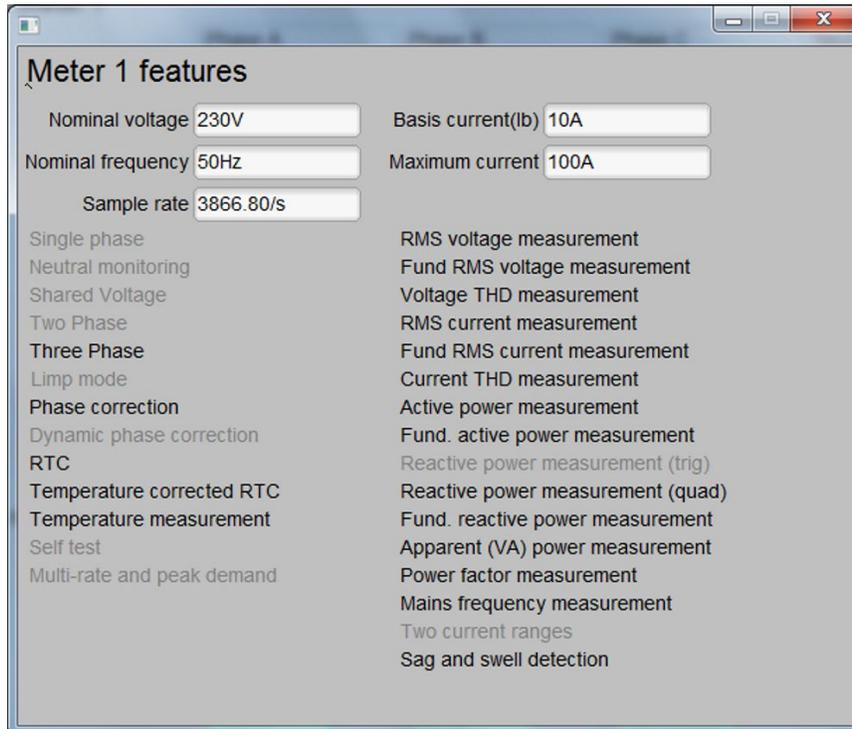


Figure 36. Meter Features Window

9 Test Data

9.1 Condition 1: No Harmonics Present

9.1.1 Active Energy versus Current

Table 5. Active Energy % Error Data

CURRENT (A)	0°	60°	-60°
0.05	-0.1020	-0.0650	-0.1350
0.10	-0.0270	-0.0300	-0.0490
0.25	-0.0100	-0.0070	-0.0440
0.50	-0.0025	0.0175	-0.0210
1.00	-0.0050	0.0160	-0.0220
2.00	-0.0090	0.0130	-0.0160
5.00	-0.0037	0.0010	-0.0120
10.00	0.0090	0.0190	-0.0030
20.00	0.0085	0.0230	-0.0180
30.00	0.0095	0.0240	-0.0133
40.00	0.0047	0.0180	-0.0150
50.00	-0.0110	0	-0.0240
60.00	-0.0213	-0.0140	-0.0420
70.00	-0.0290	-0.0340	-0.0490
80.00	-0.0520	-0.0530	-0.0690
90.00	-0.0720	-0.0810	-0.0970

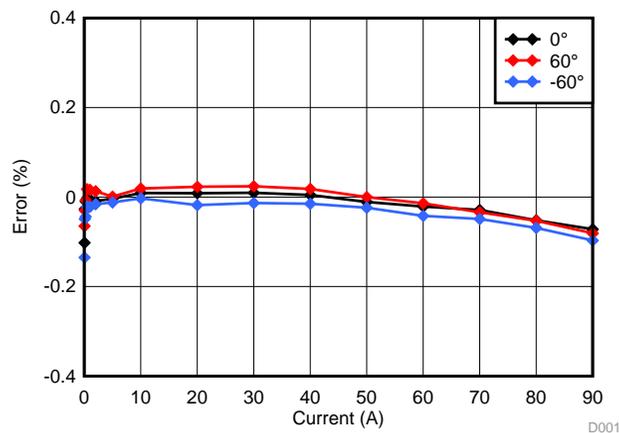


Figure 37. Active Energy % Error

9.1.2 Reactive Energy versus Current

Table 6. Reactive Energy % Error Data

CURRENT (A)	60°	-60°
0.05	-0.0980	-0.0770
0.10	0.0290	-0.0210
0.25	-0.0105	-0.0010
1.00	0.0120	-0.0030
2.00	0.0150	0
5.00	0.0180	0
10.00	0.0290	-0.0010
20.00	0.0230	-0.0120
30.00	0.0260	0.0097
40.00	0.0250	0.0030
50.00	0.0150	-0.0210
60.00	0.0110	-0.0240
70.00	-0.0080	-0.0320
80.00	0	-0.0250
90.00	-0.0110	-0.0470

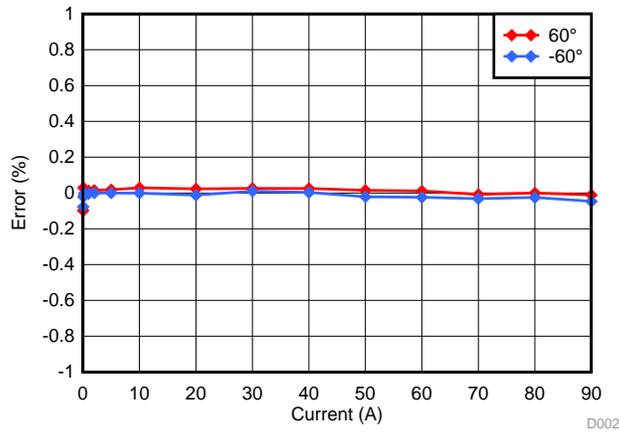


Figure 38. Reactive Energy % Error

9.1.3 Active Energy versus Voltage

Table 7. Cumulative Active Energy Measurement Error versus Voltage, 57.5 to 270 V

VOLTAGE (V)	ACTIVE ENERGY % ERROR
57.5	-0.1200
100	-0.0240
110	-0.0200
120	0.0037
150	0.0220
180	0.0060
210	0.0090
220	-0.0080
230	-0.0037
240	-0.0110
250	0.0005
260	-0.0057
265	0
270	-0.0030

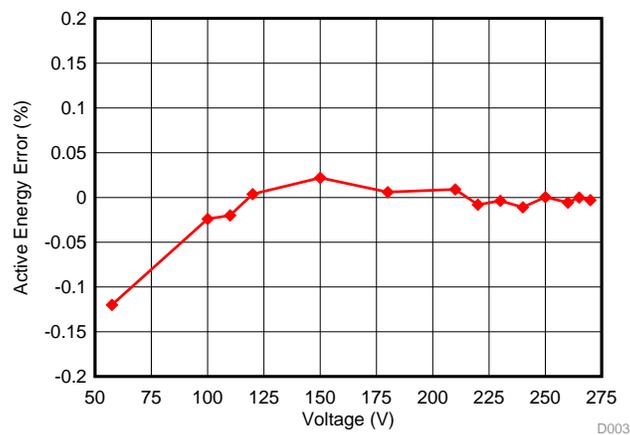


Figure 39. Cumulative Active Energy Measurement Error versus Voltage

9.1.4 Active Energy versus Frequency

Table 8. Active Energy versus Frequency

CONDITIONS	48 Hz	50 Hz	52 Hz
1.5 A, 0	-0.0027	-0.015	-0.019
1.5 A, 60	0.0250	0.006	-0.002
1.5 A, 300	-0.0400	-0.041	-0.048
15 A, 0	-0.0030	0	-0.010
15 A, 60	0.0120	0.021	0.018
15 A, 300	-0.0133	-0.032	-0.034

9.1.5 Voltage Phase-to-Phase Delay

Table 9. Voltage Phase-to-Phase Delay

ANGLE	ACTUAL (°)	MEASURED (°)	DIFFERENCE (°)
ϕ_{13}	240.192	240.03	0.162
ϕ_{21}	239.950	240.05	-0.100
ϕ_{32}	239.950	239.99	-0.040

9.2 Condition 2: Fifth Current Harmonic at 40%, 5th Voltage Harmonic at 10%, 50 Hz

9.2.1 Voltage THD

Table 10. Condition 2, Phase A Voltage THD

VOLTAGE (V)	ACTUAL VOLTAGE THD %	MEASURED VOLTAGE THD %
57.5	9.89480	9.87
120.0	9.95430	9.82
230.0	9.99800	9.97
270.0	9.98308	9.84

Table 11. Condition 2, Phase B Voltage THD

VOLTAGE (V)	ACTUAL VOLTAGE THD %	MEASURED VOLTAGE THD %
57.5	9.9106	9.95
120.0	9.9659	9.93
230.0	9.9809	9.98
270.0	9.9239	9.95

Table 12. Condition 2, Phase C Voltage THD

VOLTAGE (V)	ACTUAL VOLTAGE THD %	MEASURED VOLTAGE THD %
57.5	9.9888	9.98
120.0	9.9400	10.07
230.0	9.9822	9.79
270.0	9.9297	9.92

9.2.2 Current THD
Table 13. Condition 2, Phase A Current THD

CURRENT (A)	ACTUAL CURRENT THD %	MEASURED CURRENT THD %
0.10	37.348	36.78
0.25	37.284	37.01
1.00	37.294	37.03
10.00	37.251	37.04
50.00	37.255	37.04

Table 14. Condition 2, Phase B Current THD

CURRENT (A)	ACTUAL CURRENT THD %	MEASURED CURRENT THD %
0.10	37.334	36.85
0.25	37.279	37.06
1.00	37.278	37.12
10.00	37.266	37.12
50.00	37.278	37.12

Table 15. Condition 2, Phase C Current THD

CURRENT (A)	ACTUAL CURRENT THD %	MEASURED CURRENT THD %
0.10	37.369	36.88
0.25	37.296	37.09
1.00	37.264	37.17
10.00	37.279	37.18
50.00	37.264	37.16

9.2.3 Fundamental Active Power % Error versus Voltage
Table 16. Condition 2, Fundamental Active Power % Error versus Voltage

VOLTAGE (V)	PHASE A	PHASE B	PHASE C
	FUNDAMENTAL ACTIVE POWER % ERROR	FUNDAMENTAL ACTIVE POWER % ERROR	FUNDAMENTAL ACTIVE POWER % ERROR
57.5	-0.213790346	-0.274696617	-0.304173257
120.0	-0.022486883	-0.065833333	-0.087456272
230.0	0.017382991	-0.108634250	-0.063018819
270.0	0.001480330	-0.091063893	-0.082540623

9.2.4 Fundamental Active Power % Error versus Current
Table 17. Condition 2, Fundamental Active Power % Error versus Current

CURRENT (A)	PHASE A	PHASE B	PHASE C
	FUNDAMENTAL ACTIVE POWER % ERROR	FUNDAMENTAL ACTIVE POWER % ERROR	FUNDAMENTAL ACTIVE POWER % ERROR
0.10	-0.021723074	-0.078240459	-0.091264668
0.25	-0.001738103	-0.090398623	-0.090417485
1.00	-0.017380725	-0.051308809	-0.105148816
50.00	-0.019122121	-0.122555411	-0.086933843

9.3 Condition 3: Fifth Current Harmonic at 40%, Fifth Voltage Harmonic at 10%, 60 Hz

9.3.1 Voltage THD

Table 18. Condition 3, Phase A Voltage THD

VOLTAGE (V)	ACTUAL VOLTAGE THD %	MEASURED VOLTAGE THD %
57.5	9.9943	10.26
230.0	9.9863	10.05
270.0	9.9595	9.82

Table 19. Condition 3, Phase B Voltage THD

VOLTAGE (V)	ACTUAL VOLTAGE THD %	MEASURED VOLTAGE THD %
57.5	9.9777	10.02
230.0	9.9759	9.85
270.0	9.9671	9.98

Table 20. Condition 3, Phase C Voltage THD

VOLTAGE (V)	ACTUAL VOLTAGE THD %	MEASURED VOLTAGE THD %
57.5	9.9724	10.00
230.0	9.9783	9.94
270.0	9.9536	9.79

9.3.2 Current THD

Table 21. Condition 3, Phase A Current THD

CURRENT (A)	ACTUAL CURRENT THD %	MEASURED CURRENT THD %
0.10	37.438	36.66
0.25	37.338	36.92
1.00	37.319	37.00
10.00	37.298	36.97
50.00	37.300	36.96

Table 22. Condition 3, Phase B Current THD

CURRENT (A)	ACTUAL CURRENT THD %	MEASURED CURRENT THD %
0.10	37.430	36.80
0.25	37.335	37.05
1.00	37.325	37.13
10.00	37.312	37.12
50.00	37.314	37.13

Table 23. Condition 3, Phase C Current THD

CURRENT (A)	ACTUAL CURRENT THD %	MEASURED CURRENT THD %
0.10	37.461	36.80
0.25	37.368	37.05
1.00	37.345	37.12
10.00	37.325	37.10
50.00	37.325	37.09

9.3.3 Fundamental Active Power % Error versus Voltage

Table 24. Condition 3, Fundamental Active Power % Error versus Voltage

VOLTAGE (V)	PHASE A	PHASE B	PHASE C
	FUNDAMENTAL ACTIVE POWER % ERROR	FUNDAMENTAL ACTIVE POWER % ERROR	FUNDAMENTAL ACTIVE POWER % ERROR
57.5	-0.175679672	-0.309312388	-0.231340558
120.0	-0.123179359	-0.143202065	-0.009167431
230.0	-0.128990228	-0.107316649	-0.005652911
270.0	-0.086184576	-0.133205062	-0.001852401

9.3.4 Fundamental Active Power % Error versus Current

Table 25. Condition 3, Fundamental Active Power % Error versus Current

CURRENT (A)	PHASE A	PHASE B	PHASE C
	FUNDAMENTAL ACTIVE POWER % ERROR	FUNDAMENTAL ACTIVE POWER % ERROR	FUNDAMENTAL ACTIVE POWER % ERROR
0.10	-0.039086250	-0.138997481	-0.043487715
0.25	-0.079915220	-0.149445661	-0.001739917
1.00	-0.123179359	-0.143202065	-0.009167431
50.00	-0.095560768	-0.151172893	-0.012006264

9.4 Condition 4: Combination of Harmonics

9.4.1 Voltage THD

Table 26. Condition 4, Phase A Voltage THD

VOLTAGE (V)	ACTUAL VOLTAGE THD %	MEASURED VOLTAGE THD %
230	5	4.78

Table 27. Condition 4, Phase B Voltage THD

VOLTAGE (V)	ACTUAL VOLTAGE THD %	MEASURED VOLTAGE THD %
230	5	4.82

Table 28. Condition 4, Phase C Voltage THD

VOLTAGE (V)	ACTUAL VOLTAGE THD %	MEASURED VOLTAGE THD %
230	4.9902	4.92

9.4.2 Current THD
Table 29. Condition 4, Phase A Current THD

CURRENT (A)	ACTUAL CURRENT THD %	MEASURED CURRENT THD %
0.10	19.791	18.78
0.25	19.771	19.37
1.00	19.739	19.52
10.00	19.776	19.62
50.00	19.742	19.43

Table 30. Condition 4, Phase B Current THD

CURRENT (A)	ACTUAL CURRENT THD %	MEASURED CURRENT THD %
0.10	19.821	18.89
0.25	19.750	19.41
1.00	19.747	19.55
10.00	19.730	19.54
50.00	19.740	19.58

Table 31. Condition 4, Phase C Current THD

CURRENT (A)	ACTUAL CURRENT THD %	MEASURED CURRENT THD %
0.10	19.790	18.93
0.25	19.752	19.48
1.00	19.756	19.63
10.00	19.747	19.64
50.00	19.739	19.61

9.4.3 Fundamental Active Power % Error
Table 32. Condition 4, Fundamental Active Power % Error

CURRENT (A)	PHASE A	PHASE B	PHASE C
	FUNDAMENTAL ACTIVE POWER % ERROR	FUNDAMENTAL ACTIVE POWER % ERROR	FUNDAMENTAL ACTIVE POWER % ERROR
0.10	-0.030410983	-0.104302477	-0.169454703
0.25	-0.026075619	-0.119964532	-0.012183236
1.00	-0.002606769	-0.097770825	-0.137712325
50.00	-0.006954103	-0.103424300	-0.096504956

9.5 Condition 5: Fifth Current Harmonic at 4%, Fifth Voltage Harmonic at 2%

9.5.1 Voltage THD

Table 33. Condition 5, Phase A Voltage THD

VOLTAGE (V)	ACTUAL VOLTAGE THD %	MEASURED VOLTAGE THD %
230	1.9758	1.79

Table 34. Condition 5, Phase B Voltage THD

VOLTAGE (V)	ACTUAL VOLTAGE THD %	MEASURED VOLTAGE THD %
230	1.9638	1.38

Table 35. Condition 5, Phase C Voltage THD

VOLTAGE (V)	ACTUAL VOLTAGE THD %	MEASURED VOLTAGE THD %
230	1.9643	2.04

9.5.2 Current THD

Table 36. Condition 5, Phase A Current THD

CURRENT (A)	ACTUAL CURRENT THD %	MEASURED CURRENT THD %
0.25	4.0046	3.32
1.00	4.0168	3.77
10.00	4.0322	3.85
50.00	4.0176	4.02

Table 37. Condition 5, Phase B Current THD

CURRENT (A)	ACTUAL CURRENT THD %	MEASURED CURRENT THD %
0.25	4.0159	3.17
1.00	4.0220	3.82
10.00	4.0116	3.84
50.00	4.0123	3.91

Table 38. Condition 5, Phase C Current THD

CURRENT (A)	ACTUAL CURRENT THD %	MEASURED CURRENT THD %
0.25	4.0313	3.43
1.00	3.9964	4.25
10.00	4.0014	4.28
50.00	4.0108	4.11

9.5.3 Fundamental Active Power % Error

Table 39. Condition 5, Fundamental Active Power % Error

CURRENT (A)	PHASE A	PHASE B	PHASE C
	FUNDAMENTAL ACTIVE POWER % ERROR	FUNDAMENTAL ACTIVE POWER % ERROR	FUNDAMENTAL ACTIVE POWER % ERROR
0.25	-0.015646460	-0.088664812	-0.128644194
1.00	-0.013468891	-0.088668666	-0.106017814
50.00	-0.027813994	-0.118219750	-0.099973920

9.6 Condition 6: Power Factor = 0, Reactive Power Testing

9.6.1 Fundamental Reactive Power % Error

Table 40. Condition 6, Fundamental Active Power % Error

CURRENT (A)	PHASE A	PHASE B	PHASE C
	FUNDAMENTAL REACTIVE POWER % ERROR	FUNDAMENTAL REACTIVE POWER % ERROR	FUNDAMENTAL REACTIVE POWER % ERROR
0.10	-0.026067689	-0.152121001	-0.156426523
0.25	0	-0.085198129	-0.078245901
1.00	0.015641973	-0.079547924	-0.107737087
50.00	-0.026073353	-0.093888551	-0.089534075

9.7 Condition 7: THD_{IEC,F} Calculations

9.7.1 Voltage THD

Table 41. Condition 7, Phase A Voltage THD

VOLTAGE (V)	ESTIMATED ACTUAL VOLTAGE THD %	MEASURED VOLTAGE THD %
57.5	9.8537	9.95
120.0	10.0010	9.87
230.0	9.9217	9.80
270.0	10.0200	9.85

Table 42. Condition 7, Phase B Voltage THD

VOLTAGE (V)	ESTIMATED ACTUAL VOLTAGE THD %	MEASURED VOLTAGE THD %
57.5	9.9126	10.00
120.0	10.0030	9.92
230.0	9.9458	9.78
270.0	10.0070	10.00

Table 43. Condition 7, Phase C Voltage THD

VOLTAGE (V)	ESTIMATED ACTUAL VOLTAGE THD %	MEASURED VOLTAGE THD %
57.5	9.950	10.00
120.0	10.024	9.89
230.0	10.007	9.83
270.0	10.029	9.91

9.7.2 Current THD

Table 44. Condition 7, Phase A Current THD

CURRENT (A)	ESTIMATED ACTUAL CURRENT THD %	MEASURED CURRENT THD %
0.10	40.253	39.50
0.25	40.190	39.84
1.00	40.153	39.90
10.00	40.127	39.91

Table 45. Condition 7, Phase B Current THD

CURRENT (A)	ESTIMATED ACTUAL CURRENT THD %	MEASURED CURRENT THD %
0.10	40.270	39.58
0.25	40.180	39.92
1.00	40.168	39.98
10.00	40.143	39.97

Table 46. Condition 7, Phase C Current THD

CURRENT (A)	ESTIMATED ACTUAL CURRENT THD %	MEASURED CURRENT THD %
0.10	40.276	39.69
0.25	40.191	39.97
1.00	40.158	40.04
10.00	40.162	40.03

9.8 Condition 8: THD_{IEEE} Calculations Calculation

9.8.1 Voltage THD

Table 47. Condition 8, Phase A Voltage THD

VOLTAGE (V)	ESTIMATED ACTUAL VOLTAGE THD %	MEASURED VOLTAGE THD %
57.5	0.970422010	0.98
120.0	0.996562958	0.96
230.0	0.979446709	1.03
270.0	0.978496856	0.99

Table 48. Condition 8, Phase B Voltage THD

VOLTAGE (V)	ESTIMATED ACTUAL VOLTAGE THD %	MEASURED VOLTAGE THD %
57.5	0.995784452	0.99
120.0	0.977547464	0.96
230.0	0.990542468	1.06
270.0	0.999520058	0.97

Table 49. Condition 8, Phase C Voltage THD

VOLTAGE (V)	ESTIMATED ACTUAL VOLTAGE THD %	MEASURED VOLTAGE THD %
57.5	0.982279210	1.00
120.0	0.989169485	0.96
230.0	0.996083842	1.01
270.0	0.995984040	0.97

9.8.2 Current THD

Table 50. Condition 8, Phase A Current THD

CURRENT (A)	ESTIMATED ACTUAL CURRENT THD %	MEASURED CURRENT THD %
0.10	16.22075625	15.65
0.25	16.13066569	15.89
1.00	16.11621025	15.93
10.00	16.10818225	15.90
50.00	16.11540736	15.91

Table 51. Condition 8, Phase B Current THD

CURRENT (A)	ESTIMATED ACTUAL CURRENT THD %	MEASURED CURRENT THD %
0.10	16.19257600	15.79
0.25	16.12986244	15.94
1.00	16.13468224	15.99
10.00	16.12584649	15.97
50.00	16.12745281	15.98

Table 52. Condition 8, Phase C Current THD

CURRENT (A)	ESTIMATED ACTUAL CURRENT THD %	MEASURED CURRENT THD %
0.10	16.20948121	15.74
0.25	16.17648400	16.00
1.00	16.09534161	16.03
10.00	16.14593124	16.03
50.00	16.12905921	16.04

10 Design Files

10.1 Schematics

To download the schematics, see the design files at [TIDA-01088](#).

10.2 Bill of Materials

To download the bill of materials (BOM), see the design files at [TIDA-01088](#).

10.3 PCB Layout Recommendations

For this design, follow these general guidelines:

- Place decoupling capacitors close to their associated pins.
- Use ground planes instead of ground traces and minimize the cuts in the ground plane, especially for the ground planes of the high side of each AMC1304. In this design, there is a ground plane on both the top and bottom layer; for this situation, ensure that there is good stitching between the planes through the liberal use of vias.
- Each AMC1304 must have its own set of ground planes that are used for the high side of each AMC1304. Each of these ground planes is actually referenced from a different line voltage because each AMC1304 must be connected to a different line voltage.
- Use a different ground plane for the isolated RS-232. This other ground plane is at the potential of the RS-232 ground and not DGND.
- Avoid crosstalk from the delta-sigma modulation clock traces or the AMC1304 bit-stream traces.
- Minimize the length of the traces used to connect the crystal to the microcontroller. Place guard rings around the leads of the crystal and ground the crystal housing. In addition, there must be clean ground underneath the crystal and placing any traces underneath the crystal must be avoided. Also, keep high frequency signals away from the crystal.
- Use wide traces for power supply connections.
- Maintain at least an 8.1-mm spacing between the ground planes of the high side of each AMC1304 device and the ground plane on the controller side. This spacing maintains the recommended clearance for the AMC1304 isolation rating. In addition, ensure that the recommended clearance and creepage spacing for other isolation devices (such as the ISO7420 and ISO7421) is also followed.
- Keep the traces of the analog input pin symmetrical and as close as possible to each other.

10.3.1 Layout Prints

To download the layer plots, see the design files at [TIDA-01088](#).

10.4 CAD Project

To download the CAD project files, see the design files at [TIDA-01088](#).

10.5 Gerber Files

To download the Gerber files, see the design files at [TIDA-01088](#).

11 Software Files

To download the software files, see the design files at [TIDA-01088](#).

12 References

1. Texas Instruments, *Isolated, Shunt-Based Current Sensing Reference Design*, User's Guide, ([TIDU384](#))
2. Texas Instruments, *Self-Powered Isolated RS-232 to UART Interface*, User's Guide, ([TIDU298](#))
3. Texas Instruments, *Implementation of a Low-Cost Three-Phase Electronic Watt-Hour Meter Using the MSP430F67641*, Application Report, ([SLAA621](#))

13 About the Author

MEKRE MESGANAW is a systems engineer in the Smart Grid and Energy group at Texas Instruments, where he primarily works on grid monitoring, customer support, and reference design development. Mekre received his bachelor of science and master of science in computer engineering from the Georgia Institute of Technology.

Revision A History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (May 2016) to A Revision	Page
• Changed from preview page.....	1

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