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TI Designs: PMP9779
Output Short-Circuit Protection Reference Design for the TPS61088 Boost Converter

Design Overview

This reference design delivers an output short-circuit protection solution for the TPS61088 boost converter. This feature is realized by an over current protection (OCP) circuit. When the output is shorted to ground or the load current is higher than a certain value, the OCP circuit will disconnect the TPS61088 from the load. This solution just requires an additional low-cost comparator, a sense resistor, and a small sized N-MOSFET. With this small amount of additional circuitry, the TPS61088 is protected from being damaged in the output short circuit and over load conditions.

Design Resources

PMP9779	Design folder
TPS61088	Product Folder

Design Features

- 2.7V to 4.2V input voltage range
- 5V/3A, 9V/2A and 12V/1.5A output capability
- Output short circuit and over load protection
- True disconnection between input and output during shut down
- Ideal for power bank, blue-tooth speaker application, etc.

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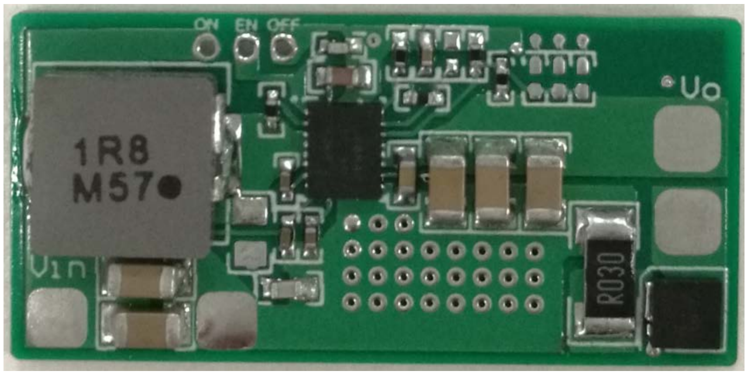

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1 Introduction

The Synchronous boost converter TPS61088 is an easy to use step-up DC-DC converter which provides a high efficiency and small size solution in portable systems. It is widely used in quick charge power bank, blue-tooth speaker, and portable POS terminal application, etc. The TPS61088 implements cycle-by-cycle current limit to protect the device from overload conditions during boost switching. This current limit function is realized by detecting the current flowing through the low side MOSFET. So the current limit feature will lose function in the output short circuit condition or the over load condition when the output voltage drops below the input voltage.

Lithium ion or lithium polymer battery is one of the key components in some portable systems, especially like power banks. Although these types of batteries are commonly used, the safety of the battery related products are always the utmost concern. The lithium ion or the lithium polymer battery has the potential risks of “fires” and “explosions” in short circuit, over voltage, or high temperature conditions. An increasing number of such catastrophes have been reported in the past few years.

To safeguard the consumers against bodily harm and property damage, UL announced the first dedicated safety standard UL2056 for power bank industry at the end of last year. The test items include output power overload test. So a power bank with output short circuit protection can easily pass the UL’s over load test and it is safe for the end customers in the case of output short circuit during the usage.

This reference design delivers an output short-circuit protection solution for the boost converter TPS61088. This feature is realized by an over current protection (OCP) circuit. When the output is shorted to ground or the load current is higher than a certain value, the TPS61088 will be disconnected from the load. This solution just requires an additional low-cost comparator, a sense resistor, and a small sized N-MOSFET. With this small amount of additional circuitry, the TPS61088 is protected from being damaged in the output short circuit and over load conditions.

2 Specification

Table 1 gives out the performance specification of this reference design. When the output current is higher than 4.4 A, the TPS61088 will be disconnected from the load.

Table 1. Performance Specification

Input Voltage	Output Voltage/Output Current	Over Current Protection Point
3V-4.2V	5V/3A, 9V/2A, 12V/1.5A	Io ≥ 4.4A

3 Design Process

This section provides the PMP9779 block diagram introduction and the over current protection circuit design. For the power components and compensation network calculation, please refer to the TPS61088 datasheet.

3.1 Block Diagram

Figure 1 shows the block diagram of this reference design. A shunt resistor Rs is placed in the output return. It converts the output current to a voltage signal V_{SENSE}. In the overload or output short circuit condition, V_{SENSE} is higher than the reference voltage V_{REF}. The comparator TL331's output signal V_{O_TL331} gets high, so Q2 turns on and Q1 turns off. Thus the boost converter TPS61088 is disconnected from the load. When the output overload or short circuit condition is removed, the circuits can recovery by toggling (disable then enable) the TPS61088's EN pin.

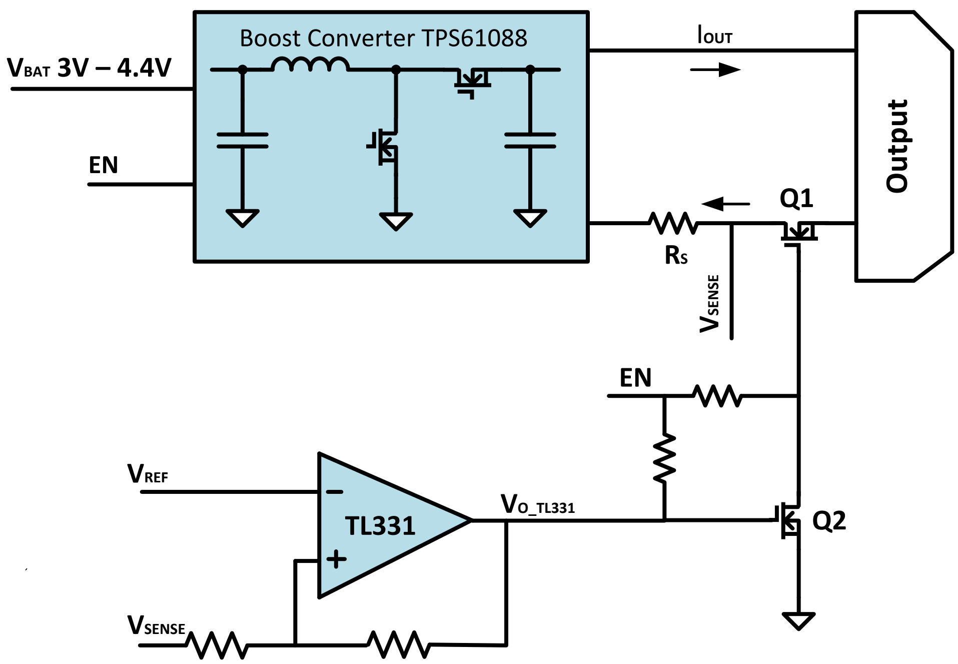

Figure 1. Block Diagram of PMP9779

3.2 Over Current Protection Circuit Design

3.2.1 Setting Over Current Protection Point

The over current protection point should be higher than the maximum output current. In this reference design, the maximum output current is 3 A (occurs at V_O = 5 V condition). We set the over current protection point at 4.4 A to avoid the protection circuit from false triggering at normal output current conditions.

3.2.2 Shunt Resistor Selection

Shunt resistor is the most versatile and cost effective means to measure the current. The voltage across it should be kept to a low value to reduce the power loss. In this reference design, the shunt resistor value R_S is chosen as 30 mΩ. The maximum continuous current I_{MEAN_MAX} flowing through the shunt resistor before OCP is 4.4 A. So the maximum shunt voltage V_{SENSE_MAX} can be calculated by the following equation:

$$V_{SENSE\_MAX} = R_S \cdot I_{MEAN\_MAX} \qquad (1)$$

The minimum power rating of the shunt resistor can be calculated by equation (2):

$$P_{rating} = V_{SENSE\_MAX} \cdot I_{MEAN\_MAX} \qquad (2)$$

So the minimum power rating of the shunt resistor is calculated as 0.58W in this reference design. A general rule of thumb is multiplying this minimum power rating by 2. That is, we should choose a ≥1W resistor in this reference design to make it more robust in the overload or output short circuit condition.

3.2.3 Comparator Circuit Design

Figure 2 illustrates the hysteresis comparator circuit in this reference design. The reference voltage V_{REF} is put at the TL331's inverting input, V_{REF} = 110mV. The current sense signal V_{SENSE} is connected to the TL331's non-inverting input through R12.

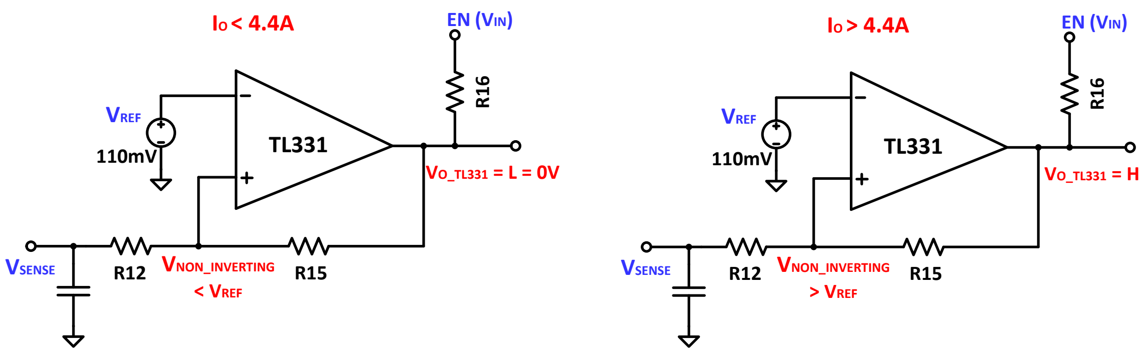

Figure 2. Comparator Circuit with Hysteresis

During the normal operation, the output current is lower than the over current protection point, the comparator's output is at logic low (0 V). So the voltage $V_{NON\_INVERTING}$ at the TL331's non-inverting positive input is:

$$V_{NON\_INVERTING} = V_{SENSE} \cdot \frac{R_{15}}{R_{15} + R_{12}} \qquad (3)$$

When the output current increases to the targeted transition point, we have:

$$V_{SENSE} = V_{SENSE\_MAX} = 132\ mV \quad (4)$$

$$V_{NON\_INVERTING} = V_{REF} = 110\ mV \quad (5)$$

Insert (4) and (5) into equation (3), we can get:

$$R_{15} = 5 \cdot R_{12} \quad (6)$$

So select R_{12} = 100 kΩ, R_{15} = 499 kΩ in this reference design.

After the over current protection, the comparator’s output is at logic high. Q1 turns off. The TPS61088 disconnects with the load. In order to avoid the Q1 being turned on and off frequently before fault clearing, the voltage $V_{NON\_INVERTING}$ at the TL331’s positive input should always higher than the reference voltage V_{REF} after OCP happens. We can realize this by choosing an appropriate resistance R16 under the minimum input voltage condition:

$$V_{IN\_MIN} \cdot \frac{R_{12}}{R_{12} + R_{15} + R_{16}} \geq V_{REF} \quad (7)$$

$$R_{16} \leq \frac{V_{IN\_MIN}}{V_{REF}} - R_{12} - R_{15} \quad (8)$$

Where

- $V_{IN\_MIN} = 3V$

We choose R_{16}=R_{12}=100 kΩ in this reference design.

4 Test Result

4.1 Startup Waveforms

Figure 3 shows the startup waveforms of the Q1's gate drive signal, inductor current and the output voltage at V_{IN} = 3.6V condition.

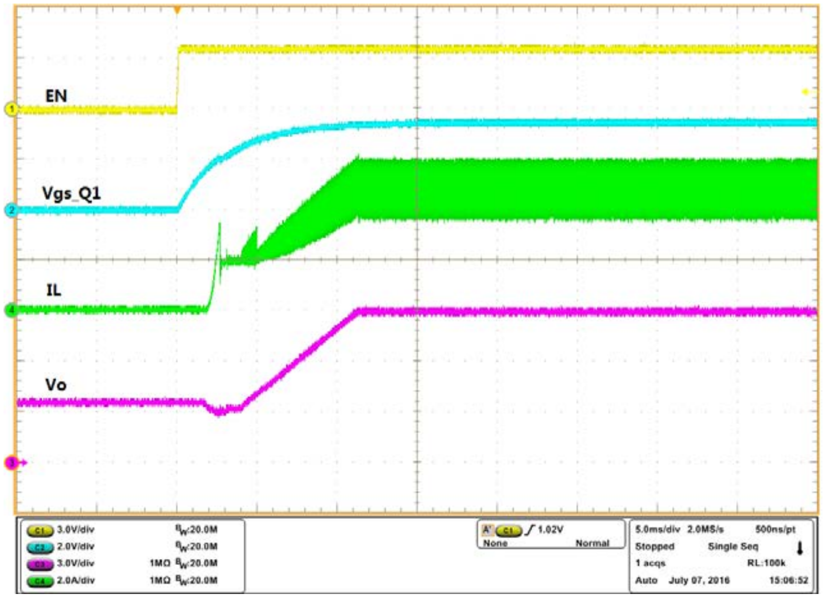

Figure 3. Startup Waveforms at V_{IN}=3.6V (V_O = 9V, I_O = 2A)

4.2 Short Circuit Protection Waveforms

Figure 4 shows the output short circuit protection performance at V_O=5 V condition. From the waveforms of the Q1's gate drive signal V_{gs_Q1} and the output current I_O, we can see that the TPS61088 can be disconnected from the load within 5 us in the output short circuit condition.

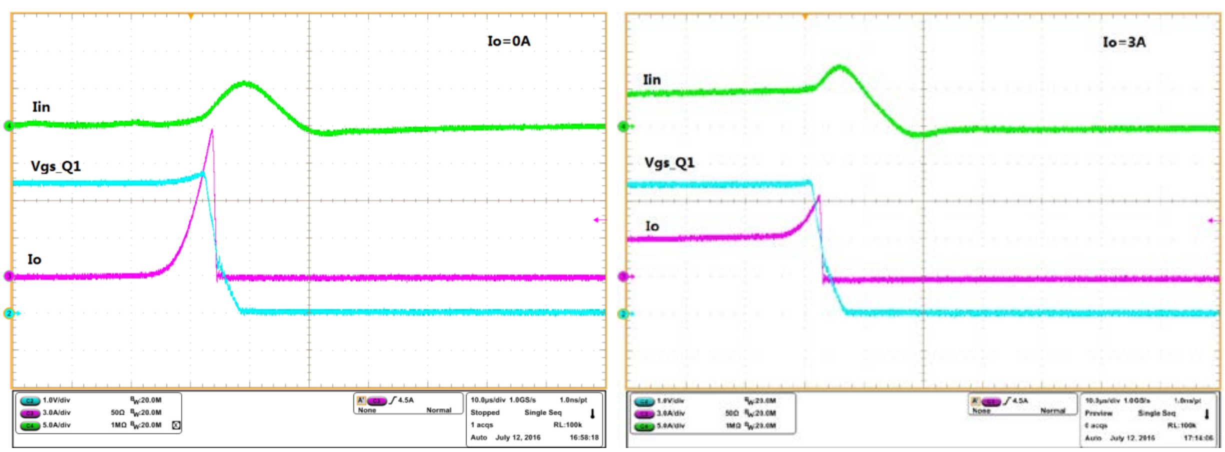

Figure 4. Output Short Circuit Performance at V_O=5V (V_{IN} = 3.6V)

Figure 5 shows the output short circuit protection performance at V_O=9 V condition. From the waveforms of the Q1's gate drive signal V_{gs_Q1} and the output current I_O, we can see that the TPS61088 can be disconnected from the load within 5 us in the output short circuit condition.

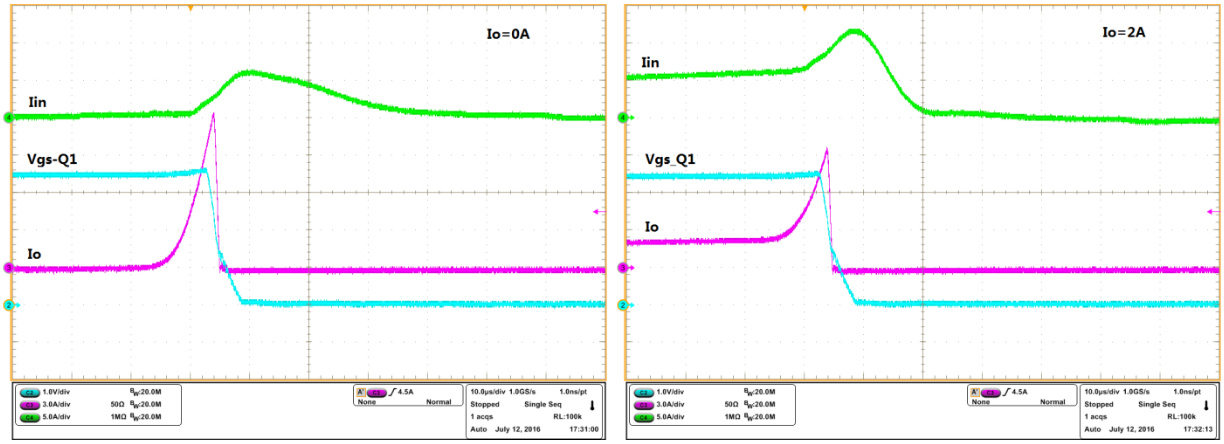

Figure 5. Output Short Circuit Performance at V_O=9V (V_{IN} = 3.6V)

Figure 6 shows the output short circuit protection performance at V_O=12 V condition. From the waveforms of the Q1's gate drive signal V_{gs_Q1} and the output current I_O, we can see that the TPS61088 can be disconnected from the load within 5 us in the output short circuit condition.

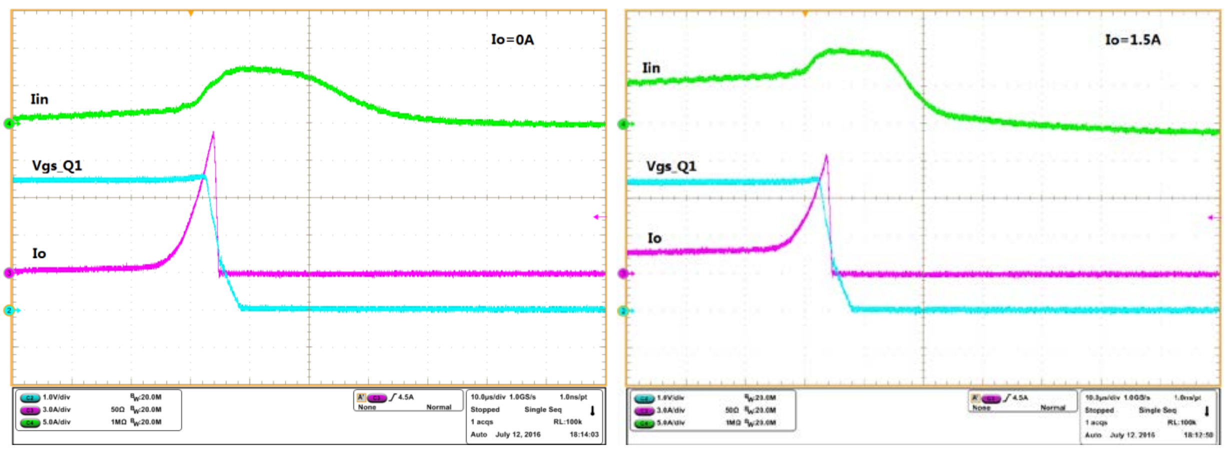

Figure 6. Output Short Circuit Performance at V_O=12V (V_{IN} = 3.6V)

5 Schematic, Bill of Materials and PCB Layout

This section provides the PMP9779 schematic, bill of materials (BOM) and board layout.

5.1 Schematic

Figure 7 illustrates the schematic of this reference design.

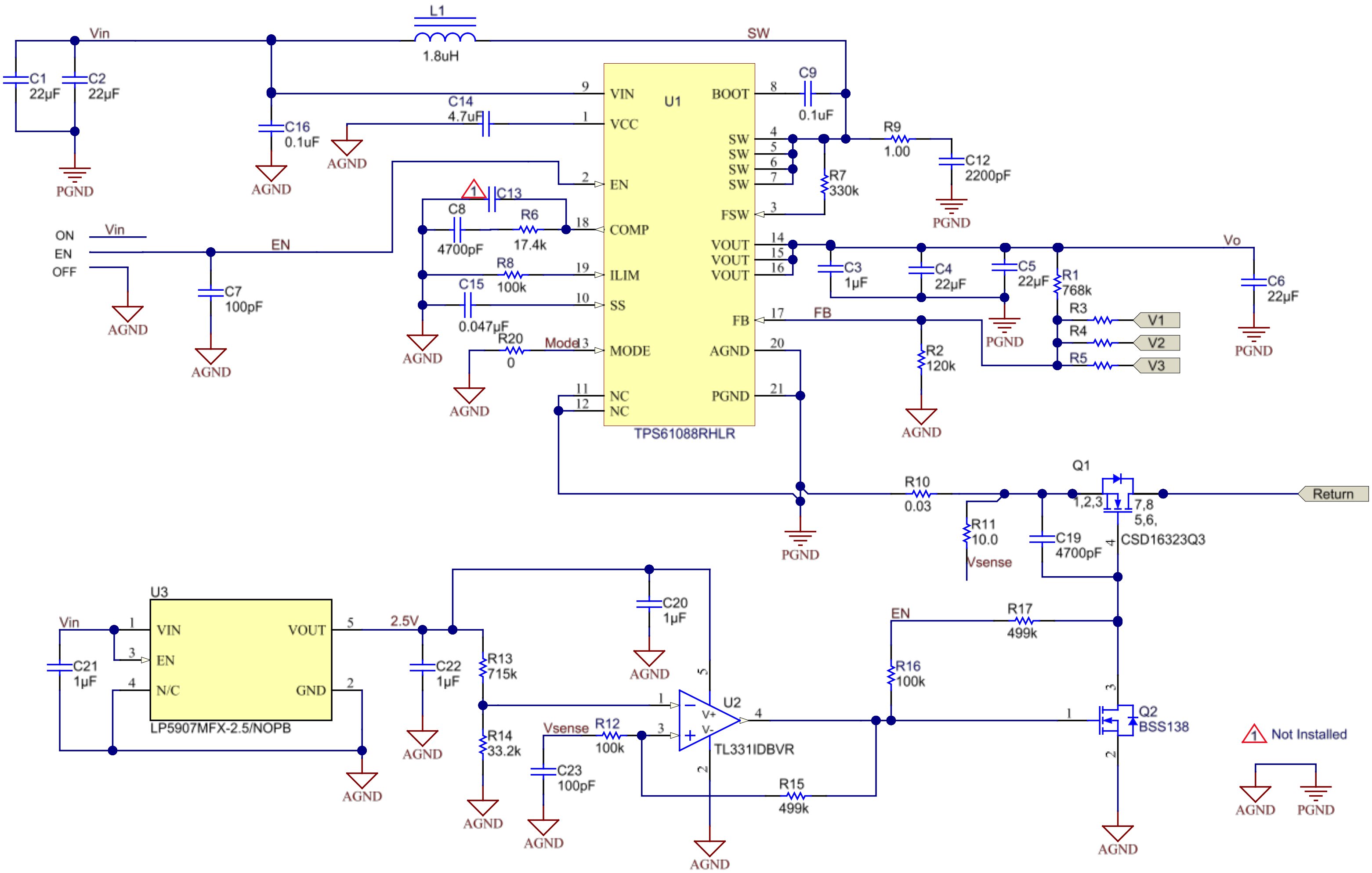

Figure 7. PMP9779 Schematic

5.2 Bill of Materials

Table 2 displays the PMP9779 bill of materials.

Table 2. PMP9779 Bill of Materials

Designator	QTY	Value	Description	Package	Part Number	MFG
C1, C2, C4, C5, C6	5	22uF	CAP, CERM, 22 µF, 16 V, +/- 10%, X5R, 1206	1206	GRM31CR61C226KE15L	MuRata
C3	1	1uF	CAP, CERM, 1 µF, 25 V, +/- 10%, X7R, 0603	0603	GRM188R71E105KA12D	MuRata
C7, C23	2	100pF	CAP, CERM, 100 pF, 50 V, +/- 1%, C0G/NP0, 0402	0402	GRM1555C1H101FA01D	MuRata
C8	1	4700pF	CAP, CERM, 4700 pF, 50 V, +/- 10%, X5R, 0402	0402	GRM155R61H472KA01D	MuRata
C9, C16	2	0.1uF	CAP, CERM, 0.1uF, 16V, +/-10%, X5R, 0402	0402	GRM155R61C104KA88D	MuRata
C12	1	2200pF	CAP, CERM, 2200 pF, 50 V, +/- 5%, C0G/NP0, 0603	0603	GRM1885C1H222JA01D	MuRata
C14	1	4.7uF	CAP, CERM, 4.7uF, 10V, +/-10%, X5R, 0603	0603	0603ZD475KAT2A	AVX
C15	1	0.047uF	CAP, CERM, 0.047 µF, 16 V, +/- 10%, X7R, 0402	0402	GRM155R71C473KA01D	MuRata
C19	1	4700pF	CAP, CERM, 4700 pF, 25 V, +/- 10%, X7R, 0603	0603	GRM188R71E472KA01D	MuRata
C20, C21, C22	3	1uF	CAP, CERM, 1 µF, 25 V, +/- 10%, X5R, 0402	0402	GRM155R61E105KA12D	MuRata
L1	1	1.8uH	Inductor, Shielded Drum Core, Metal Composite, 1.2 µH, 12.9 A, 0.007 ohm, SMD	9.5x8.7mm	CDMC8D28NP-1R2MC	Sumida
Q1	1	25V	MOSFET, N-CH, 25 V, 60 A, SON 3.3x3.3mm	SON 3.3x3.3mm	CSD16323Q3	Texas Instruments
Q2	1	50V	MOSFET, N-CH, 50 V, 0.22 A, SOT-23	SOT-23	BSS138	Fairchild Semiconductor
R1	1	768k	RES, 768 k, 1%, 0.063 W, 0402	0402	CRCW0402768KFKED	Vishay-Dale
R2	3	120k	RES, 120 k, 1%, 0.063 W, 0402	0402	CRCW0402120KFKED	Vishay-Dale
R8, R12, R16	4	100k	RES, 100k ohm, 1%, 0.063W, 0402	0402	CRCW0402100KFKED	Vishay-Dale
R6	1	17.4k	RES, 17.4k ohm, 1%, 0.063W, 0402	0402	CRCW040217K4FKED	Vishay-Dale
R7	1	330k	RES, 330 k, 5%, 0.063 W, 0402	0402	CRCW0402330KJNED	Vishay-Dale
R10	1	0.03	RES, 0.03, 1%, 1 W, 2010	2010	CSRN2010FK30L0	Stackpole Electronics Inc
R11	1	10.0	RES, 10.0, 1%, 0.063 W, 0402	0402	CRCW040210R0FKED	Vishay-Dale
R13	1	715k	RES, 715 k, 1%, 0.063 W, 0402	0402	CRCW0402715KFKED	Vishay-Dale
R14	1	33.2k	RES, 33.2 k, 1%, 0.063 W, 0402	0402	CRCW040233K2FKED	Vishay-Dale
R15	1	499k	RES, 499 k, 1%, 0.063 W, 0402	0402	CRCW0402499KFKED	Vishay-Dale
R17	1	499k	RES, 499 k, 1%, 0.063 W, 0402	0402	CRCW0402499KFKED	Vishay-Dale
R20	1	0	RES, 0, 5%, 0.063 W, 0402	0402	RC0402JR-070RL	Yageo America
U1	1		13.2-V Output, Synchronous Boost Converter with 10-A Switch, RHL0020A	RHL0020A	TPS61088RHLR	Texas Instruments
U2	1		SINGLE DIFFERENTIAL COMPARATOR, DBV0005A	DBV0005A	TL331IDBVR	Texas Instruments
U3	1		ULTRA LOW-NOISE, 250-mA LINEAR REGULATOR FOR RF AND ANALOG CIRCUITS REQUIRES NO BYPASS CAPACITOR, DBV0005A	DBV0005A	LP5907MFX-2.5/NOPB	Texas Instruments
C13	0	47pF	CAP, CERM, 47 pF, 50 V, +/- 1%, C0G, 0402	0402	GRM1555C1H470FA01D	MuRata
R9	0	1.00	RES, 1.00, 1%, 0.125 W, 0805	0805	CRCW08051R00FKEA	Vishay-Dale

5.3 PCB Layout

Figure 8 through Figure 13 show the PMP9779 PCB layout.

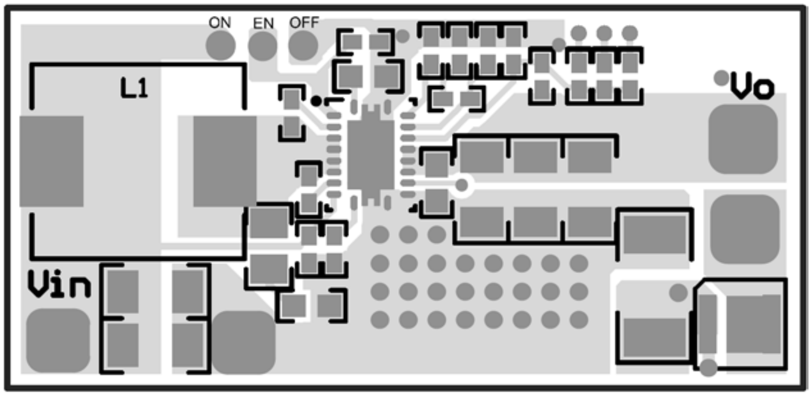

Figure 8. PMP9779 Top Layer and Top Silkscreen

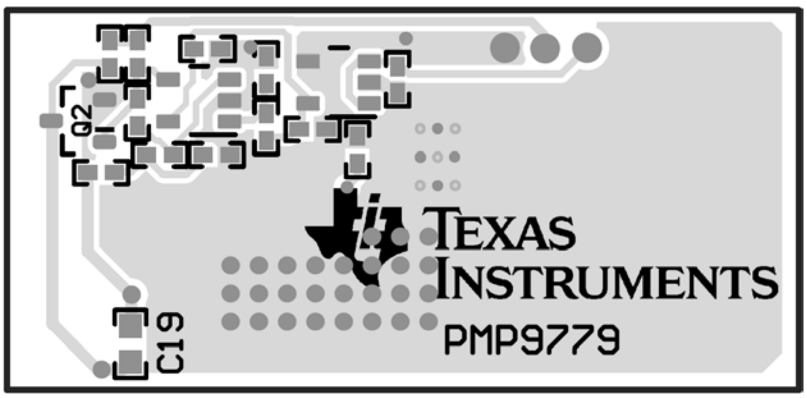

Figure 9. PMP9779 Bottom Layer and Bottom Silkscreen

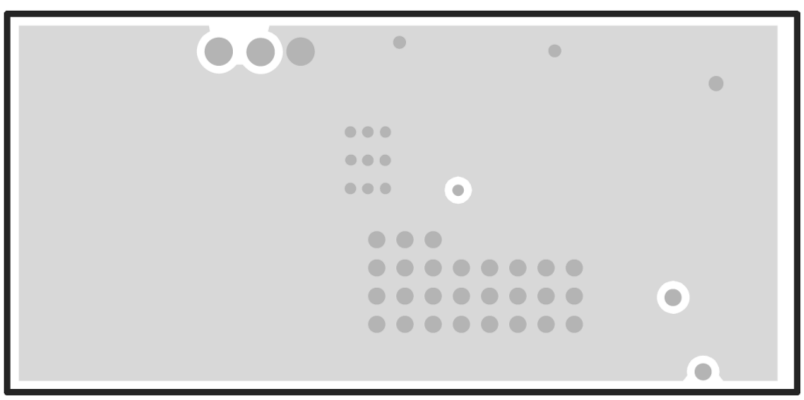

Figure 10. PMP9779 Internal Layer 1

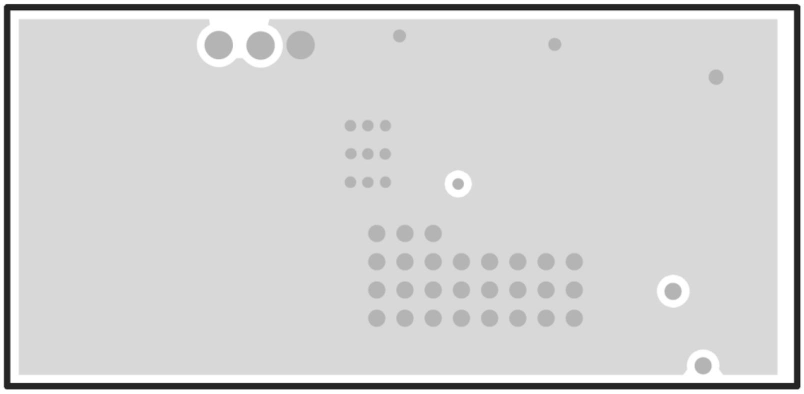

Figure 11. PMP9779 Internal Layer 2

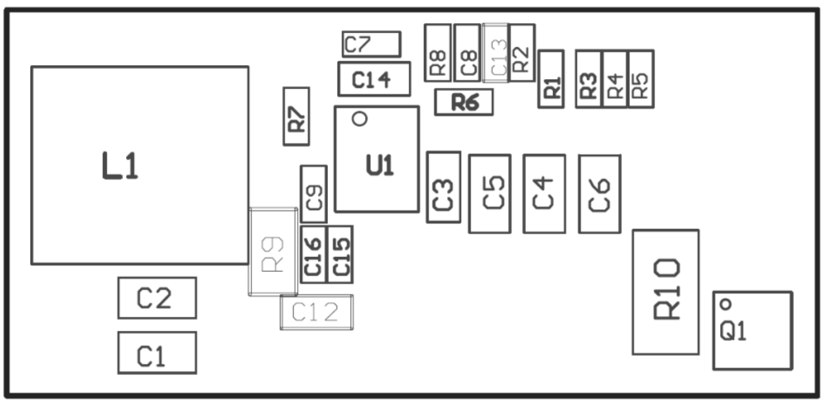

Figure 12. PMP9779 Top-side Assembly Drawing

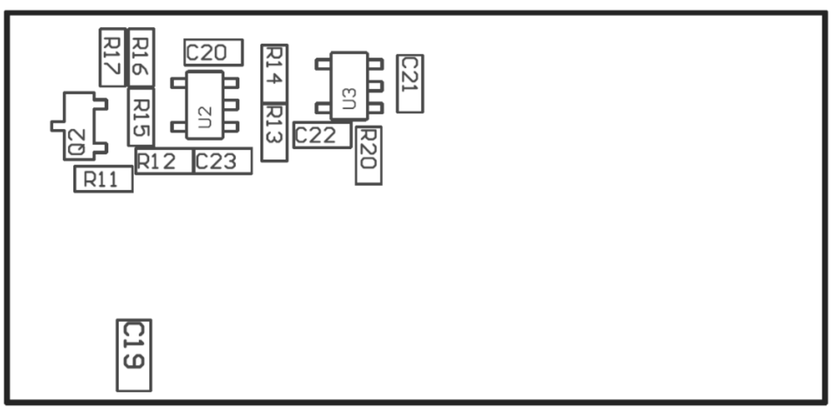

Figure 13. PMP9779 Bottom-side Assembly Drawing

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