**Description**

This parallel LDO reference design showcases the TPS7A85 low-noise, low-dropout linear regulator (LDO) in a parallel configuration, which is capable of sourcing 3.5 A per LDO or 7 A per board. Additional design flexibility includes the ability to stack this design to meet the current requirements of an application.

**Features**

- Output Current: Up to 7 A per Board (Two TPS7A85 LDOs per Board)
- Low Dropout Voltage: 200 mV (Typical)
- Low Noise Output: 3.33 μVRMS (10 Hz to 100 kHz for One LDO) When Paralleling Eight LDOs
- High Output Accuracy: 1% (Over Line, Load, and Temperature)

**Applications**

- Powering FPGAs and DSPs
- Post DC-DC Power Filtering
- Servers

**Resources**

- TIDA-01232 Design Folder
- TPS7A85 Product Folder

---

An IMPORTANT NOTICE at the end of this TI reference design addresses authorized use, intellectual property matters and other important disclaimers and information.
1 System Description

Low-noise low-dropout regulators (LDO) are required in many applications to ensure that power supply noise does not couple into the signal chain. The requirements for current continue to increase as new high-speed analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and clocking circuitry increase data speed and bandwidth. Using a single LDO for the supply is not always possible due to device availability and power dissipation limitations. The TIDA-01232 reference design solves this issue by using multiple LDOs configured to share current in parallel. The current sharing is achieved by using a single low-value ballast resistor, which can be designed as a copper trace on the resistor of a printed-circuit board (PCB).

This circuit uses the high-current LDO, TPS7A85, which is a 4-A device. Every board is populated with two TPS7A85 devices and can provide up to 7 A of current. The boards are designed so that multiple boards can be stacked on top of each other. For example, if a second board is stacked on top of the first board, the solution can provide up to 14 A.

1.1 Key System Specifications

Table 1. Key System Specifications

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SPECIFICATIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input power rail, $V_{IN}$</td>
<td>$V_{OUT} + 200$ mV (typical)</td>
</tr>
<tr>
<td>Bias power rail $^{(1)}$, $V_{BIAS}$</td>
<td>3.0 V to 6.5 V</td>
</tr>
<tr>
<td>Maximum output current, $I_{OUT}$</td>
<td>3.5 A multiplied by the number of LDOs (7 A per board)</td>
</tr>
<tr>
<td>Output voltage range, $V_{OUT}$</td>
<td>0.8 V to 3.95 V (using ANY-OUT™)</td>
</tr>
<tr>
<td>Optimized for output Voltage, $V_{OUT}$</td>
<td>0.8 V</td>
</tr>
<tr>
<td>Ballast resistor, $R_{BALLAST}$</td>
<td>5 mΩ</td>
</tr>
<tr>
<td>Maximum voltage drop across ballast resistor $^{(2)}$, $V_{BALLAST}$</td>
<td>20 mV</td>
</tr>
</tbody>
</table>

$^{(1)}$ Required for $V_{IN} < 1.4$ V, recommended for $V_{IN} < 2.2$ V for best dropout.

$^{(2)}$ The delta between $V_{NOMINAL}$ to $V_{OUT}$ is greater due to the resistance from the connectors in between the boards.
2 System Overview

2.1 Block Diagram

Figure 1. Two LDOs With Ballast Resistors
2.2 Design Considerations

2.2.1 Theory of Operation

2.2.1.1 Ballast Resistor

This solution uses ballast resistors. Ballast resistors provide an easy way to connect multiple voltage sources together to supply power to a common load. Critical for this method is to minimize the voltage difference at the output of each individual LDO. As LDO accuracy improves, the designer can reduce the size of the ballast resistor.

Every LDO has its own voltage reference and each independent reference is slightly different from every other independent reference; therefore, to achieve the smallest possible error, this solution connects these voltages together through the NR/SS pin. The remaining error sources are the feedback resistor network, the ballast resistor, the internal output field-effect transistor (FET), and the amplifier. Section 2.2.2 and Section 3.1.1 provide further detail on how this solution minimizes sources of error.

The following formulas in Equation 1 and Equation 2 are used to size the ballast resistor:

\[ E_{V_{out}} = E_{V_{ref}} + 2 \times (1 - \frac{V_{ref}}{V_{outNom}}) \times E_{R_{fb}} \]  
\[ (1) \]

where,
- \( E_{V_{out}} \) is the maximum expected error of the LDO output,
- \( E_{V_{ref}} \) is the maximum expected error of the LDO internal reference,
- \( V_{ref} \) is the reference voltage of the LDO,
- \( E_{R_{fb}} \) is the maximum expected error of the feedback resistors.

\[ R_{Ballast} = \frac{V_{outNom} \times (2 \times E_{V_{out}})}{2 \times I_{outMaxSingle} - I_{outMaxTotal}} \]  
\[ (2) \]

where,
- \( R_{Ballast} \) is the ballast resistor,
- \( V_{outNom} \) is the nominal LDO output,
- \( E_{V_{out}} \) is the maximum expected error of the LDO output,
- \( I_{outMaxSingle} \) is the current limit of a single LDO,
- \( I_{outMaxTotal} \) is the maximum current of the system.

Minimize the error and the ballast resistor by using the same LDO (TPS7A85) for each of the LDOs paralleled. To further reduce the error, chose an LDO that has the NR/SS voltage (reference voltage) routed to a pin.

Use the following formula in Equation 3 to determine if the output of this solution delivers a high enough voltage:

\[ V_{outTotMin} = V_{outNom} \times (1 - E_{V_{out}} - \frac{I_{outMaxTotal}}{n}) \times R_{Ballast} \times (1 + E_{R_{ballast}}) \]  
\[ (3) \]

where,
- \( V_{outTotMin} \) is the minimum output of the solution (voltage at load) \(^{(2)}\),
- \( V_{outNom} \) is the nominal LDO output,
- \( E_{V_{out}} \) is the maximum expected error of the LDO output,
- \( I_{outMaxTotal} \) is the maximum current of the system,
- \( R_{Ballast} \) is the ballast resistor,
- \( E_{R_{ballast}} \) is the maximum expected error due to the ballast resistor tolerance,
- \( n \) is the number of parallel LDOs.

\(^{(1)}\) \( V_{ref} \) is equal to \( V_{FB} \)

\(^{(2)}\) This formula applies to an ideal solution meaning that there are no other resistance elements on the current path, such as a via.
Designers may be tempted to move the point where the feedback is connected to the output after the ballast resistor and let the LDO regulate this voltage. The issue here is that the effect of the ballast the resistor would be eliminated and the LDOs would no longer share the load current.

When the resistor is defined for two LDOs, the same resistor must be used to add additional LDOs. As long as the LDOs are the same, the biggest output difference does not change; therefore, the ballast resistor remains the same.

2.2.2 Component Selection

2.2.2.1 LDO Selection

The criteria for the LDO is as follows:

- High accuracy output
- ANY-OUT™ feedback resistors
- High current
- NR/SS pin

ANY-OUT™ feedback resistors provide an advantage in accuracy over traditional adjustable LDOs with external resistor networks. Traditionally, external resistor dividers are not included in the accuracy specification of an LDO. ANY-OUT™ feedback resistors are internal to the LDO and are matched so that the ratio of the resistor divider is accurate. This matching allows the ANY-OUT™ feedback resistors to be included in the overall accuracy specification of the LDO, which makes a 1% LDO with ANY-OUT™ more accurate than a traditional 1% adjustable LDO with external feedback resistors.

The NR/SS pin allows for minimizing the error of the voltage reference, which narrows down the range of the outputs between the LDOs. Section 3.1.1 provides additional information.

The 4-A, high-precision LDO TPS7A85 meets the criteria, which is the reason it has been chosen for this design.

2.2.3 Connector Selection

The PCB was designed to be stacked upon itself, which is achieved by using 100-mil connectors.

The parts listed in Table 2 are used for this reference design:

<table>
<thead>
<tr>
<th>FUNCTION</th>
<th>PART NUMBER</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output</td>
<td>SSQ-104-03-G-D</td>
</tr>
<tr>
<td>ANY-OUT™</td>
<td>SSQ-106-03-G-D</td>
</tr>
<tr>
<td>GND, NR/SS</td>
<td>SSQ-102-03-G-S</td>
</tr>
</tbody>
</table>

2.2.4 Capacitor Selection

This reference design uses local capacitors for the input (C1 through C4, C13 through C16), local output capacitors (C7, C18), feed forward capacitors (C6, C17), as well as global output capacitors (C9 through C12). TI advises to follow the recommendations of the data sheet for capacitor selection. Designers can typically find this information in the “Application and Implementation” sections of data sheets.

(1) Capacitor designators refer to the Schematics.
(2) Capacitors C1, C9, and C13 were not populated.
2.3 Highlighted Products

2.3.1 TPS7A85

The TPS7A85 is a low-noise (4.4 µVRMS), low-dropout linear regulator (LDO) capable of sourcing 4 A with only 240 mV of maximum dropout. The device output voltage is pin-programmable from 0.8 V to 3.95 V and adjustable from 0.8 V to 5.0 V using an external resistor divider.

The combination of low-noise (4.4 µVRMS), high power supply rejection ratio (PSRR), and high output current capability makes the TPS7A85 ideal to power noise-sensitive components such as those used in high-speed communications, video, medical, or test and measurement applications. The high performance of the TPS7A85 limits power-supply-generated phase noise and clock jitter, which make this device ideal for powering high-performance serializer and deserializer (SerDes), ADCs, DACs, and RF components. RF amplifiers specifically benefit from the high performance and 5.0-V output capability of the device.

The exceptional accuracy (1% over line, load, and temperature), remote sensing, excellent transient performance, and soft-start capabilities of the TPS7A85 ensure optimal system performance for digital loads that require low-input voltage, low-output (LILO) voltage operation, such as application-specific integrated circuits (ASICs), field-programmable gate arrays (FPGAs), and digital signal processors (DSPs).

The versatility of the TPS7A85 makes it a popular choice for many demanding applications.
3 Hardware, Testing Requirements, and Test Results

3.1 Hardware

3.1.1 Ballast Resistor Implementation

This subsection serves as a guideline for designing a PCB ballast resistor. Section 2.2.1.1 describes the formulas used.

Because no target \( V_{\text{outMin}} \) has been established for this design, the iterative part to reach a target voltage can be skipped.

For this calculation \( V_{\text{outNom}} = 0.8 \text{ V} \), which results in the following \( E_V \) in Equation 4:

\[
E_V = E_{\text{Vref}} + 2 \times \left( 1 - \frac{V_{\text{out}}}{V_{\text{outNom}}} \right) \times E_{\text{Rfb}} = \left( V_{\text{outNom}} \times 1\% \right) + 2 \times \left( 1 - \frac{0.8 \text{ V}}{V_{\text{outNom}}} \right) \times E_{\text{Rfb}} = \left( V_{\text{outNom}} \times 1\% \right) + 2 \times \left( 1 - 1 \right) \times E_{\text{Rfb}} = 0.8 \text{ V} \times 0.01 = 8 \text{ mV}
\]

(4)

The error of 8 mV is specified for a single LDO over the full temperature range including the tolerance of the voltage reference as well as the tolerance of the internal feedback resistors, amplifier, and FET. For this reference design, the NR/SS pins are shorted together; therefore, the voltage references of each individual LDO are also shorted to each other. As such, the accuracy of the output remains 1% but the voltage difference between the individual LDOs will be closer to each other.

Measurements prove that the \( V_{\text{OUT}} \) of the LDOs with the same \( V_{\text{REF}} \) are closer to each other than the calculated 8 mV. Figure 2 shows such a measurement. For example, if the \( V_{\text{NR/SS}} \) is in the blue range, \( V_{\text{OUT}} \) is most likely to fall within the blue marked range of the upper histogram. The same principle applies to the range marked in red. By connecting these two reference voltages together, the \( V_{\text{REF}} \) at the error amplifier input will be somewhere in between these two voltages. The movement of \( V_{\text{REF}} \) also influences the output and moves the range in between the two marked ranges.

Figure 2. Histogram of \( V_{\text{NR/SS}} \) Compared to \( V_{\text{OUT}} \)
After testing various NR/SS voltages at $V_{outNom} = 0.8$ V, the typical range of $V_{OUT}$ for each $V_{NR/SS}$ pin did not surpass 1.5 mV, which would otherwise result in an $E_{Vout}$ of ±0.75 mV.

Using this output range means that the following ballast resistor would be required:

$$R_{Ballast} = \frac{V_{outNom} \times (2 \times E_{Vout})}{2 \times I_{outMaxSingle} - I_{outMaxTotal}} = \frac{0.8 \text{ V} \times 2 \times 0.75 \text{ mV}}{2 \times 4 \text{ A} - 7.5 \text{ A}} = 2.4 \text{ mO}$$

(5)

For some additional margin and to be able to change the $V_{outNom}$ up to 1.6 V, this value is set to 5 mΩ.

Choosing $I_{outMaxTotal} = 7.5 \text{ A}$ is an iterative procedure for evaluating the size and length of the PCB resistor.

After defining the value for the ballast resistor, the next step is to design the PCB trace dimensions to match this resistive value. Equation 6 shows how to calculate the resistance of a PCB trace:

$$R = \frac{I \times \rho}{A \times (1 + \alpha \times (T_A - T_0))}$$

(6)

where,

- $R$ is the trace resistor of the PCB in Ω,
- $I$ is the length of the trace in meters,
- $\rho$ is the resistivity in Ω meters $\rho_{copper} = 16.8 \times 10^{-9}$ Ωm,
- $A$ is the vertical area of trace in square meters,
- $\alpha$ is the temperature coefficient in °C$^{-1}$ $\alpha_{copper} = 3.9 \times 10^{-3}$°C$^{-1}$,
- $T$ is the ambient temperature $T_0 = 25$°C.

Figure 3 shows the PCB trace dimensions.

![Figure 3. PCB Trace Dimensions](image)

Use the diagrams of the trace resistance as a function of the trace width to find a reasonable length versus width ratio. The temperature is considered as well and added to the individual plots to avoid burning the trace (see Figure 4).

![Figure 4. 400-mil Length PCB Trace Width versus Trace Resistance (Ω)](image)
Equation 7 shows the formula for the temperature per IPC-2221:

$$
\Delta T = \left(\frac{I}{k \times A^c}\right)^\frac{1}{b}
$$

(7)

where,

• $\Delta T$ is the temperature difference,
• $I$ is the current through the trace,
• $A$ is the vertical area of trace in square mil,
• $b$ is 0.44,
• $c$ is 0.725,
• $k$ is 0.024 for an internal PCB layer and 0.048 for an external PCB layer.

Figure 4 shows that with a trace width of 19 mil, a length of 400 mil and a thickness of 2 oz should match the desired 5 mΩ. The following calculations of the trace and temperature reinforce the findings of this plot:

$$
R = \frac{I \times \rho}{A \times (1 + \alpha \times (T_A - T_0))} = \frac{(400 \text{ mil} \times 2.54 \times 10^{-5} \text{ (m/mil)}) \times (1.68 \times 10^{-8} \text{ Ωm})}{((2.8 \times 19) \text{ mil}^2 \times 6.45 \times 10^{-10} \text{ (m/mil)^2}) \times (1 + \frac{3.9 \times 10^{-3} \text{ °C}}{\text{ °C}} \times (25 - 25) \text{ °C})}
$$

(8)

$$
\Delta T_{4A} = \left(\frac{I}{k \times A^c}\right)^\frac{1}{b} = \left(\frac{4 \text{ A}}{0.048 \times (2.8 \text{ mil} \times 19 \text{ mil})^{0.725}}\right)^\frac{1}{0.44} = 33.2 \text{ °C}
$$

(9)

$$
\Delta T_{4A} = \left(\frac{I}{k \times A^c}\right)^\frac{1}{b} = \left(\frac{3.5 \text{ A}}{0.048 \times (2.8 \text{ mil} \times 19 \text{ mil})^{0.725}}\right)^\frac{1}{0.44} = 24.5 \text{ °C}
$$

(10)

Per the calculations, with a 2-oz (2.8-mil) thick copper trace at ambient temperature (25°C), the trace should have a 19-mil width and 400-mil length to reach the desired 5-mΩ ballast resistor.
3.2 Testing and Results

3.2.1 Test Setup

The scope shots in this section show the typical values. The boards are powered by $V_{\text{IN}} = 1.1\, \text{V}$, $V_{\text{BIAS}} = 4.5\, \text{V}$ unless otherwise noted. The power supply used for $V_{\text{IN}}$ was the Chroma 62006P-100-25. The scope shots were taken with the LeCroy WaveSurfer 454. Each board has two LDOs in parallel. Multiples of two LDOs are added by stacking boards: four LDOs is two boards stacked, six LDOs is three boards stacked, and so forth.

3.2.2 Test Results

3.2.2.1 Start-Up

For the following scope shots blue is $V_{\text{IN}}$, green is $V_{\text{OUT}}$, red is $I_{\text{IN}}$, and magenta is $V_{\text{EN}}$.

The following scope shots are for two LDOs (one board).

Figure 5. Start-up—Two LDOs, 6 A

Figure 6. Start-up—Two LDOs, 6 A (Zoomed in)

Figure 7. Shutdown—Two LDOs, 6 A
The following scope shots are for six LDOs (three boards).

Figure 8. Start-up—Six LDOs, No Load

Figure 9. Start-up—Six LDOs, 6 A

Figure 10. Start-up—Six LDOs, 24 A

Figure 11. Start-up—Six LDOs, 24 A (Zoomed in)

Figure 12. Shutdown—Six LDOs, 24 A
If the system is started into a full load, TI recommends to first establish $V_{\text{BIAS}}$ and $V_{\text{IN}}$ and then turn the devices ON using the enable pin. Use a supervisor or a microcontroller to perform this action. The reason for these steps is to relieve the supply and avoid the high load drop $V_{\text{IN}}$ under $V_{\text{UVLO}} - V_{\text{HYS}}$, which causes the LDOs to shut down again. The ringing at the falling edges is caused by the inductance of the load (in this case a 1-m long cable) and the inductance of the cable connecting the boards to the power supply. If $V_{\text{IN}}$ spikes higher than $V_{\text{UVLO}}$ while shutting down, the LDOs may try to power up again.

![Enable Start-up—Six LDOs, 24 A](image1)

![Enable Shutdown—Six LDOs, 24 A](image2)

![Enable Start-up—No Load](image3)

### 3.2.2.2 Noise

The following graphs show the noise performance of two, four, and eight parallel LDOs. A resistive load of 0.123 $\Omega$ is used for all three examples, which results in a total current load of approximately 6.5 A when the output is set to 0.8 V.

The two main considerations for these graphs are as follows: First, the peaks on the upper end of the frequency are a result of the internal charge pump of the LDO. See the subsection regarding charge pump noise in *TPS7A85 High-Current (4 A), High-Accuracy (1%), Low-Noise (4.4 $\mu$VRMS), LDO Voltage Regulator* for further details[3]. Second, the noise keeps decreasing for each LDO added in parallel, which is similar to when amplifiers are set in parallel. By paralleling amplifiers, the noise can be improved by the ratio of $\sqrt{2}$ for each time the number of amplifiers is doubled.
Figure 16. Output Noise—One LDO (Noise $_{10 \text{ Hz} - 100 \text{ kHz}} = 7.69 \mu V_{\text{RMS}}$)

Figure 17. Output Noise—Two Parallel LDOs (Noise $_{10 \text{ Hz} - 100 \text{ kHz}} = 5.98 \mu V_{\text{RMS}}$)

Figure 18. Output Noise—Four Parallel LDOs (Noise $_{10 \text{ Hz} - 100 \text{ kHz}} = 4.32 \mu V_{\text{RMS}}$)

Figure 19. Output Noise—Eight Parallel LDOs (Noise $_{10 \text{ Hz} - 100 \text{ kHz}} = 3.33 \mu V_{\text{RMS}}$)

Figure 20. Output Noise
3.2.2.3 Sharing Performance

For the error plot, the board (or boards) with the worst sharing performance were selected to show the worst case.

The following graphs have two LDOs (one board).

![Graph 1: Sharing Board 1](image1)

![Graph 2: Sharing Board 2](image2)

![Graph 3: Sharing Board 3](image3)

![Graph 4: Sharing Board 4](image4)

![Graph 5: Sharing Error Board 3](image5)
The following error plots have four LDOs (two boards in parallel).

Figure 26. Sharing Boards 1 and 2

Figure 27. Sharing Boards 1 and 3

Figure 28. Sharing Boards 1 and 4

Figure 29. Sharing Boards 2 and 3

Figure 30. Sharing Boards 2 and 4

Figure 31. Sharing Boards 3 and 4
The following error plots have six LDOs (three boards in parallel).
### 3.2.2.4 Load Transients

The following scope shots show the load transient with $I_{OUT\_MAX} = 23$ A in red and $V_{OUT}$ in blue. The difference between input GND and output GND was subtracted from $V_{OUT}$ to reduce the GND bounce at the output of the system. Note that three boards in parallel = six LDOs.

The ringing on Figure 37 results from the inductance in the cables. Expect this ringing to be much flatter or even disappear if the load is on the same PCB as the LDOs.

![Figure 36. Load Transient 0 A to 23 A](image)

![Figure 37. Load Transient 23 A to 0 A](image)

![Figure 38. Load Transient 23 A](image)

### 3.2.3 Comparison to TIDU421

Table 3 shows a quick overview comparing two reference designs: TIDA-01232 and TIDU421. In summary, TI recommends the TIDA-01232 reference design if a very-high-current, low-noise voltage source is required and the TIDU421 reference design if high accuracy at the output is required.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TIDA-01232</th>
<th>TIDU421</th>
</tr>
</thead>
<tbody>
<tr>
<td>LDOs parallel</td>
<td>Tested up to eight</td>
<td>Designed for two LDOs</td>
</tr>
<tr>
<td>Load regulations</td>
<td>Voltage drop over ballast resistor</td>
<td>Direct load regulation</td>
</tr>
<tr>
<td>Additional components</td>
<td>PCB resistance</td>
<td>Amplifier and shunt</td>
</tr>
<tr>
<td>Maximum tested current</td>
<td>23 A (six LDOs)</td>
<td>6 A (two LDOs)</td>
</tr>
</tbody>
</table>
4 Design Files

4.1 Schematics
To download the schematics, see the design files at TIDA-01232.

4.2 Bill of Materials
To download the bill of materials (BOM), see the design files at TIDA-01232.

4.3 PCB Layout Recommendations
The available PCB design files correspond to “Rev B” of the schematics and layout. The changes to “Rev A” are as follows:
• The PCB ballast resistor has been changed from a longer, multi-layer design to a shorter single-layer design. The resistance of the PCB trace has not been changed and remains at 5 mΩ.
• The BIAS, VIN, and GND test points have been moved to the edge of the board for easier access when boards are stacked together.
• Zener diodes have been added to clamp input as well as output voltages to prevent damaging the device due to voltage peaks generated by the high currents and the inductance of the cables. Zener diodes have also been used and populated in “Rev A”.
• Minor changes have been made on the silkscreen

4.3.1 Layout Prints
To download the layer plots, see the design files at TIDA-01232.

4.4 Altium Project
To download the Altium project files, see the design files at TIDA-01232.

4.5 Gerber Files
To download the Gerber files, see the design files at TIDA-01232.

4.6 Assembly Drawings
To download the assembly drawings, see the design files at TIDA-01232.

5 Related Documentation
1. Texas Instruments, Ballast Resistors Allow Load Sharing Between Two Paralleled DC/DC Converters, Application Report (SLVA250)
2. Texas Instruments, TI Precision Designs: Verified Design 6A Current-Sharing Dual LDO, TI Precision Design (TIDU421)
3. Texas Instruments, TPS7A85 High-Current (4 A), High-Accuracy (1%), Low-Noise (4.4 μVRMS), LDO Voltage Regulator, TPS7A85 Data Sheet (SBVS267)

5.1 Trademarks
ANY-OUT is a trademark of Texas Instruments.

6 About the Author
NICOLÁS ROMÁN is an application engineer who did a rotation in a rotation in the Linear Power business unit. His final deployment will be as a field application engineer in the TI office in Zürich Switzerland. Nicolás graduated with a BSc FHO in Electrical Engineering at the HSR in Rapperswil, Switzerland (a University of applied science).
IMPORTANT NOTICE FOR TI DESIGN INFORMATION AND RESOURCES

Texas Instruments Incorporated ("TI") technical, application or other design advice, services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using any particular TI Resource in any way, you (individually or, if you are acting on behalf of a company, your company) agree to use it solely for this purpose and subject to the terms of this Notice.

TI’s provision of TI Resources does not expand or otherwise alter TI’s applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources.

You understand and agree that you remain responsible for using your independent analysis, evaluation and judgment in designing your applications and that you have full and exclusive responsibility to assure the safety of your applications and compliance of your applications (and of all TI products used in or for your applications) with all applicable regulations, laws and other applicable requirements. You represent that, with respect to your applications, you have all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. You agree that prior to using or distributing any applications that include TI products, you will thoroughly test such applications and the functionality of such TI products as used in such applications. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

You are authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT. AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED “AS IS” AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING TI RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY YOU AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

You agree to fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of your non-compliance with the terms and provisions of this Notice.

This Notice applies to TI Resources. Additional terms apply to the use and purchase of certain types of materials, TI products and services. These include: without limitation, TI’s standard terms for semiconductor products http://www.ti.com/sc/docs/stdterms.htm), evaluation modules, and samples (http://www.ti.com/sc/docs/sampterms.htm).

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2017, Texas Instruments Incorporated