TI Designs: TIDA-01457
3- to 11.5-V<sub>IN</sub>, –5-V<sub>OUT</sub>, 1.5-A Inverting Power Module Reference Design for Small, Low-Noise Systems

Description
This small and simple, low-noise inverting power module design (voltage inverter) cleanly supports a –5-V output voltage at up to 1.5 A of current from a 3- to 11.5-V input. Featuring TI's TPS82130 MicroSiP™ power module step-down converter in an inverting buck-boost topology, the design achieves a power density of 584 mW/mm<sup>3</sup> and a solution size of less than 50 mm<sup>2</sup>, allowing it to power sensitive analog loads in space-constrained, high-temperature communications equipment, such as optical modules. This design also supports many common industrial equipment, including those that require a 5-V input and –5-V output voltage inverter at up to 1 A.

Features
- Simple Power Module Design
- Total Solution Size Less Than 50 mm<sup>2</sup>
- High Output Current of 1.5 A (V<sub>IN</sub> ≥ 7.5 V)
- Wide Input Voltage Range of 3 to 11.5 V
- Low Noise (Less Than 10-mV Output Ripple)
- 125°C Rated Solution

Applications
- Optical Line Card
- Optical Modules
- Optical Networking: EPON
- Telecom Infrastructure: Remote Radio Unit (RRU)
- General Purpose Industrial

Resources
TIDA-01457 Design Folder
TPS82130 Product Folder

An IMPORTANT NOTICE at the end of this TI reference design addresses authorized use, intellectual property matters and other important disclaimers and information.
1 System Description

A negative voltage around –5 V is frequently required to bias the laser driver in an optical module and other communications equipment. This function requires several hundred milliamps of current and is powered from a 3.3-V source. This TI Design delivers an output current up to 600 mA at the lowest 3-V input voltage, which is a good match to the required output power and input voltage.

A negative voltage is also required in numerous industrial applications to bias operational amplifiers (op amps), programmable gain amplifiers (PGAs), and data converters (ADCs or DACs). In both applications, an integrated power module shortens the design time and enables a very-small solution size, while the low-output noise has a minimal effect on the actual signal.

1.1 Key System Specifications

Table 1. Key System Specifications

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SPECIFICATIONS</th>
<th>DETAILS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage range ($V_{IN}$)</td>
<td>3 to 11.5 V</td>
<td>—</td>
</tr>
<tr>
<td>Output voltage ($V_{OUT}$)</td>
<td>–5 V</td>
<td>—</td>
</tr>
<tr>
<td>Output current ($V_{IN} \geq 7.5$ V)</td>
<td>1.5 A</td>
<td>Figure 8</td>
</tr>
<tr>
<td>Output current ($V_{IN} = 5$ V)</td>
<td>1 A</td>
<td>Figure 8</td>
</tr>
<tr>
<td>Output current ($V_{IN} = 3$ V)</td>
<td>600 mA</td>
<td>Figure 8</td>
</tr>
</tbody>
</table>
2 System Overview

2.1 Block Diagram

![Block Diagram](image)

Figure 1. TIDA-01457 Block Diagram

2.2 Highlighted Products

2.2.1 TPS82130

The TPS82130 is a 3-A, step-down converter power module, which integrates the power inductor to achieve a very-small solution size and simple design. The power module accepts up to a 17-V input voltage from its input pin to ground pin. This wide input voltage range is ideally suited for an inverting converter, which, at a minimum, requires a voltage rating of the input voltage plus the output voltage.

2.3 Design Considerations

2.3.1 Inverting Buck-Boost Topology Concept

The inverting buck-boost topology is very similar to the buck topology. In the buck configuration that Figure 2 shows, the positive connection (V_OUT) is connected to the VOUT pin of the power module and the return connection is connected to the ground (GND) of the power module. However, in the inverting buck-boost configuration that Figure 3 shows, the power module ground is used as the negative output voltage pin (labeled as \(-V_{\text{OUT}}\)). The terminal formerly known as the positive output in the buck configuration is used as the ground. This inverting topology allows the output voltage to be inverted and always lower than the ground.

![Buck Topology](image)

Figure 2. TPS82130 Buck Topology
Figure 3. TPS82130 Inverting Buck-Boost Topology

The circuit operation is different in the inverting buck-boost topology than in the buck topology. Figure 4a shows that the output voltage terminals are reversed, though the components are wired the same as a buck converter. As Figure 4b shows, during the ON-time of the control MOSFET, the inductor is charged with current while the output capacitor supplies the load current. The inductor does not provide current to the load during this time. During the OFF-time of the control MOSFET and the ON-time of the synchronous MOSFET (see Figure 4c), the inductor provides current to the load and the output capacitor. These changes affect many parameters, which the following subsections describe in further detail.

Figure 4. Inverting Buck-Boost Configuration

The average inductor current is affected in this topology. In the buck configuration, the average inductor current is equal to the average output current because the inductor always supplies current to the load during both the ON- and OFF-times of the control MOSFET. However, in the inverting buck-boost configuration, only the output capacitor supplies the load with current, while the load is completely disconnected from the inductor during the ON-time of the control MOSFET. During the OFF-time, the inductor connects to both the output capacitor and the load (see Figure 4). Because the OFF-time is $1 - D$ of the switching period, the average inductor current in Equation 1 is calculated as:

$$I_{L(Avg)} = \frac{I_{OUT}}{1 - D}$$

(1)

The duty cycle for the typical buck converter is simply $V_{OUT} / V_{IN}$, but the calculation of the duty cycle in Equation 2 for an inverting buck-boost converter becomes:

$$D = \frac{V_{OUT}}{V_{OUT} - V_{IN}}$$

(2)
Equation 3 provides the peak-to-peak inductor ripple current:

\[
\Delta I_L = \frac{V_{IN}D}{f_sL}
\]

where:
- \(\Delta I_L\) (A): Peak-to-peak inductor ripple current
- \(D\): Duty cycle
- \(f_s\) (MHz): Switching frequency
- \(L\) (µH): Inductor value of typically 1 µH
- \(V_{IN}\) (V): Input voltage with respect to ground, not with respect to the device ground or \(V_{OUT}\)

Equation 4 calculates the maximum inductor current:

\[
I_L = I_{L(avg)} + \frac{\Delta I_L}{2}
\]

### 2.3.2 \(V_{IN}\) and \(V_{OUT}\) Range

The input voltage that can be applied to an integrated circuit (IC) operating in the inverting buck-boost topology is less than the input voltage for the same IC operating in the buck topology. The reason for this difference is because the ground pin of the IC is connected to the (negative) output voltage. Therefore, the input voltage across the device is \(V_{IN}\) to \(V_{OUT}\), not \(V_{IN}\) to ground. Thus, the input voltage range of the TPS82130 is 3 to 17 V + \(V_{OUT}\), where \(V_{OUT}\) is a negative value.

The output voltage range is the same as when configured as a buck converter, but negative. The output voltage for the inverting buck-boost topology must be set between –0.9 and –6 V. The output voltage is set in the same way as the buck configuration, with two resistors connected to the FB pin. Use the same equation in the TPS82130 datasheet to set the output voltage, keeping both \(V_{OUT}\) and \(V_{FB}\) as positive values. The TIDA-01457 design sets the output voltage at –5 V, which gives an input voltage range of 3 to 12 V. However, it is not recommended to use a 12-V input voltage because voltage tolerances on the input supply can violate the recommended operating range of the TPS82130.

### 2.3.3 Maximum Output Current

In the inverting buck-boost topology, the maximum output current is reduced as compared to the buck topology. This reduction is a result of the peak inductor current being higher, as calculated in Equation 4. With a power module, there are additional thermal limits arising from the small size of the power module itself. Finally, there are further limits on the maximum output current that occur from stability due to the right-half plane zero, which occurs in the inverting buck-boost topology. Figure 8 shows the maximum output current based on temperature rise and stability for the TIDA-01457 design. The current limit for the TPS82130 device occurs above all curves in Figure 8 and therefore does not limit the maximum output current more than thermal or stability limits. The current limit itself still operates to limit the peak inductor current.

#### 2.3.3.1 Thermal Limits

The primary maximum output current limitation in most designs is a thermal limitation. As the output current increases, the absolute power loss (in mW) in the TPS82130 also increases, which causes a higher temperature rise across the thermal impedance of the TPS82130 device.

The TPS82130 datasheet recommends operating below a device temperature of 110°C and forbids operating above 125°C for reliability. Therefore, Figure 8 contains two thermal limit lines: one for a 110°C and one for a 125°C operating temperature. These lines are calculated by multiplying the power loss of the TPS82130 from Figure 9 by the \(\theta_{JA}\) of the TPS82130EVM-720, which is provided in the device datasheet as 46.1°C/W, and adding this value to a 25°C ambient temperature.
Using this method, the maximum output current at any ambient temperature can be calculated. Simply subtract the maximum ambient temperature from either 110°C or 125°C to obtain the allowable temperature rise. Divide the $\theta_{JA}$ of the printed circuit board (PCB) by this temperature rise to obtain the allowable power loss. Find this power loss in Figure 9 to determine the maximum output current under specific conditions. 46.1°C/W is useful as an estimate of $\theta_{JA}$. See Equation 5 for the calculation.

$$ P_{LOSS} \leq \frac{125 - T_{A\_MAX}}{\theta_{JA}} $$

(5)

### 2.3.3.2 Stability Limits and Output Capacitor Selection

The "recommended" curve in Figure 8 shows the recommended maximum output current based on stability. The TIDA-01457 design must be operated at load currents below this line. In most applications, which have ambient temperatures above 25°C, the thermal limit lines move down below the recommended line (as explained in Section 2.3.3.1), which further limits the maximum output current.

The inverting buck-boost topology contains a right-half plane zero, which significantly and negatively impacts the control loop response by adding an increase in gain along with a decrease in phase at a high frequency. This right-half plane zero can cause instability. Equation 6 estimates the frequency of the right-half plane zero.

$$ f_{(RHP)} = \frac{-(1-D)^2 \times V_{OUT}}{(D \times L \times f_{OUT} \times 2 \times \pi)} $$

(6)

The TIDA-01457 design uses four 22-µF output capacitors, which have an effective capacitance of about 36 µF at the –5-V output voltage. This amount of capacitance pushes the crossover frequency of the control loop down to frequencies low enough so that the right-half plane zero is sufficiently higher in frequency for stability. While one of these output capacitors requires placement near the TPS82130 device, the others can be placed at the point of load and serve as their input decoupling capacitor. When three of the output capacitors are placed at the point of load, the solution size is below 50 mm$^2$. If these three capacitors are included, the solution size of all components shown within the "Active Circuitry" box on the front page becomes around 75 mm$^2$.

More output capacitance improves stability by increasing the separation between the right-half plane zero and crossover. The right-half plane zero frequency occurs at lower frequencies with lower input voltages, which have a higher duty cycle. Load transient testing is the best test for stability, as described in the Simplifying Stability Checks application report (SLVA381) [1]. Because the VOS pin of the TPS82130 is connected on the device, it is impossible to break the entire control loop and measure a bode plot.

### 2.3.4 Enable Pin Configuration

The device is enabled when the voltage at the EN pin trips its threshold and the input voltage is above the undervoltage lockout (UVLO) threshold. The TPS82130 device stops operation when the voltage on the EN pin falls below its threshold or the input voltage falls below the UVLO threshold.

Because $V_{OUT}$ is the IC ground in this configuration, the EN pin must be referenced to $V_{OUT}$ instead of ground. In the buck configuration, 0.9 V is considered as high and less than 0.3 V is considered as low. In the inverting buck-boost configuration, however, the $V_{OUT}$ voltage is the reference; therefore, the high threshold is 0.9 V + $V_{OUT}$ and the low threshold is 0.3 V + $V_{OUT}$. For example, if $V_{OUT} = –5$ V, then $V_{EN}$ is considered at a high level for voltages above –4.1 V and a low level for voltages below –4.7 V.
This behavior can cause difficulties enabling or disabling the part because, in some applications, the IC providing the EN signal may not be able to produce negative voltages. The level-shifter circuit that Figure 5 shows removes any difficulties associated with the offset EN threshold voltages by eliminating the requirement for negative EN signals. If disabling the TPS82130 is not desired, the EN pin may be directly connected to $V_{IN}$ without this circuit.

The positive signal that originally drove EN is instead tied to the gate of Q1 (SYS_EN). When Q1 is OFF (SYS_EN grounded), Q2 has 0 V across its $V_{GS}$ and also remains OFF. In this state, the EN pin is initially at the level of the output voltage ($-5$ V), which is below the low-level threshold, and disables the device. When SYS_EN provides enough positive voltage to turn Q1 ON ($V_{GS}$ threshold as specified in the MOSFET datasheet), the gate of Q2 is at ground potential through Q1. This action drives the $V_{GS}$ of Q2 negative and turns Q2 ON. Then $V_{IN}$ ties to EN through Q2 and the pin is above the high-level threshold, which turns the device ON. Be careful to ensure that the $V_{GD}$ and $V_{GS}$ of Q2 remain within the MOSFET ratings during both the enabled and disabled states. Failing to adhere to this constraint can result in damaged MOSFETs.

Figure 24 and Figure 25 show the enable and disable sequence. The SYS_EN signal activates the enable circuit and the G/D node signal represents the shared node between Q1 and Q2. This circuit has been tested with a 5-V SYS_EN signal and dual N/PFET Si1029X. The EN signal is the output of the circuit and goes from $V_{IN}$ to $V_{OUT}$ to properly enable and disable the device. The PG pin is used as an output discharge to accelerate the return of $V_{OUT}$ to 0 V, when the IC is disabled.
2.3.5 Power Good Pin Configuration

The TPS82130 has a built-in power good (PG) function to indicate whether the output voltage has reached its appropriate level or not. The PG pin is an open-drain output that requires a pullup resistor. Because $V_{OUT}$ is the IC ground in this configuration, the PG pin is referenced to $V_{OUT}$ instead of ground, which means that the TPS82130 device pulls PG to $V_{OUT}$ when it is low.

This behavior can cause difficulties in reading the state of the PG pin, because in some applications the IC detecting the voltage level of the PG pin may not be able to withstand negative voltages. The level-shifter circuit shown in Figure 6 removes any difficulties associated with the offset PG pin voltages by eliminating the negative output signals of the PG pin. If the PG pin functionality is not required, it may be left floating or connected to $V_{OUT}$ without this circuit. Note that to avoid violating its absolute maximum rating, the PG pin should not be driven more than 6 V above the negative output voltage (IC ground).

![Figure 6. PG Pin Level Shifter](image)

Inside the TPS82130, the PG pin is connected to an N-channel MOSFET (Q3). By tying the PG pin to the gate of Q1, when the PG pin is pulled low, Q1 is off and Q2 is on because Q2's $V_{GS}$ is at $V_{CC}$. SYS_PG is then pulled to ground.

When Q3 turns OFF, the gate of Q1 is pulled to ground potential which turns Q1 ON. This sequence of events pulls the gate of Q2 below ground, which turns it OFF. SYS_PG is then pulled up to the $V_{CC}$ voltage. Note that the $V_{CC}$ voltage must be at an appropriate logic level for the circuitry connected to the SYS_PG net.

Figure 26 and Figure 27 show this PG pin level-shifter sequence. The PG signal activates the PG pin level-shifter circuit and the G/D node signal represents the shared node between Q1 and Q2. This circuit has been tested with a $V_{CC}$ of 5 V and dual NFET Si1902DL. The SYS_PG net is the output of the circuit and goes between ground and 5 V and is easily read by a separate device.
2.3.6 Discharging Output Voltage

If the TPS82130 device is disabled in a light-load or no-load condition, the PG pin can accelerate return of \( V_{\text{OUT}} \) to 0 V by providing an additional discharge path. When the IC has been disabled through the EN pin, the PG pin is connected to the device ground (\(-V_{\text{OUT}}\)) through an internal MOSFET. Placing a resistor between ground and the PG pin creates a discharge path to ground.

The added resistor must be sized to limit the current into the PG pin to a safe level, which the TPS82130 datasheet specifies as 10 mA at maximum. A 499-\( \Omega \) PG resistor has been chosen for this \(-5\)-V output voltage.

2.3.7 Adjustable Soft-Start Time

The TPS82130 features an adjustable soft-start time. The soft-start time is the rise time of the output voltage and is adjustable with the capacitor, CSS, on the SS/TR pin. If needed, the output voltage rise time is adjustable to match the rise time of a corresponding 5-V rail in the system. The soft-start time is set in the same way as described in the TPS82130 datasheet[3].

2.3.8 Input Capacitor Selection

An input capacitor, CIN, is required to provide a local bypass for the input voltage source. A low equivalent series resistance (ESR) X5R or X7R ceramic capacitor is best for input voltage filtering and minimizing interference with other circuits. For most applications, a 10-\( \mu \)F ceramic capacitor is recommended from \( V_{\text{IN}} \) to ground (system ground, not \(-V_{\text{OUT}}\)). The CIN capacitor value can be increased without any limit for better input voltage filtering.

For the inverting buck-boost configuration of the TPS82130, TI does not recommend installing a capacitor from \( V_{\text{IN}} \) to \(-V_{\text{OUT}}\). Such a capacitor, if installed, provides an AC path from \( V_{\text{IN}} \) to \(-V_{\text{OUT}}\). When \( V_{\text{IN}} \) is applied to the circuit, this dV/dt across a capacitor from \( V_{\text{IN}} \) to \(-V_{\text{OUT}}\) creates a current that must return to ground (the return of the input supply) to complete its loop. This current may flow through the body diode of the internal low-side MOSFET and the inductor to return to ground. Flowing through the body diode pulls the VOUT pin below IC ground, which violates its absolute maximum rating. Such a condition may damage the TPS82130 and is not recommended; therefore, a capacitor from \( V_{\text{IN}} \) to \(-V_{\text{OUT}}\) is not required or recommended. If such a capacitor (CBP) is present, then a Schottky diode must be installed on the output, as the schematic in Figure 7 shows.

![Figure 7. Installation of Schottky Diode D1 Required, if Installing CBP](image-url)
3 Getting Started Hardware

To test this TI Design, simply apply an input voltage between the J1 and J4 connectors. Then, connect a jumper between ON and EN on JP1.

4 Testing and Results

Figure 8. Maximum Output Current

Figure 9. Efficiency Over Load
Figure 10. Efficiency Over $V_{IN}$ (600-mA Load)

Figure 11. Load Regulation

Figure 12. Line Regulation (600-mA Load)

Figure 13. Switching Frequency Over $V_{IN}$ (600-mA Load)
Figure 14. Switching Frequency Over Load

Figure 15. Transient Response (3.3 $V_{IN}$, 0- to 600-mA Load Step)
Figure 16. Transient Response (5 V<sub>IN</sub>, 0- to 1-A Load Step)

Figure 17. Transient Response (7.5 V<sub>IN</sub>, 0- to 1.5-A Load Step)
3- to 11.5-V_{IN} –5-V_{OUT}, 1.5-A Inverting Power Module Reference Design for Small, Low-Noise Systems

Figure 18. Output Voltage Ripple (3.3 V_{IN}, 1-mA Load)

Figure 19. Output Voltage Ripple (3.3 V_{IN}, 600-mA Load)
Figure 20. Output Voltage Ripple (5 V\textsubscript{IN}, 1-mA Load)

Figure 21. Output Voltage Ripple (5 V\textsubscript{IN}, 1-A Load)
Figure 22. Output Voltage Ripple (11.5 V<sub>IN</sub>, 1-mA Load)

Figure 23. Output Voltage Ripple (11.5 V<sub>IN</sub>, 1.5-A Load)
Figure 24. Start-up on EN (5 V_in, No Load)

Figure 25. Shutdown on EN (5 V_in, No Load)
Figure 26. PG on Start-up (5 V_{IN}, No Load)

Figure 27. PG on Shutdown (5 V_{IN}, No Load)
5 Design Files

5.1 Schematics
To download the schematics, see the design files at TIDA-01457.

5.2 Bill of Materials
To download the bill of materials (BOM), see the design files at TIDA-01457.

5.3 PCB Layout Recommendations

5.3.1 Layout Prints
To download the layer plots, see the design files at TIDA-01457.

5.4 Gerber Files
To download the Gerber files, see the design files at TIDA-01457.

5.5 Assembly Drawings
To download the assembly drawings, see the design files at TIDA-01457.

6 Related Documentation

3. Texas Instruments, *TPS82130 17-V Input 3-A Step-Down Converter MicroSiP™ Module with Integrated Inductor*, TPS82130 Datasheet (SLVSCY5)

6.1 Trademarks
MicroSiP is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.
IMPORTANT NOTICE FOR TI DESIGN INFORMATION AND RESOURCES

Texas Instruments Incorporated ("TI") technical, application or other design advice, services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using any particular TI Resource in any way, you (individually or, if you are acting on behalf of a company, your company) agree to use it solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources.

You understand and agree that you remain responsible for using your independent analysis, evaluation and judgment in designing your applications and that you have full and exclusive responsibility to assure the safety of your applications and compliance of your applications (and of all TI products used in or for your applications) with all applicable regulations, laws and other applicable requirements. You represent that, with respect to your applications, you have all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. You agree that prior to using or distributing any applications that include TI products, you will thoroughly test such applications and the functionality of such TI products as used in such applications. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

You are authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT. AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING TI RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY YOU AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

You agree to fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of your non-compliance with the terms and provisions of this Notice.

This Notice applies to TI Resources. Additional terms apply to the use and purchase of certain types of materials, TI products and services. These include: without limitation, TI's standard terms for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm), evaluation modules, and samples (http://www.ti.com/sc/docs/sampterms.htm).

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2017, Texas Instruments Incorporated