The reference design is a high-efficiency and super transient AC/DC converter with a 85- to 265-V wide AC input, 12-V/5-V/3.3-V multiplexed DC output, and a 450-W maximum output, which applies well to gaming PCs, desktop PC PSUs, entry-level server PSUs, and other low-cost AC/DC PSUs. The circuit consists of a front-end continuous conduction mode (CCM) power factor correction (PFC) circuit, followed by an LLC stage for isolated DC/DC conversion. The design uses the UCC28180 controller for the PFC stage and UCC256301 controller for the LLC stage to achieve a compact and robust control structure. For high-efficiency needs, synchronous rectification is done using the UCC24612 and low R_DS(on) MOSFETs. This design can be used as an AC/DC supply in many applications demanding efficient and super transient power conversion.

**Features**

- Wide Operating Input Range: 85- to 265-V AC With Full Power Delivery Over Entire Range
- Leading Transient Performance With Half Duty Cycle Response for Line Transient and Dynamic Load
- Peak Overall Efficiency of 93% at 230-V AC and 91.8% at 115-V AC, Fan Cooling Needed up to 55°C Ambient Operation
- High Power Factor > 0.96 at 230-V AC From 50% to 100% Load Meets PFC Regulations and Current THD as per IEC 61000-3-2 Class D
- Meets Requirements of Conducted Emissions Standard: EN55032 Class B (CE)
- Single-Layer PCB Design to Achieve Low Cost

**Applications**

- Gaming PCs
- Entry-Level Server PSUs
- Desktop PC PSUs
- Other Low-Cost AC/DC PSUs

**Resources**

- TIDA-01501
- TIDA-01444
- TIDA-01503
- UCC256301
- UCC28180
- CSD18540Q5B
- UCC24612
- LM258A
- TL431B

**Description**

The reference design is a high-efficiency and super transient AC/DC converter with a 85- to 265-V wide AC input, 12-V/5-V/3.3-V multiplexed DC output, and a 450-W maximum output, which applies well to gaming PCs, desktop PC PSUs, entry-level server PSUs, and other low-cost AC/DC PSUs. The circuit consists of a front-end continuous conduction mode (CCM) power factor correction (PFC) circuit, followed by an LLC stage for isolated DC/DC conversion. The design uses the UCC28180 controller for the PFC stage and UCC256301 controller for the LLC stage to achieve a compact and robust control structure. For high-efficiency needs, synchronous rectification is done using the UCC24612 and low R_DS(on) MOSFETs. This design can be used as an AC/DC supply in many applications demanding efficient and super transient power conversion.
1 System Description

This reference design is a high-efficiency and super transient AC/DC converter for desktop PC PSUs, gaming PC PSUs, entry-level server PSUs, and other low-cost AC/DC PSUs. The circuit consists of a front-end continuous conduction mode (CCM) power factor correction (PFC) circuit, followed by an LLC-based second stage. The design uses the UCC28180 controller for PFC stage and UCC256301 controller for LLC stage to achieve a compact and robust control structure. Synchronous rectification based on the UCC24612 and low $R_{D\text{son}}$ FETs from Texas Instruments help in achieving higher efficiencies. This reference design can be used as an AC/DC supply in many applications demanding efficient and super transient power conversion.

The converter is designed for a wide input voltage range of 85- to 265-V AC with full power delivery over entire range and has multiplexed DC outputs of 12 V, 5 V, and 3.3 V. An output of 12 V has a maximum power delivery of 450 W at a maximum current of 37.5 A and outputs of 5 V and 3.3 V have a total maximum power delivery of 180 W with arbitrary power distributions in two channels. The converter has super transient performance achieved by the technique of half duty cycle response for line transient and dynamic load and also has line and load regulation within ±5%.

The design has an operating peak efficiency of around 93% with 230-V AC and 91.8% with 115-V AC at half load. The design has a high power factor $> 0.96$ at 230-V AC from a 50% to 100% load and meets PFC regulations and current THD as per IEC 61000-3-2 Class D. The design form factor (110 mm × 144 mm) is compact for the power level of 450 W. The single-layer PCB design achieves low cost very well. The system also has some robust protections built in (OVP, OCP, and OTP), which make the converter more secure and reliable.

The EMI filter at the front end of the circuit is designed to meet EN55032 class-B conducted emission levels. This filter is followed by an active boost PFC stage operating in CCM. This PFC stage regulates the DC bus voltage to 408 V, stabilized against line dropouts with a bulk storage capacitor. The isolated power stage of the charger is an LLC resonant converter operating very close to resonant frequency at a 12-V output. The operation moves to above or below resonance according to the voltage and current requirements of the load. The output voltage feedback is achieved using the LM258 op amp circuit, which has integrated dual op amps. A TL431 device generates the required reference levels for the feedback circuitry. There is provision to alter the voltage references by means of a small external add-on card. The system is designed to meet below 480 mW of standby power when no load is connected. This is achieved using a simple logic circuit that disables PFC and LLC power stages when load is not present.

The design uses a 20-W power supply board (TIDA-01503), which is designed to meet the auxiliary needs of a general power supply. The design supports an input voltage range from 100- to 425-V DC and provides a 15-V DC (3.75-W) non-isolated outputs. In addition, a 15-V DC (3.75-W) and 5-V DC (12.5-W) isolated output is also provided to support isolated auxiliary power needs. The features of the power supply board include easy pluggability, compact size, high efficiency, low no-load power consumption, and low cost. Find more details in the design guide of the power supply reference design, the TIDA-01503.

The design delivers high performances with low power consumption and a low bill of material (BOM) cost. Various parameters of the design like regulation, efficiency, EMI signature, output ripple, startup, and switching stresses are tested and documented.
### 1.1 Key System Specifications

#### Table 1. Key System Specifications

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>SPECIFICATION</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>INPUT CHARACTERISTICS</strong></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Input voltage (V\textsubscript{INAC})</td>
<td>85 230 265</td>
<td>VAC</td>
<td></td>
</tr>
<tr>
<td>Frequency (f\textsubscript{LINE})</td>
<td>47 50 63</td>
<td>Hz</td>
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</tr>
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<td><strong>OUTPUT CHARACTERISTICS</strong></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>Output voltage</td>
<td>Output Channel 1</td>
<td>12</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Output Channel 2</td>
<td>5</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Output Channel 3</td>
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<td>V</td>
</tr>
<tr>
<td>Maximum output current</td>
<td>For 12 V\textsubscript{OUT}</td>
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<td>A</td>
</tr>
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<td></td>
<td>For 5 V\textsubscript{OUT}</td>
<td>30</td>
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</tr>
<tr>
<td></td>
<td>For 3.3 V\textsubscript{OUT}</td>
<td>30</td>
<td>A</td>
</tr>
<tr>
<td>Line regulation</td>
<td>For 12 V\textsubscript{OUT}</td>
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<td>%</td>
</tr>
<tr>
<td>Load regulation</td>
<td>For 12 V\textsubscript{OUT}</td>
<td>5</td>
<td>%</td>
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<tr>
<td>Ripple and noise</td>
<td>V\textsubscript{OUT} = 12-V DC</td>
<td>70</td>
<td>mV</td>
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<tr>
<td></td>
<td>V\textsubscript{OUT} = 5-V DC</td>
<td>100</td>
<td>mV</td>
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<tr>
<td></td>
<td>V\textsubscript{OUT} = 3.3-V DC</td>
<td>150</td>
<td>mV</td>
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<tr>
<td>Output power (PO)</td>
<td></td>
<td>450</td>
<td>W</td>
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<tr>
<td>Output transient response</td>
<td>12 V\textsubscript{OUT}, 50% load as the step load</td>
<td>4</td>
<td>%</td>
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<tr>
<td>Output OVP</td>
<td>For 12 V\textsubscript{OUT}</td>
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<td>V</td>
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<td>Output OCP</td>
<td>For 12 V\textsubscript{OUT}</td>
<td>120</td>
<td>%</td>
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<td><strong>SYSTEM CHARACTERISTICS</strong></td>
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<tr>
<td>Efficiency</td>
<td>Low line</td>
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<td></td>
<td>High line</td>
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<td>IEC61000-3-2, class D</td>
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<tr>
<td></td>
<td>THD</td>
<td>IEC61000-3-2, class D</td>
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<tr>
<td>Board form factor</td>
<td>Length × Breadth × Height</td>
<td>110</td>
<td>144</td>
</tr>
</tbody>
</table>
2 System Overview

2.1 Block Diagram

Figure 1. TIDA-01501 Block Diagram

2.2 Highlighted Products

2.2.1 UCC28180—CCM PFC Controller

The UCC28180 is a high-performance, CCM, 8-pin programmable frequency PFC controller. The wide and programmable operating frequency of the controller provides flexibility to design at a high frequency to optimize the components. The UCC28180 uses trimmed current loop circuits to achieve less than a 5% THD from a medium-to-full load (50% to 100%). A reduced current sense threshold enables the UCC28180 device to use a 50% smaller shunt resistor, resulting in lower power dissipation while maintaining low THD. The UCC28180 also consists of an integrated fast gate driver, with a drive of 2-A source current and –1.5-A sink current, which eliminates the need for an external gate driver. The UCC28180 device also has a complete set of system protection features that greatly improves reliability and further simplifies the design:

- Soft overcurrent
- Cycle-by-cycle peak current limit
- Output overvoltage
- VCC undervoltage lockout (UVLO) protection
- Open pin protections (ISENSE and VSENSE pins)

2.2.2 UCC256301—LLC Controller

The UCC256301 is a fully featured LLC controller. The UCC256301 includes a range of features designed to make LLC converter operation well controlled and robust. The part aims to unburden the LLC designer and allow mainstream applications to benefit from efficiency advantages of the LLC topology.

This device uses hybrid hysteretic control to provide best in class line and load transient response. The control effort is approximately linear proportional to average input current in one cycle. The control makes the open loop transfer function a first-order system so that it’s very easy to compensate. The system is always stable with proper frequency compensation.

The UCC256301 provides a highly efficient burst mode with consistent burst power level during each burst on cycle. The burst power level is programmable and adaptively changes with input voltage, making the optimization of efficiency very easy.

Other features include fast exit from burst mode, up to 1 MHz of switching frequency, overtemperature, output overvoltage, three-level overcurrent protections, and X-capacitor discharge.
2.2.3  **UCC24612—Secondary-Side Synchronous Rectifier Controller**

To achieve higher efficiencies at low output voltages, synchronous rectification is inevitable. To achieve high reliability and avoid false triggering and related failures of synchronous rectifiers, a device requires a highly reliable, proven, and fail-proof controller. The UCC24612 meets all the requirements of a synchronous rectifier controller for LLC converters.

The UCC24612 is a high-performance controller and driver for standard and logic-level N-channel MOSFET power devices used for low-voltage secondary-side synchronous rectification. The combination of controller and MOSFET emulates a near-ideal diode rectifier. This solution not only directly reduces power dissipation of the rectifier but also indirectly reduces primary-side losses as well due to compounding of efficiency gains. Using drain-to-source voltage sensing, the UCC24612 is ideal for LLC resonant power supplies.

This device is available in a 5-pin SOT-23-5 package.

Other key features include:

- Up to 1-MHz operating frequency
- \( V_{DS} \) MOSFET sensing
- 4-A sink, 1-A source gate-drive capability
- Micro-power sleep current for 90+ designs
- Automatic light-load management
- Synchronous wake-up from sleep and light-load modes
- Adaptive minimum off time for better noise immunity
- 16-ns typical turnoff propagation delay
- 9.5-V gate drive clamp levels for minimum driving loss

2.2.4  **LM258A—Operational Amplifiers**

Both voltage and current control loop compensation is performed using the widely proven and cost effective LM258 dual op amp. Some key features that make it extremely suitable for loop compensation in the present design include:

- Also works on single supply: 3 to 32 V
- Low supply-current drain, independent of supply voltage: 0.7 mA typical
- Wide unity gain bandwidth: 0.7 MHz
- Low input bias and offset parameters input offset voltage: 2 mV typical
- Input offset current: 2 nA typical
- Input bias current: 15 nA typical
- Differential input voltage range equal to maximum-rated supply voltage: 32 V
- Open-loop differential voltage gain: 100 dB typical
- Internal frequency compensation

2.2.5  **CSD18540Q5B—60-V N-Channel NexFET™ Power MOSFET**

To achieve high-efficiency synchronous rectification, TI’s power MOSFET CSD18540Q5B has been employed in this reference design. This is a 60-V rated FET with an extremely low on-state resistance of 1.8 m\( \Omega \). Some additional features that make this FET suitable for the present design include:

- Low \( Q_g \) and \( Q_{gd} \)
- Low-thermal resistance
- Avalanche rated
- Lead-free terminal plating
- RoHS compliant
- Halogen free
- SON 5-mm × 6-mm plastic package
2.2.6 **TIDA-01444—180-W, Dual-Channel Step-Down Converter**

A dual-channel, step-down converter is needed to get 5-V and 3.3-V DC outputs from 12-V DC output of LLC. The TIDA-01444 design is used for this purpose. This design implements a 180-W buck, dual-channel DC/DC converter with a regulatory 12-V DC input voltage designed to provide the terminal load voltage with greater than 97% efficiency and good thermal performance. The switching frequency synchronization between the dual channels is easily realized. The true differential remote sense of the dual outputs compensates the line voltage drop providing more accurate voltage for the terminal load. For improved high power density and a low profile, this integrated circuit reference design uses a planar inductor to replace the traditional discrete inductor. This reference design has complete protection and temperature sense functions. For more details, see the TIDA-01444 design guide. Note that the dual-channel, step-down converter TIDA-01444 is already mounted on the TIDA-01501 board and hence is an integral part of it.

2.2.7 **TIDA-01503**

This design is a 20-W, multiple outputs, auxiliary power supply designed for use in power converters targeted for industrial system applications. This solution is a multiple output flyback converter implemented using the UCC28704 to provide constant-voltage (CV) and constant-current (CC) output regulation and uses discontinuous conduction mode (DCM) valley switching to achieve high efficiency. The design is compact and affordable due to minimal component count with all the necessary built-in protections such as output overcurrent and output short circuit. Hardware is designed and tested to pass EFT requirements and aids to meet low power efficiency performance of the Department of Energy (DoE) Level VI standards.

2.3 **System Design Theory**

The design process starts by deciding on the component values in the LLC power train and then moving to the PFC stage.

2.3.1 **LLC Design Goal Parameters**

Table 2 shows the design goal parameters for the LLC stage.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>SPECIFICATION</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>INPUT CHARACTERISTICS</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input voltage (V&lt;sub&gt;INDC&lt;/sub&gt;)</td>
<td>N/A</td>
<td>365</td>
<td>408</td>
</tr>
<tr>
<td><strong>OUTPUT CHARACTERISTICS</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output voltage</td>
<td>N/A</td>
<td>12</td>
<td>V</td>
</tr>
<tr>
<td>Maximum output power</td>
<td>N/A</td>
<td>450</td>
<td>W</td>
</tr>
<tr>
<td>Efficiency</td>
<td>N/A</td>
<td>0.95</td>
<td>%</td>
</tr>
<tr>
<td>Nominal switching frequency</td>
<td>N/A</td>
<td>110</td>
<td>kHz</td>
</tr>
<tr>
<td>Line regulation</td>
<td>N/A</td>
<td>5</td>
<td>%</td>
</tr>
<tr>
<td>Load regulation</td>
<td>N/A</td>
<td>5</td>
<td>%</td>
</tr>
</tbody>
</table>

2.3.2 **LLC Circuit Component Design**

One of the reasons that LLC topology is so popular is that it can achieve zero voltage switching (ZVS) over a wide range of operating conditions. ZVS is important because it reduces switching losses in the power devices.
2.3.2.1 **Design Approach for PSU Application**

LLC topology has been widely used in telecom and server power supplies. LLC topology can get a wide gain range by changing the frequency. LLC topology usually applies to generate a constant output voltage for a wide input DC voltage ranging or generate a variable output voltage for a constant input DC voltage. With the wider frequency range, the wider LLC gain is the more difficult circuit design is. For PSU application, the situation is different. The input and output voltage are both constant, which makes the design easier. LLC topology can achieve both ZVS for primary MOSFET and ZCS for secondary diode under resonant frequency. Considering efficiency, therefore, the converter is designed to operate at frequency slightly lower than resonance (second resonance) when generating a 12-V output at full load.

2.3.2.2 **LLC Transformer Turns Ratio**

Determine the transformer turns ratio by the nominal input and output voltages.

\[
\frac{V_{\text{IN(nom)}}}{2} = \frac{V_{\text{OUT(nom)}}}{2} = 17 \Rightarrow 16
\]

Where:

- \( V_{\text{IN}} \) is the voltage on the bulk capacitor; this is regulated at 408-V DC

No additional diode drop needs to be accounted for because a synchronous rectifier is used. Further, the converter operates at resonance when delivering a 12-V DC output.

2.3.2.3 **Determine Equivalent Load Resistance**

Determine the equivalent load resistance using Equation 2:

\[
R_e = \frac{8 \times n^2 \times V_{\text{OUT(nom)}}}{\pi^2 \times I_{\text{OUT(nom)}}} = \frac{8 \times 16^2}{\pi^2} \times \frac{12}{37.5} = 66.4 \, \Omega
\]

(2)

2.3.2.4 **LLC Gain Range**

Determine the LLC gain range \( M_{G(\text{min})} \) and \( M_{G(\text{max})} \).

\[
M_{G(\text{min})} = n \frac{V_{\text{OUT(min)}}}{V_{\text{IN(max)}} / 2} = 16 \frac{12}{428 / 2} = 0.935
\]

(3)

\[
M_{G(\text{max})} = n \frac{V_{\text{OUT(max)}}}{V_{\text{IN(min)}} / 2} = 16 \frac{12}{365 / 2} = 1.096
\]

(4)
Figure 2 shows the LLC gain curve with the selected $L_N$ and $Q_E$:

![Figure 2. LLC Gain Curve With Selected $L_N$ and $Q_E$](image)

2.3.2.5 Select $L_N$ and $Q_E$

$L_N$ is the ratio between the magnetizing inductance and the resonant inductance.

$$L_N = \frac{L_m}{L_r}$$  \hspace{1cm} (5)

$Q_E$ is the quality factor of the resonant tank.

$$Q_E = \frac{\sqrt{L_r / C_r}}{R_E}$$  \hspace{1cm} (6)

In Equation 6, $R_E$ is the equivalent load resistance.

Selecting $L_N$ and $Q_E$ values must result in an LLC gain curve, as shown in Figure 3, that intersects with $M_G(\text{min})$ and $M_G(\text{max})$ traces. The peak gain of the resulting curve must be larger than $M_G(\text{max})$. 

---

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The relationship between $M_{G(\text{peak})}$ and $Q_E$ with respect to $L_n$ is shown in Figure 3:

![Figure 3. $M_{G(\text{peak})}$ versus $Q_E$ With Respect to $L_n$](image)

In this case, the selected $L_n$ and $Q_e$ values are:

$L_n = 7$

$Q_e = 0.358$

### 2.3.2.6 Switching Frequency

The wide switching frequency of the UCC256301 is from 35 kHz to 1 MHz, which makes this reference design more flexible. To make the transformer and inductor with a smaller size and LLC converter, always work under resonant frequency with a 12-V DC output at full load. The second resonant frequency is chosen to be 115 kHz.

$$f_0 = 115 \text{ kHz}$$

(7)

### 2.3.2.7 Determine Component Parameters for LLC Resonant Circuit

The resonant tank parameters can be calculated as follows:

$$C_r = \frac{1}{2\pi \times Q_e \times f_0 \times R_e} = \frac{1}{2\pi \times 0.358 \times 115 \text{ kHz} \times 66.4 \Omega} = 58 \text{ nF}$$

(8)

$$L_r = \frac{1}{(2\pi \times f_0)^2 \times C_r} = \frac{1}{(2\pi \times 115 \text{ kHz})^2 \times 58 \text{ nF}} = 33 \mu\text{H}$$

(9)

$$L_m = L_n \times L_r = 7 \times 28.2 \mu\text{H} = 231 \mu\text{H}$$

(10)

After the preliminary parameters are selected, find the closest actual component value that is available, re-check the gain curve with the selected parameters, and then run time domain simulation to verify the circuit operation. This results in the following resonant tank parameters:

$C_r = 55 \text{ nF}$

$L_r = 32.8 \mu\text{H}$

$L_m = 230 \mu\text{H}$
Based on the final resonant tank parameters, the resonant frequency can be calculated as follows:

\[
f_0 = \frac{1}{2\pi\sqrt{L_r C_r}} = \frac{1}{2\pi \sqrt{55 \text{ nF} \times 32.8 \text{ \mu H}}} = 118.5 \text{ kHz}
\]  

Based on the new LLC gain curve, the normalized switching frequency at maximum and minimum gain are given by:

\[
f_n(Mg_{\text{max}}) = 0.73
\]

\[
f_n(Mg_{\text{min}}) = 1.3
\]

The maximum and minimum switching frequencies are:

\[
f_{\text{SW}(\text{max})} = 86.5 \text{ kHz}
\]

\[
f_{\text{SW}(\text{min})} = 154 \text{ kHz}
\]

2.3.2.8 LLC Primary Side Currents

The primary side currents are calculated for selecting components. The currents are calculated based on a 110% overload condition.

The primary side RMS load current is given by:

\[
I_{OE} = \frac{\pi}{2\sqrt{2}} \times \frac{I_O}{n} = \frac{\pi}{2\sqrt{2}} \times \frac{1.1 \times 37.5 \text{ A}}{16} = 2.864 \text{ A}
\]

The RMS magnetizing current at minimum switching frequency is given by:

\[
I_m = \frac{2\sqrt{2}}{\pi} \times \frac{nV_{\text{OUT}}}{\omega L_m} = \frac{2\sqrt{2}}{\pi} \times \frac{16 \times 12}{2\pi \times 86.5 \text{ kHz} \times 230 \text{ \mu H}} = 1.383 \text{ A}
\]

The total current in resonant tank is given by:

\[
I_t = \sqrt{I_m^2 + I_{OE}^2} = \sqrt{(1.383 \text{ A})^2 + (2.864 \text{ A})^2} = 3.18 \text{ A}
\]

2.3.2.9 LLC Secondary Side Currents

The total secondary-side RMS load current is the current referred from the primary-side current (I_{OE}) to the secondary side.

\[
I_{OES} = n \times I_{OE} = 16 \times 2.864 \text{ A} = 45.824 \text{ A}
\]

In this design, the transformer’s secondary side has a center-tapped configuration. The current of each secondary transformer winding is calculated by:

\[
I_{ws} = \frac{\sqrt{2} \times I_{OES}}{2} = \frac{\sqrt{2} \times 45.824 \text{ A}}{2} = 32.4 \text{ A}
\]

The corresponding half-wave average current is:

\[
I_{sav} = \frac{\sqrt{2} \times I_{OES}}{\pi} = \frac{\sqrt{2} \times 45.824 \text{ A}}{\pi} = 20.63 \text{ A}
\]
2.3.2.10 LLC Transformer

A bias winding is needed for output voltage protection. The transformer can be built or purchased according to these specifications:

- Turns ratio is primary to secondary to bias = 16 to 1 to 1
- Primary terminal voltage: 450-V AC
- Primary magnetizing inductance: \( L_m = 230 \, \mu H \)
- Primary side winding rated current: \( I_p = 3.18 \, A \)
- Secondary terminal voltage: 24-V AC
- Secondary winding rated current: \( I_{WS} = 32.4 \, A \)
- Minimum switching frequency: 86.5 kHz
- Maximum switching frequency: 154 kHz
- Insulation between primary and secondary sides: IEC 60950 reinforced insulation

The minimum operating frequency during normal operation is that calculated above, but during shutdown the LLC can operate at right above ZCS boundary condition, which is a lower frequency. The magnetic components in the resonant circuit, the transformer, and resonant inductor must be rated to operate at this lower frequency.

2.3.2.11 LLC Resonant Inductor

The AC voltage across the resonant inductor is given by its impedance times the current:

\[
V_{Lr} = \omega L R I_R = 2\pi \times 86.5 \times 10^3 \times 32.8 \times 10^{-6} \times 3.18 = 56.7 \, V 
\]  

(22)

The inductor can be built or purchased according to the following specifications:

- Inductance: \( L_r = 32.8 \, \mu H \)
- Rated current: \( I_r = 3.18 \, A \)
- Terminal AC voltage: \( V_{Lr} = 56.7 \, V \)
- Frequency range: 86.5 to 154 kHz

The minimum operating frequency during normal operation is that calculated above but during shutdown the LLC can operate at right above ZCS boundary condition, which is a lower frequency. The magnetic components in the resonant circuit, the transformer, and resonant inductor must be rated to operate at this lower frequency.

2.3.2.12 LLC Resonant Capacitor

This capacitor carries the full-primary current at a high frequency. A low dissipation factor part is needed to prevent overheating in the part.

The AC voltage across the resonant capacitor is given by its impedance times the current.

\[
V_{CR} = \frac{I_r}{\omega C_r} = \frac{3.18}{2\pi \times 86.5 \times 10^3 \times 55 \times 10^{-9}} = 106.4 \, V 
\]  

(23)

\[
V_{CR(rms)} = \sqrt{\left( \frac{V_{IN(max)}}{2} \right)^2 + V_{CR}^2} = \sqrt{\left( \frac{428}{2} \right)^2 + 106.4^2} = 239 \, V 
\]  

(24)

Peak voltage:

\[
V_{CR(peak)} = \frac{V_{IN(max)}}{2} + \sqrt{2} \times V_{CR} = \frac{428}{2} + \sqrt{2} \times 106.4 = 364.4 \, V 
\]  

(25)

Valley voltage:

\[
V_{CR(valley)} = \frac{V_{IN(max)}}{2} - \sqrt{2} \times V_{CR} = \frac{428}{2} - \sqrt{2} \times 106.4 = 65.8 \, V 
\]  

(26)
2.3.2.13 LLC Primary Side MOSFETs

Specify the MOSFET parameters required for the converter. Each MOSFET sees the input voltage as its maximum applied voltage. Choose the MOSFET voltage rating to be 1.5 times of the maximum bulk voltage:

\[ V_{\text{LLC (peak)}} = 1.5 \times V_{\text{in (max)}} = 642 \text{ V} \]

Choose the MOSFET current rating to be 1.1 times of the maximum primary side RMS current:

\[ I_{\text{LLC}} = 1.1 \times I_f = 3.5 \text{ A} \]

2.3.2.14 LLC Rectifier Diodes

The voltage rating of the output diodes is given by:

\[ V_{\text{DB}} = 1.2 \times \frac{V_{\text{in (max)}}}{n} = 1.2 \times \frac{428}{16} = 32.1 \text{ V} \]

The current rating of the output diodes is given by:

\[ I_{\text{SAV}} = \frac{\sqrt{2} \times I_{\text{OES}}}{\pi} = \frac{\sqrt{2} \times 45.817}{\pi} = 20.625 \text{ A} \]

2.3.2.15 LLC Output Capacitors

The LLC converter topology does not require an output filter although a small second-stage filter inductor may be useful in reducing peak-to-peak output noise. Assuming that the output capacitors carry the full wave output current of the rectifier, then the capacitor ripple current rating is:

\[ I_{\text{RECT}} = \frac{\pi}{2\sqrt{2}} \times I_{\text{OUT}} = \frac{\pi}{2\sqrt{2}} \times 37.5 = 41.652 \text{ A} \]

Use a 20-V rating for 12-V output voltage:

\[ V_{\text{LLC (Cap)}} = 20 \text{ V} \]

The capacitor’s RMS current rating is:

\[ I_{\text{C (out)}} = \sqrt{\left(\frac{\pi}{2\sqrt{2}} \times I_{\text{OUT}}\right)^2 - I_{\text{OUT}}^2} = \sqrt{\left(\frac{\pi}{2\sqrt{2}} \times 37.5\right)^2 - 37.5^2} = 18.128 \text{ A} \]

Solid aluminum capacitors with conductive polymer technology have high-ripple current ratings and are a good choice here. The ripple current rating for a single capacitor may not be sufficient, so multiple capacitors are often connected in parallel.

The ripple voltage at the output of the LLC stage is a function of the amount of AC current that flows in the capacitors. To estimate this voltage, assume that all the current, including the DC current in the load, flows in the filter capacitors.

\[ E_{\text{max}} = \frac{V_{\text{OUT (pk-pk)}}}{I_{\text{ RECT (pk)}}} = \frac{0.12 \text{ V}}{2 \frac{\pi}{4} \times 37.5 \text{ A}} = 2.037 \text{ m} \Omega \]

The capacitor specifications are:

- Voltage rating: 20 V
- Ripple current rating: 41.652 A
- ESR: < 2.037 mΩ
2.3.3 PFC Stage Design Goal Parameters

Table 3 shows the design goal parameters for the PFC stage.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>SPECIFICATION</th>
<th>UNIT</th>
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<tbody>
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<td></td>
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<td>Input voltage (V_{IN})</td>
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<td>265  V</td>
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<td>Line frequency</td>
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<td>OUTPUT CHARACTERISTICS</td>
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<td>PF</td>
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<td>Line regulation</td>
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<td>%</td>
</tr>
<tr>
<td>Load regulation</td>
<td>N/A</td>
<td>5</td>
<td>%</td>
</tr>
</tbody>
</table>

2.3.3.1 Design Procedure for PFC Stage

The boost topology operated in CCM is a popular choice for a PFC stage because it has lower component stresses than other topologies. This topology becomes more important at higher power levels.

The basic schematics for the three boost PFC circuits [Discontinuous Conduction Mode (DCM), Transition Mode (TM), and CCM] are the same. The differences relate to whether or not the inductor current is allowed to go to zero for part of the PWM cycle (DCM) and whether the PFC frequency is held constant or used as a control variable.

2.3.3.2 PFC Stage Output Current Calculation

The first step is to determine the maximum load current on the PFC stage, allowing for an overload to 110% of maximum load power.

\[
I_{OUT(PFC)} = \frac{110\% \times P_{OUT}}{V_{BLK}} = \frac{1.1 \times 450 \text{ W}}{398 \text{ V}} = 1.244 \text{ A}
\]  \hspace{1cm} (36)

2.3.3.3 Line Current Calculation

Next, determine the maximum RMS input-line current, allowing for an overload to 110% of maximum load power.

\[
I_{LINE(RMS(max))} = \frac{110\% \times P_{OUT}}{\eta V_{AC(min)}} = \frac{1.1 \times 450 \text{ W}}{0.98 \times 85 \text{ A}} = 5.94 \text{ A}
\]  \hspace{1cm} (37)

The peak line current is:

\[
I_{LINE(PEAK(max))} = \sqrt{2} \times I_{LINE(RMS(max))} = \sqrt{2} \times 5.94 \text{ A} = 8.4 \text{ A}
\]  \hspace{1cm} (38)

The average line current is given by:

\[
I_{LINE(AVG(max))} = \frac{2 \times I_{LINE(PEAK(max))}}{\pi} = \frac{2 \times 8.4}{\pi} = 5.35 \text{ A}
\]  \hspace{1cm} (39)
2.3.3.4 Bridge Rectifier

A typical bridge rectifier has a forward voltage drop \(V_{F,\text{BR}}\) of 0.95 V. The power loss in the bridge rectifier can be calculated from:
\[
P_{\text{BR}} = 2 \times V_{F(\text{BR})} \times I_{\text{LINE}(\text{AVG}(\text{max}))} = 2 \times 0.95 \text{ V} \times 5.35 \text{ A} = 10.165 \text{ W}
\]
(40)

The bridge rectifier must be rated to carry the full-line current \(I_{\text{LINE}(\text{AVG}(\text{max}))}\). The voltage rating of the bridge must be at least 600 V. The bridge rectifier also carries the full inrush current as the bulk capacitor \(C_{\text{BLK}}\) charges when the line is connected. The amplitude and duration of this current is difficult to determine in advance because it depends on parameters that are hard to predict.

2.3.3.5 PFC Boost Inductor

The boost inductor is usually chosen so that the peak-to-peak amplitude of the switching frequency ripple current, \(I_{\text{HFR, PFC}}\), is between 20% and 40% of the average current at peak of line. This design example uses \(I_{\text{HFR, PFC}} = 40\%\). Numerically, this is from Equation 41:
\[
I_{\text{HFR}} = 0.4 \times I_{\text{LINE}(\text{PEAK}(\text{max}))} = 0.4 \times 8.4 \text{ A} = 3.36 \text{ A}
\]
(41)

The maximum duty cycle is:
\[
D_{\text{MAX}} = 1 - \frac{V_{\text{IN}(\text{min})}}{\sqrt{2}} \times \frac{\sqrt{2}}{V_{\text{BLK}}} = 1 - \frac{85 \times \sqrt{2}}{398} = 0.698
\]
(42)

The minimum boost inductor value is calculated from the maximum duty cycle in Equation 42.
\[
L_{\text{PFC}} \geq \frac{V_{\text{BLK}} \times D_{\text{MAX}} (1 - D_{\text{MAX}})}{I_{\text{HFR}} \times I_{\text{PFC}}} = \frac{398 \times 0.698 (1 - 0.698)}{68 \text{ kHz} \times 3.36} = 367 \mu \text{H}
\]
(43)

The boost inductor must be able to support a maximum current of:
\[
I_{\text{L(PEAK)}} = I_{\text{LINE}(\text{PEAK}(\text{max}))} + \frac{I_{\text{HFR}}}{2} = 8.4 \text{ A} + \frac{3.36 \text{ A}}{2} = 10.08 \text{ A}
\]
(44)

The boost inductor was selected with the following specifications to allow proper margins:
- \(L_{\text{PFC}} = 630 \mu \text{H}\)
- \(\text{Current} = 12 \text{ A}\)

2.3.3.6 PFC Input Capacitor

The purpose of the input capacitor is to provide a local, low-impedance source for the high-frequency ripple currents, which flow in the PFC inductor. The allowed voltage ripple on \(C_{\text{IN}}\) is \(\Delta V_{\text{IN}}\).
\[
\Delta V_{\text{IN}} = 10\% \times \sqrt{2} \times V_{\text{AC}(\text{min})} = 10\% \times \sqrt{2} \times 85 \text{ V} = 12 \text{ V}
\]
(45)

\[
C_{\text{IN}} = \frac{I_{\text{HFR}}}{8 \times I_{\text{PFC}} \times \Delta V_{\text{IN}}} = \frac{3.36 \text{ A}}{8 \times 68 \text{ kHz} \times 12 \text{ V}} = 515 \text{ nF}
\]
(46)

An X2-rated film capacitor of 470 nF is chosen for this application.

2.3.3.7 PFC Stage MOSFET

The main specifications for the PFC stage MOSFET are:
- \(B_{\text{VDS}, \text{min}}\), drain source breakdown voltage: \(\geq 600 \text{ V}\)
- \(R_{\text{DS(on)}}\), on-state drain source resistance: approximately 150 mΩ at 100°C
- \(t_r\), device rise time: approximately 25 ns (Note that this time varies with change in the gate turnoff resistance)
- \(t_f\), device fall time: approximately 7 ns (Note that this time varies with change in the gate turnon resistance)
The losses in the device are calculated in the following equations. These calculations are approximations because the losses are dependent on parameters, which are not well controlled. For example, the $R_{DS(on)}$ of a MOSFET can vary by a factor of 2 from 25°C to 125°C. Therefore, several iterations may be needed to choose an optimum device for an application different to the one discussed. The conduction losses are estimated by:

$$\psi_D = \left[ \frac{P_{OUT(max)}}{\sqrt{2} \times V_{AC(min)}} \times \sqrt{2 - \frac{16 \times \sqrt{2} \times V_{AC(min)}}{3 \pi \times V_{BLK}}} \right]^2$$

$$R_{DS(on)} = \left[ \frac{450}{\sqrt{2} \times 85 \text{ V}} \times \sqrt{2 - \frac{16 \times \sqrt{2} \times 85 \text{ V}}{3 \pi \times 398}} \right]^2 0.15 \Omega = 3.13$$

(47)

The switching losses in the MOSFET are estimated by:

$$P_{Q1(SW)} = \frac{1}{2} P_{FPC} \left( V_{BLK} \times I_{LINE(RMS(max))} \times (t_r + t_f) + C_{OSS} \times V_{BLK}^2 \right)$$

$$= \frac{1}{2} 68k \times \left( 398 \times 5.94 \text{ A} \times (25n + 7n) + 70p \times 398^2 \right) = 2.57 \text{ W}$$

$$P_{Q1} = P_{Q1(COND)} + P_{Q1(SW)} = 3.13 \text{ W} + 2.57 \text{ W} = 5.7 \text{ W}$$

(48)

(49)

### 2.3.3.8 PFC Boost Diode

Reverse recovery losses can be significant in a CCM boost converter, so a silicon carbide diode is chosen here because it has no reverse recovery charge ($Q_{RR}$), and therefore zero reverse recovery losses. The disadvantage is that the cost is higher than that of silicon ultra-fast diodes. The losses are estimated as follows:

$$P_{D1} = V_F \times I_{OUT} = 1.2 \text{ V} \times 1.244 \text{ A} = 2 \text{ W}$$

(50)

### 2.3.3.9 Bulk Capacitor

The value of the bulk capacitor is determined by two factors.

1. The value must be large enough to provide the required hold-up time.
2. The value must be large enough to keep the ripple at twice line frequency within the required limits.

For PC PSU applications, the back-up time is not a target design parameter. Hence, a value of 220 μF is chosen for this particular design. The peak-to-peak ripple voltage at twice line frequency on $C_{BLK}$ is calculated as follows:

$$V_{BLK(ripples)} = \frac{I_{OUT(PFC)}}{2 \pi \times f_{LINE(min)} \times C_{BLK}} = \frac{1.244}{2 \pi \times 50 \text{ Hz} \times 220 \mu F} = 18 \text{ V}$$

(51)

### 2.3.3.10 Sense Resistor

To accommodate the gain of the non-linear power limit, the sense resistor, $R_{SENSE}$, is sized such that it triggers the soft overcurrent at 10% higher than the maximum peak inductor current using the minimum soft overcurrent threshold of the ISENSE pin, VSOC, of ISENSE equal to 0.259 V.

$$R_{SENSE} = \frac{V_{SOC(min)}}{I_{L(PEAK)} \times 1.1} = \frac{0.259}{10.08 \text{ A} \times 1.1} = 0.0234 \Omega$$

(52)

The power dissipated across the sense resistor, $P_{RSENSE}$, must be calculated:

$$P_{RSENSE} = I_{L(RMS(max))}^2 \times R_{SENSE} = 5.94 \text{ A}^2 \times 0.0234 \Omega = 0.826 \text{ W}$$

(53)
3 Hardware, Testing Requirements, and Test Results

3.1 Required Hardware

3.1.1 Testing Conditions

• Input conditions: $V_{\text{IN}}$: 85- to 265-V AC. Set the input current limit to 8 A.
• Output conditions: Electronic load, 0 to 16 V, 600 W.

3.1.2 Equipment Needed

• Isolated AC source
• Single-phase power analyzer
• Digital oscilloscope
• Multimeters
• Electronic load

3.2 Testing and Results

3.2.1 Test Setup

1. Connect input terminals of the reference board to the AC power source.
2. Connect output terminals to electronic load, maintaining correct polarity.
3. Set a minimum load of about 1 A and minimum voltage of 20 V.
4. Gradually increase the input voltage from 0 V to turn on voltage of 85-V AC.
5. Observe that the output voltage across the load terminals has risen to about 12 V.
6. Increase the load and observe the smooth switching waveforms.
7. The user can compare the results with those presented in the design guide.

3.2.2 Test Results

3.2.2.1 Efficiency and Regulation

3.2.2.1.1 Performance Data

<table>
<thead>
<tr>
<th>$V_{\text{INAC}}$ (VAC)</th>
<th>$I_{\text{INAC}}$ (A)</th>
<th>PF</th>
<th>$I_{\text{THD}}$ (%)</th>
<th>$P_{\text{INAC}}$ (W)</th>
<th>$V_{\text{OUT}}$ (V)</th>
<th>$I_{\text{OUT}}$ (A)</th>
<th>$P_{\text{OUT}}$ (W)</th>
<th>EFFICIENCY (%)</th>
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</thead>
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Table 5. At 115-V AC

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<th>V_{INAC} (VAC)</th>
<th>I_{INAC} (A)</th>
<th>PF</th>
<th>I_{THD} (%)</th>
<th>P_{INAC} (W)</th>
<th>V_{OUT} (V)</th>
<th>I_{OUT} (A)</th>
<th>P_{OUT} (W)</th>
<th>EFFICIENCY (%)</th>
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</table>

3.2.2.1.2 Efficiency of Overall System

![Figure 4. Efficiency of Overall System](image)

High level curve: 230 V AC / 50 Hz
Low level curve: 115 V AC / 60 Hz
3.2.2.1.3 Load Regulation

![Graph showing load regulation](image)

**Figure 5. Load Regulation**

3.2.2.2 Waveforms

3.2.2.2.1 PFC Switching Waveforms

**NOTE:**
- CH1: PFC switch node voltage (100 V/div, bandwidth: 20 MHz);
- CH4: PFC inductor current (2 A/div, bandwidth: 20 MHz);
- Test condition: \( V_{\text{IN}} = 115\text{-V AC/60 Hz}; I_{\text{OUT}} = 50\% \text{ load} \)

![Graph showing PFC switching waveforms](image)

**Figure 6. Half Load, 115-V AC/60 Hz, PFC Transient Point**
NOTE: CH1: PFC switch node voltage (100 V/div, bandwidth: 20 MHz);
CH4: PFC inductor current (2 A/div, bandwidth: 20 MHz);
Test condition: \( V_{\text{IN}} = 230\text{-V AC/50 Hz}; I_{\text{OUT}} = 50\% \) load

Figure 7. Half Load, 230-V AC/50 Hz, PFC Transient Point
3.2.2.2 LLC Waveforms

NOTE: CH1: LLC switch node voltage (100 V/div, bandwidth: 20 MHz);
CH4: LLC resonant current (1 A/div, bandwidth: 20 MHz);
Test condition: $V_{IN} = 115$-V AC/60 Hz; $I_{OUT} = 50\%$ load

Figure 8. Half Load, LLC Waveform
3.2.2.2.3 Output Synchronous Rectifier Waveform

**NOTE:**

CH1: Gate driver of SR1 (2 V/div, bandwidth: 20 MHz);
CH2: Gate driver of SR2 (2 V/div, bandwidth: 20 MHz);
CH4: LLC resonant current (1 A/div, bandwidth: 20 MHz);
Test condition: $V_{\text{IN}} = 115$-V AC/60 Hz; $I_{\text{OUT}} = 50\%$ load

![SR Rectifier Gate Driver](image_url)

Figure 9. SR Rectifier Gate Driver
3.2.2.3 Thermal Measurements

This section features two sets of thermal images. These thermal images are taken under room temperature with 500 LFM airflow measured at the board. Figure 10 shows the thermal image for both the top and bottom side of the board. The input voltage is 115-V AC, and the loads are 37.5 A for 12 V\textsubscript{OUT}.

![Figure 10. Thermal Performance at 115-V AC With Full Load](image)

Figure 10 shows the thermal image for both the top and bottom side of the board. The input voltage is 230-V AC, and the loads are 37.5 A for 12 V\textsubscript{OUT}.

![Figure 11. Thermal Performance at 230-V AC With Full Load](image)
3.2.2.4 Conducted Emissions

Generally, conducted emissions will be more at full load. As a result, this operating point is chosen for measuring conducted EMI. The test is performed at an input voltage of 115-V AC and 230-V AC at a 450-W resistive load. The conducted emissions in a pre-compliance test setup are compared against EN55032 class-B limits and meet the Class-B limits comfortably.

Figure 12 and Figure 13 show the results of the test at 230-V AC:

![Figure 12. CE as per EN55032 Class B, L Line at 230-V AC](image)

![Figure 13. CE as per EN55032 Class B, N Line at 230-V AC](image)

Table 6. CE Quasi-Peak and Average Margins Test Result, L Line at 230-V AC

<table>
<thead>
<tr>
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<th>QUASIPEAK (dBµV)</th>
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Table 7. CE Quasi-Peak and Average Margins Test Result, N Line at 230-V AC

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Figure 14 and Figure 15 show the results of the test at 115-V AC:

![Figure 14. CE as per EN55032 Class B, L Line at 115-V AC](image)

Table 8. CE Quasi-Peak and Average Margins Test Result, L Line at 115-V AC

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Figure 15. CE as per EN55032 Class B, N Line at 115-V AC

Table 9. CE Quasi-Peak and Average Margins Test Result, N Line at 115-V AC

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4 Design Files

4.1 Schematics
To download the schematics, see the design files at TIDA-01501.

4.2 Bill of Materials
To download the bill of materials (BOM), see the design files at TIDA-01501.

4.3 PCB Layout Recommendations

4.3.1 Power Stage Specific Guidelines
Key guidelines for routing power stage components:

- Minimize the loop area and trace length of the power path circuits, which contain high-frequency switching currents, on both the primary and secondary sides of the converter. This helps reduce EMI and improve converter overall performance.
- Keep traces with high dV/dt potential and high dI/dt capability away from or shielded from sensitive signal traces.
- Keep power ground and control ground separately for each power supply stage. If they are electrically connected, tie them together at one point near DC input return or output return of the given stage correspondingly.
- When multiple capacitors are used in parallel for current sharing, the layout must be symmetrical across both leads of the capacitors. If the layout is not identical, the capacitor with the lower series trace impedance will see higher currents and become hotter.
- Tie the heat-sinks of all the power switching components to their respective power grounds.
- Place protection devices such as TVS, snubbers, capacitors, or diodes physically close to the device. The devices are intended for protection and hence need to be routed with short traces to reduce inductance.
- Choose the width of PCB traces based on acceptable temperature rise at the rated current per IPC2152 as well as acceptable DC and AC impedances. Also, the traces must withstand the fault currents (such as short-circuit current) before the activation of electronic protection such as fuse or circuit breaker.
- Determine the distances between various circuits according to the requirements of applicable standards such as the UL60950.
- Adapt thermal management to fit the end-equipment requirements.

4.3.2 Controller Specific Guidelines
For PFC controller UCC28180:
- The VBULK is a high-impedance connection and must be shielded by a ground plane from any high-voltage switching nets. The copper area connecting the VBULK pin to the lower resistor or filter capacitor and the last resistor in the high-side divider chain must be kept to a minimum to reduce parasitic capacitance to any nearby switching nets. The bottom resistor in the divider network and filter capacitor must be placed close to the VBULK pin.
- Locate all of the controller support components at specific signal pins (VSENSE, VCOMP, ISENSE, ICOMP, and FREQ) close to their connection pin. Connect the other end of the component to the SGND with the shortest trace length.
- The trace routing for the voltage sensing and current sensing circuit components to the device must be as short as possible to reduce parasitic effects on the current limit, current monitoring accuracy, and voltage monitoring accuracy. These traces must not have any coupling-to-switching signals on the board.
- The optimum placement for a decoupling capacitor is close to the VCC and GND terminals of the device. Take care to minimize the loop area formed by the bypass-capacitor connection and the GND terminal of the device.
For LLC controller UCC256301:

- Put a 2.2-µF ceramic capacitor on VCC pin in addition to the energy storage electrolytic capacitor. The 2.2-µF ceramic capacitor should be put as close as possible to the VCC pin.
- RVCC pin should have a bypass capacitor of 4.7 µF or more. It is recommended to add a 0.1-µF ceramic capacitor in addition to the 4.7 µF. The capacitors should be put as close as possible to the RVCC pin. RVCC cap needs to be at least 5 times of boot capacitor.
- Minimum recommended boot capacitor is 0.1 µF. The minimum value of the boot capacitor needs to be determined by the minimum burst frequency. The boot capacitor should be large enough to hold the bootstrap voltage during the lowest burst frequency. Please refer to the boot leakage current in the electrical table.
- Use large copper pour around GND pin
- The filtering capacitor on BW, ISNS, BLK should be put as close as possible to the pin
- FB trace should be as short as possible
- Soft-start capacitor should be put as close as possible to LL/SS pin
- Use film capacitor or C0G, NP0 ceramic capacitor on VCR divider and ISNS capacitor for low distortion
- It is recommended that ISNS resistor is less than 500 Ω to keep the node impedance low
- Add necessary filtering capacitors on BW pin to filter out the high spikes on the bias winding waveform. It is critical to filter out the high spikes because internally the signal is peak detected and then sampled at the low side turn off edge.
- Do not put any capacitor on HV pin to ground. The layout of this pin should result in low parasitic capacitance (< 60 pF) from HV pin to ground.
- Keep necessary high voltage clearance.

4.3.3 Layout Prints
To download the layer plots, see the design files at TIDA-01501.

4.4 Altium Project
To download the Altium project files, see the design files at TIDA-01501.

4.5 Gerber Files
To download the Gerber files, see the design files at TIDA-01501.

4.6 Assembly Drawings
To download the assembly drawings, see the design files at TIDA-01501.

5 Related Documentation
This reference design did not use any documentation in its creation.

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6 About the Author
CHENG LIU is a systems engineer at Texas Instruments, where he is responsible for developing reference design solutions for the industrial segment. Cheng brings to this role his extensive experience in power electronics, high frequency high power density DC/DC and analog circuit design. Cheng earned his masters of electrical machinery and apparatus from Wuhan University of Technology in 2012.
Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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<td>• Changed Table 4: At 230-V AC</td>
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<td>• Changed Table 5: At 115-V AC</td>
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<td>• Changed Figure 4: Efficiency of Overall System</td>
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<td>• Changed Figure 11: Thermal Performance at 230-V AC With Full Load</td>
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