TI Designs: TIDA-01557
>92% Efficiency, 200-W, <100-mW Standby, Fast Transient, Desktop PC PSU Reference Design

Description
This reference design is a compact, high-efficiency, fast transient, universal input, 12-V DC, 200-W nominal output, AC/DC power supply (PSU) targeted for desktop PCs and gaming adapters. The circuit of the design consists of a front-end transition-mode (TrM) power factor correction (PFC) circuit based on the UCC28056, followed by an LLC stage for isolated DC/DC conversion based on the UCC256301. For high efficiency needs, synchronous rectification is done using the UCC24612-2 synchronous rectifier controller and low $R_{DS(on)}$ MOSFETs CSD18511. This reference design does not need an additional auxiliary PSU to meet no-load and light-load specifications. The design can be used as an AC/DC PSU in applications that demand efficient power conversion and a fast transient response.

Features
- Wide Operating Input Range: 85- to 265-V AC With Full Power Delivery Over Entire Range
- Leading Transient Performance for Line Transient and Dynamic Load: 40-µs Response Time for Step Load Change of 15 A
- Peak Overall Efficiency of 92.47% at 230-V AC and 90.51% at 115-V AC, Fan Cooling Needed up to 55°C Ambient Operation
- High Power Factor > 0.96 at 230-V AC From 50% to 100% Load Meets PFC Regulations and Current THD as per IEC 61000-3-2 Class D
- Very Low No-Load Power Consumption of < 75 mW (Without Synchronous Rectifiers) and < 100 mW (With Synchronous Rectifiers)
- Light Load Efficiency of > 50% at 0.25 W; > 79% at 2 W; > 81% at 4 W
- System Protected for Overcurrent, Short-Circuit, and Overvoltage Ensuring Safety Needs
- Single-Layer, CEM-1 Material PCB Design to Achieve Low Cost
- Small PCB: 70 × 125 × 35 mm and Fits in Both SFX12 and Gaming Adapter Form-Factor
- Designed to Meet Requirements of Conducted Emissions Standard: EN 55022/11 Class B

Applications
- Desktop PC PSUs
- Gaming PCs
- Entry-Level Server PSUs
- Other Low-Cost AC/DC PSUs
System Description

Most power supplies (PSUs) in modern desktop personal computers universally use switched-mode PSUs, which convert mains AC to low-voltage regulated DC power for powering the internal components of a computer. It is the most significant part of the system because it feeds power to the other components, including the CPU, graphics card, hard drive, SSD, and so on. These PSUs need to conform to specifications of desktop platform guidelines such as ATX specifications, which includes form factor and voltage, current, power ratings, environment, safety, EMI/EMC, and acoustics specifications. Newer generation PSUs demand for higher power density and have moved to adopt small form factors such as SFX, micro-ATX, and TFX, which have reduced dimensions compared to standard ATX PSUs. Most of these PSUs feature a single 12-V rail, while others have multiple rails. Multiple output PSUs provide a dedicated 5-V standby (5VSB) voltage so that the standby functions on the computer and certain peripherals are powered, whereas single-output PSUs demand for the 12-V rail itself to operate in high efficiency, providing the required low-wattage standby power.

The global regulatory environment surrounding the legislation of external power supply efficiency and no-load power draw has rapidly evolved in the last decade. The newer generation power supplies need to meet multiple norms such as United States Department of Energy (DoE) Level VI standard, 80PLUS Efficiency level certifications.

This reference design is a high-efficiency and fast transient 200-W AC/DC converter for desktop PC PSUs, gaming PC PSUs, entry-level server PSUs, and other low-cost AC/DC PSUs. The circuit consists of a front-end transition mode (TrM) power factor correction (PFC) circuit, followed by an LLC-based isolated DC/DC power stage. The design uses the UCC28056 controller for the PFC stage and UCC256301 controller for LLC stage to achieve a compact and robust control structure. Synchronous rectification based on the UCC24612 and low R\text{DS(on)} FETs CSD18511 from Texas Instruments help in achieving higher efficiencies.

The converter is designed for a wide input voltage range of 85-V to 265-V AC with full power delivery over the entire range and single DC outputs of 12 V, which have a maximum power output of 200 W, delivering a maximum current of 16.5 A. The design has an operating peak efficiency of around 92.5% with 230-V AC and 90.5% with 115-V AC at half load. The design has a high power factor of > 0.96 at 230-V AC from a 50% to 100% load and meets PFC regulations and current THD as per IEC 61000-3-2 Class D. The design form factor (70 mm × 125 mm) is compact for the power level of 200 W. The single-layer PCB design achieves low cost very well. The system also has some robust protections built in (OVP and OCP), which make the converter more secure and reliable. The EMI filter is designed to meet EN 55022 class-B conducted emission levels. The design meets low standby power of < 100 mW without needing additional auxiliary power.

This reference design is fully tested and validated for various parameters such as regulation, efficiency, EMI signature, output ripple, startup, and switching stresses. Overall, the design meets the key challenges of desktop PC power supplies to provide safe and reliable power with all protections built-in, while delivering high performance with low power consumption and low bill-of-material (BOM) cost.
### 1.1 Key System Specifications

#### Table 1. Key System Specifications

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
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<tr>
<td><strong>INPUT CONDITIONS</strong></td>
<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>Input voltage</td>
<td>$V_{INAC}$</td>
<td></td>
<td>85</td>
<td>230</td>
<td>265</td>
<td>VAC</td>
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<tr>
<td>Frequency</td>
<td>$f_{LINE}$</td>
<td></td>
<td>47</td>
<td>50</td>
<td>63</td>
<td>Hz</td>
</tr>
<tr>
<td>No load power</td>
<td>$P_{SB}$</td>
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<td></td>
<td></td>
<td>100</td>
<td>mW</td>
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<td><strong>OUTPUT CONDITIONS</strong></td>
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<td>Output voltage</td>
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<tr>
<td>Output current</td>
<td></td>
<td></td>
<td>16.5</td>
<td></td>
<td></td>
<td>A</td>
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<td>Line regulation</td>
<td>$V_{O} = 12$ V</td>
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<td>1</td>
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<td></td>
<td>%</td>
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<tr>
<td>Load regulation</td>
<td>$V_{O} = 12$ V</td>
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<td>1</td>
<td></td>
<td></td>
<td>%</td>
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<td>Output voltage ripple</td>
<td>$V_{O} = 12$ V, Peak-Peak</td>
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<td>60</td>
<td>120</td>
<td>mV</td>
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<td>Output power (nominal)</td>
<td>$P_{O}$</td>
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<td>200</td>
<td>W</td>
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<td>Output transient response</td>
<td>$12$-V $V_{O}$: 1-A to 15-A steps, 0.5 A/$\mu$s</td>
<td>±4</td>
<td>±5</td>
<td></td>
<td>%</td>
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<td>Holdup time</td>
<td>$V_{O} = 12$ V, $I_{O} = 13.3$ A (80% load)</td>
<td></td>
<td>30</td>
<td>40</td>
<td>ms</td>
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<td><strong>SYSTEM CHARACTERISTICS</strong></td>
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</tr>
<tr>
<td>Efficiency</td>
<td>$V_{IN} = 230$-V AC RMS and full load at $12$-V output</td>
<td>92.26</td>
<td>%</td>
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<tr>
<td></td>
<td>$V_{IN} = 115$-V AC RMS and full load at $12$-V output</td>
<td>90.37</td>
<td>%</td>
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<td>Power factor</td>
<td>$V_{IN} = 230$-V AC RMS and full load at $12$-V output</td>
<td>0.99</td>
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<tr>
<td></td>
<td>$V_{IN} = 115$-V AC RMS and full load at $12$-V output</td>
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<td>Protections</td>
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<td>Brownout or brown-in</td>
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<tr>
<td>Operating ambient</td>
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<tr>
<td>Standards and norms</td>
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<td></td>
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<tr>
<td>Board form factor (FR4 material, 2 layer)</td>
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<td>70 × 125 × 35</td>
<td>mm</td>
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</tr>
</tbody>
</table>
2 System Overview

2.1 Block Diagram

Figure 1. TIDA-01557 Block Diagram

2.2 Highlighted Products

The following highlighted products are used in this reference design. These sections also highlight the key features for selecting the devices for this reference design. For the complete details of these highlighted devices, see their respective product data sheets.

2.2.1 UCC28056

To implement the high-performance, small form factor, PFC design at 200-W power, the UCC28056 is the preferred controller as it offers series of benefits to address the next generation needs of low THD norms for desktop PC power supplies.

The UCC28056 is a high-performance, small-size, 6-pin, fully featured PFC controller offering excellent light load efficiency and standby power. The UCC28056 controller simplifies the design of a PSU, requiring good power factor that must also be capable of meeting modern tough standards for efficiency and standby power. At a full load, the UCC28056 operates the PFC power stage at maximum switching frequency in TrM. At a reduced load, the part transitions seamlessly into discontinuous conduction mode (DCM), automatically reducing switching frequency for maximum efficiency. At a light load, DCM operation is combined with burst mode operation to further improve light load efficiency and standby power. UCC28056 integrates all the features necessary to implement a high performance and robust PFC stage into a 6-pin package and requires a minimal number of external components to interface with the power stage. This device maximizes the BOM savings by eliminating need of aux winding.

Key specifications for this device include:
• Innovative DCM control law to prevent valley jumping
• Superior no-load and light-load efficiency
• Robust protection: Fast response second OVP on a dedicated pin
• Soft-start and soft recovery after OVP
• Input voltage brownout detection
• Eliminates need of aux winding
• Innovative DCM control law to prevent valley jumping
• Strong drive capability: –1.0 A and +0.8 A

This controller is a companion device to be used with the UCC256301 LLC controller to achieve the best no-load standby power performance.
2.2.2 UCC256301—LLC Controller

LLC resonant converters are one of the most widely used topologies for implementing medium- to high-power, isolated, DC/DC power stages in industrial power supplies. These converters are popular due to their ability to achieve soft-switching (ZVS turnon) for the high-voltage MOSFET and hence improving the overall efficiency of the system.

LLC converters in industrial power supplies do face some specific requirements. Some industrial power supplies need to support an over load (up to 1.5 times the nominal load) for a short period of time. Ensure that the LLC converter does not enter capacitive (ZCS) region during the overload operation; otherwise, it can be catastrophic. The UCC256301 with its ZCS avoidance feature can ensure that the system does not enter the ZCS region under all operating conditions and hence ensures the safety of the system. Apart from the overload (also known as power boost) functionality, industrial power supplies typically need a tunable output voltage with a wide range. For example, for a 24-V nominal output voltage, this can range from 21 V to 28 V. The UCC256301 provides a wide operating frequency range from 35 kHz to 1 MHz to make it easier to design wide output voltage range using an LLC converter.

With its unique hybrid hysteretic control, the UCC256301 provides excellent line and load transient response, minimizing the need for output filter capacitors. Its wide frequency range can reduce the PFC bulk capacitor required to meet the holdup time requirement in the industrial power supplies. With the integrated high-voltage gate drive, X-Cap discharge function, and additional output OVP, the UCC256301 reduces the amount of external discreet components required to implement a high efficiency industrial PSU.

2.2.3 UCC24612

To achieve higher efficiencies at low output voltages, synchronous rectification is inevitable. To achieve high reliability and avoid false triggering and related failures of synchronous rectifiers, a device requires a highly reliable, proven, and fail-proof controller. The UCC24612 meets all the requirements of a synchronous rectifier controller for LLC converters.

The UCC24612 is a multi-mode synchronous rectifier controller for active clamp flyback and LLC applications. With its 4-A sink and 1-A source capability, the proportional gate drive of this device helps in using this synchronous rectifier in LLC applications where the system could be operating way above the resonant frequency. The adaptive off-time feature adds robustness to the synchronous rectifier by preventing false triggering.

2.2.4 CSD18511Q5A—Synchronous FET

To achieve high-efficiency synchronous rectification, TI’s power MOSFET CSD18511Q5A has been employed in this reference design. The CSD18511 is 40-V NexFET™ power MOSFET device available in SON5x6, D2PAK, and TO-220 packages. Its ultra-low resistance minimizes conduction losses, while its ultra-low Qrr minimize reverse recovery losses in this high frequency system.

Key specifications for this device include:
- On-resistance at 10 V (typ): 0.88 mΩ to 4.1 mΩ
- Total gate charge (typ) at 10 V (Qg): 119 nC to 29 nC
- SON5x6, TO-220, and D2PAK packages
2.3 System Design Theory

This reference design provides universal AC mains powered 200-W output at 12 V and 16.5 A. The UCC28056 controls a PFC boost front end, while the UCC256301 LLC resonant-half bridge converts the PFC output to isolated 12 V and 16.5 A. The total system efficiency is 92.5% with a 230-V AC input and over 90.5% with a 110-V AC input at full load. In addition, several protections are embedded into this design which includes input under-voltage protection and output short circuit protection.

Low EMI, high efficiency, high power factor, and reliable power supply are main focus of this reference design for targeted applications.

2.3.1 PFC Regulator Stage Design

PFC circuit shapes the input current of the power supply to maximize the real power available from the mains. In addition, it is important to have the PFC circuit comply with low total harmonic distortion (THD) regulatory requirements such as IEC 61000-3-2. Currently, two modes of operation have been widely used to implement PFC. For higher power circuits (> 300 W), the topology of choice is the boost converter operating in continuous conduction mode (CCM) and with average current mode control. For lower power applications (<250W), typically the Transition Mode (TrM) or Critical Conduction Mode (CrCM) boost topology is used.

For low power levels such as 200 W, it is advisable to use TrM operation as it offers inherent zero-current switching of the boost diodes (no reverse-recovery losses), which permits the use of less expensive diodes without sacrificing efficiency. In addition, variable frequency operation results in distributed EMI spectrum and low emissions.

The design process and component selection for this design are illustrated in the following sections.

To make the designing easier, use the Excel® design calculator in the product folder of this reference design. The design can also be simulated and designed in WEBENCH®.

2.3.1.1 Circuit Component Design—Design Goal Parameters

Table 2 lists the design goal parameters for the PFC converter design. These parameters are used in further calculations to select components.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
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<tr>
<td>INPUT</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input voltage</td>
<td>(V_{AC})</td>
<td>85</td>
<td>230</td>
<td>265</td>
<td>VAC</td>
</tr>
<tr>
<td>Input frequency</td>
<td>(f_{LINE})</td>
<td>47</td>
<td>50</td>
<td>63</td>
<td>Hz</td>
</tr>
<tr>
<td>Brownout voltage</td>
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<td>70</td>
<td></td>
<td></td>
<td>VAC</td>
</tr>
<tr>
<td>Power factor</td>
<td>(PF)</td>
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<td></td>
<td>0.99</td>
<td></td>
</tr>
<tr>
<td>Hold up time</td>
<td>(t_{HOLD})</td>
<td>10</td>
<td></td>
<td>15</td>
<td>ms</td>
</tr>
<tr>
<td>OUTPUT</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output voltage</td>
<td>(V_{DCBUS})</td>
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<td>390</td>
<td>410</td>
<td>VDC</td>
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<tr>
<td>Output power</td>
<td>(P_{DCBUS})</td>
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<td>W</td>
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<td>Line regulation</td>
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<td>&lt;1%</td>
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</tr>
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<td>Load regulation</td>
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<td></td>
<td></td>
<td>&lt;1%</td>
<td></td>
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<tr>
<td>Minimum PFC switching frequency</td>
<td>(f_{SW})</td>
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<td>kHz</td>
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<tr>
<td>Targeted efficiency</td>
<td>(\eta_{PFC})</td>
<td></td>
<td></td>
<td>95%</td>
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</table>
2.3.1.2 Input Current Calculations and Fuse Selection

The input fuse and bridge rectifier are selected based upon the input current calculations. The boost voltage is designed to regulate at 390-V DC for an input AC voltage range of 85-V to 265-V AC operation. The boost PFC converter is designed for output power of 225 W, considering the downstream DC/DC converter operating at > 95% efficiency.

Determine the maximum input power (P_IN) averaged over the AC line period using Equation 1:

\[ P_{IN} = \frac{P_{DCBUS}}{\eta_{PFC}} = \frac{220 \text{ W}}{0.95} = 231.6 \text{ W} \]  

(1)

Determine the maximum average output current (I_{DCBUS(max)}) using Equation 2:

\[ I_{DCBUS(max)} = \frac{P_{DCBUS}}{V_{DCBUS(min)}} = \frac{220 \text{ W}}{390 \text{ VDC}} = 0.564 \text{ A} \]  

(2)

Determine the maximum RMS input current (I_{IN_RMS(max)}) using Equation 3:

\[ I_{IN_RMS(max)} = \frac{P_{DCBUS}}{\eta_{PFC} \times V_{IN(min)} \times PF} = \frac{220 \text{ W}}{0.95 \times 85 \text{ VAC} \times 0.99} = 2.752 \text{ A} \]  

(3)

Determine the maximum input current (I_{IN(max)}) and the maximum average input current (I_{IN_AVG(max)}) based upon the calculated RMS value, assuming the waveform is sinusoidal using Equation 4 and Equation 5, respectively:

\[ I_{IN(max)} = \sqrt{2} \times I_{IN_RMS(max)} = \sqrt{2} \times 2.752 \text{ A} = 3.89 \text{ A} \]  

(4)

\[ I_{IN_AVG(max)} = \frac{2}{\pi} \times I_{IN(max)} = \frac{2}{\pi} \times 3.89 \text{ A} = 2.478 \text{ A} \]  

(5)

2.3.1.3 Bridge Rectifier

The maximum input AC voltage is 265-V AC, so the DC voltage can reach voltage levels of up to 375-V DC. Considering a safety factor of 30%, select a component with voltage rating greater than 500-V DC.

The input bridge rectifier must have an average current capability that exceeds the input average current (I_{IN_AVG(max)}). To optimize the power loss due diode forward voltage drop, a higher current bridge rectifier is recommended.

This reference design uses the 600-V, 15-A diode GBU15L05 for input rectification.

Forward voltage drop of bridge rectifier diode, \( V_{(F_{BRIDGE})} = 0.9 \text{ V} \)

The maximum power loss (at full load and minimum line voltage) in the input bridge (P_{BRIDGE}) can be calculated as using Equation 6:

\[ P_{BRIDGE} = 2 \times V_{(F_{BRIDGE})} \times I_{IN_AVG(max)} = 2 \times 0.9 \text{ V} \times 2.478 \text{ A} = 4.46 \text{ W} \]  

(6)

2.3.1.4 Boost Inductor Design

For a detailed list of equations, see the Boost Inductor Design section of the UCC28056 data sheet.

For the boost inductance value required to ensure that the maximum load can be delivered from the minimum line voltage, use Equation 7:

\[ L_{PFC0} = \frac{V_{LinRMSMin}^2}{110\% \times P_{LdMax}} \times \frac{T_{ONMAX0}}{2} = 200 \mu \text{H} \]  

(7)

The maximum current in the power components will flow while delivering maximum load when supplied from minimum Line voltage. In this condition UCC28056 always operates in transition mode (CRM).

The maximum RMS current of the boost inductor occurs at the minimum line voltage and maximum input power.

\[ I_{LPFCRMSMax} = \frac{2}{\sqrt{3}} \times \frac{110\% \times P_{LdMax}}{V_{LinRMSMin}} = 3.157 \text{ A} \]  

(8)
Based upon the above inductor requirements, a custom magnetic is designed: 200 µH, 4.0-A RMS current and 9.0-A saturation current.

### 2.3.1.5 Boost Switch Selection

For a detailed list of equations, see the Boost Switch Selection section of the UCC28056 data sheet.

The maximum RMS current in the switch occurs at the maximum load and minimum line:

\[
I_{\text{MosRMSMax}} = \frac{110\% \times P_{\text{LdMax}}}{V_{\text{LinRMSMin}}} \times \left[ \frac{4}{3} \times \frac{32 \times \sqrt{2} \times V_{\text{LinRMSMin}}}{9 \times \pi \times V_{\text{OUT}}} \right] = 2.703 \text{ A}
\]

(9)

Select a MOSFET for the boost switch on the following basis:

- The voltage rating must be greater than the maximum output voltage. Under transient or line surge testing the output voltage can rise well above its normal regulation level. For this design example, a MOSFET voltage rating of 600 V is chosen to support a regulated output voltage of 390 V.
- Based upon an acceptable level of conduction loss in the MOSFET, the \(R_{\text{DSon}}\) value required can be calculated from the maximum RMS current. For this design example, an IPP60R190P6 MOSFET from Infineon is selected with \(R_{\text{DSon}}\) at 125°C = 0.36 Ω, giving maximum conduction power loss in the MOSFET below 2.63 W.
- For best efficiency, use a MOSFET that incorporates a fast body diode. Operating with a discontinuous inductor current (DCM) from a low input voltage incurs an additional switching power loss if a MOSFET with slow body diode is used.

### 2.3.1.6 Boost Diode Selection

For a detailed list of equations, see the Boost Diode Selection section of the UCC28056 data sheet.

The maximum RMS current in the boost diode occurs at the maximum load and minimum line:

\[
I_{\text{DioRMSMax}} = \frac{4}{3} \times \frac{110\% \times P_{\text{LdMax}}}{V_{\text{LinRMSMin}}} \times \left[ \frac{2 \times \sqrt{2} \times V_{\text{LinRMS}}}{\pi \times V_{\text{OUT}}} \right] = 1.63 \text{ A}
\]

(10)

Conduction power loss in the boost diode is primarily a function of the average output current.

\[
I_{\text{DioAVGMax}} = \frac{P_{\text{LdMax}}}{V_{\text{OUT}}} = 0.56 \text{ A}
\]

(11)

Select a boost diode on the following basis:

- The boost diode requires the same voltage rating as the boost MOSFET switch.
- The boost diode must have average and RMS current ratings that are higher than the numbers calculated in Equation 10 and Equation 11.
- Diodes are available with a range of different speed and recovery charge. With a low reverse recovery charge, fast diodes typically have a higher forward voltage drop. Therefore, fast diodes have a higher conduction loss but lower switching loss. With high reverse recovery charge, slow diodes typically have a lower forward voltage drop. Therefore, slow diodes have a lower conduction loss but higher switching loss. Maximum efficiency is achieved when the diode speed rating matches the application.

This reference design uses the MUR460 diode from Onsemi. This diode has a voltage rating of 600 V and an average current rating of 4 A. The MUR460 diode has a forward voltage drop of around 0.85 V, giving a conduction loss in the boost diode of less than 0.722 W.

### 2.3.1.7 Output Capacitor Selection

The hold-up time is the main requirement in determining the output capacitance. ESR and the maximum RMS ripple current rating can also be important, especially at higher power levels.

\[
C_{\text{OUT(min)}} \geq \frac{2 \times P_{\text{DCBUS}} \times t_{\text{holdup}}}{\left( V_{\text{DCBUS}}^2 - V_{\text{holdup}}^2 \right)}
\]

(12)

The system needs to have a 16-ms back-up for 80% of the load (176 W).
The holdup voltage is considered as 330 V for continuous operation of the downstream DC/DC converter.

\[ V_{\text{holdup}} = 330 \text{ V} \]

\[ C_{\text{OUT(min)}} \geq \frac{2 \times 176 \text{ W} \times 16.0 \text{ ms}}{(390 \text{ V}^2 - 330 \text{ V}^2)} = 130.4 \mu\text{F} \]  

(13)

Considering a 20% tolerance, the capacitance needed is 156 µF. The actual value used in this reference design is 150 µF.

\[ I_{\text{COUT(RMS)}} = \frac{P_{\text{DCBUS}}}{V_{\text{DCBUS(min)}}} \times \frac{16 \times V_{\text{DCBUS(min)}}}{3 \times \pi \times V_{\text{AC(min)}} \times \sqrt{2}} - 1 \]  

(14)

\[ I_{\text{COUT(RMS)}} = \frac{220 \text{ W}}{330 \text{ V}} \times \frac{16 \times 330 \text{ V}}{3 \times \pi \times 85 \times \sqrt{2}} - 1 = 1.28 \text{ A} \]  

(15)

Based on Equation 14, the 150-µF, 20%, 450-V/1.7-A RMS capacitor is selected.

### 2.3.1.8 Output Voltage Set Point

Select the divider ratio of \( R_{\text{FBtop}} \) and \( R_{\text{FBbottom}} \) to set the \( V_{\text{REF}} \) voltage to 2.5 V at the desired output voltage. The current through the divider is reduced to the least to keep the no load power loss as small as possible. Consider the pullup resistor \( R_{\text{FBtop}} \) to be 9.72 MΩ.

Using the internal 2.5-V reference (\( V_{\text{REF}} \)), the bottom divider resistor (\( R_{\text{FBbottom}} \)) is selected to meet the design goals of the output voltage.

\[ R_{\text{FBbottom}} = \frac{V_{\text{REF}} \times R_{\text{FBtop}}}{V_{\text{OUT}} - V_{\text{REF}}} \]  

(16)

\[ R_{\text{FB2}} = \frac{2.5 \text{ V} \times 9.72 \text{ M} \Omega}{390 \text{ V} - 2.5 \text{ V}} = 62.7 \text{ k} \Omega \]  

(17)

A standard value 61.9-kΩ resistor for \( R_{\text{FB2}} \) results in a nominal output voltage set point of 395 V.

A small capacitor on the VOSNS pin must be added to filter out noise. Limit the value of the filter capacitor such that the RC time constant is limited to approximately 100 µs so as not to significantly reduce the control response time to output voltage deviations.

\[ C_{\text{VOSNS}} = \frac{150 \mu\text{S}}{R_{\text{FBbottom}}} = 2392 \mu\text{F} \]  

(18)

The closest standard value of 2200 pF is used on the VOSNS pin.
2.3.2 LLC Converter Stage Design

The DC/DC stage in an industrial AC/DC converter needs to support a wide output voltage range and a hold-up time of > 20 ms. Combine this requirement with the need to meet the short-time power boost feature, the LLC-based DC/DC stage needs to be designed with sufficient Q and proper operating point to maximize efficiency.

The UCC256301 is with its hybrid hysteretic mode control and ZCS avoidance helps in developing a robust LLC power stage for use in these applications.

Table 3. Design Parameters for LLC Power Stage Design

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage</td>
<td>$V_{\text{INDC}}$</td>
<td>340</td>
<td>397</td>
<td>410</td>
<td>VDC</td>
</tr>
<tr>
<td>Output voltage</td>
<td>$V_{\text{OUT}}$</td>
<td>12</td>
<td></td>
<td></td>
<td>VDC</td>
</tr>
<tr>
<td>Output power limit</td>
<td>$P_{\text{OUT,Max}}$</td>
<td></td>
<td>200</td>
<td></td>
<td>W</td>
</tr>
<tr>
<td>Max output power</td>
<td>$P_{\text{OUT}}$</td>
<td>210</td>
<td></td>
<td></td>
<td>W</td>
</tr>
<tr>
<td>Nominal switching frequency</td>
<td>$f_{\text{SWNOM}}$</td>
<td>100</td>
<td></td>
<td></td>
<td>kHz</td>
</tr>
<tr>
<td>Line regulation</td>
<td></td>
<td>1</td>
<td></td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>Load regulation</td>
<td></td>
<td>1</td>
<td></td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>Targeted efficiency</td>
<td></td>
<td>97</td>
<td></td>
<td></td>
<td>%</td>
</tr>
</tbody>
</table>

2.3.2.1 Determine $M_g$

The transformer turns ratio is determined by Equation 19:

$$n = \frac{2}{\frac{V_{\text{DCIN,NOM}}}{V_O}}$$

(19)

From the specifications, the nominal values for input voltage and output voltage are 397 V and 12 V, respectively, so the turns ratio can be calculated as:

$$n = \frac{2}{12} = 16.54$$

(20)

No additional diode drop needs to be accounted for because a synchronous rectifier is used. The value used for turns ratio ($n$) for further calculations is 16.5.

2.3.2.2 LLC Gain Range $M_g_{\text{min}}$ and $M_g_{\text{max}}$

$M_g_{\text{min}}$ and $M_g_{\text{max}}$ can be determined by using Equation 21 and Equation 23, respectively:

$$M_{g_{\text{min}}} = n \times \frac{V_{O_{\text{min}}}}{\frac{V_{\text{DCIN,Max}}}{2}}$$

(21)

$$M_{g_{\text{min}}} = 16.5 \times \frac{12 \text{ V}}{\frac{410 \text{ V}}{2}} = 0.965$$

(22)
2.3.2.3 Determine Equivalent Load Resistance ($R_E$) of Resonant Network

To determine the equivalent load resistance at nominal and peak load under nominal output voltage and peak output voltage, use Equation 25:

$$R_E = \frac{8 \pi^2 n^2}{\pi^2} \left( \frac{V_{O_{\text{nom}}}}{I_{O_{\text{nom}}}} \right) = \frac{8 \times 16.5^2}{\pi^2} \left( \frac{12}{16.67} \right) = 159.02 \, \Omega$$

(25)

2.3.2.4 Select $L_N/L_R$ Ratio ($L_N$) and $Q_E$

$L_N$ is the ratio between the magnetizing inductance and the resonant inductance.

$$L_N = \frac{L_m}{L_r}$$

(26)

$Q_E$ is the quality factor of the resonant tank.

$$Q_E = \sqrt{\frac{L_r}{C_r R_e}}$$

(27)

Selecting $L_N$ and $Q_E$ values must result in an LLC gain curve, as shown in Figure 2, that intersects with $M_{G(\text{min})}$ and $M_{G(\text{max})}$ traces. The peak gain of the resulting curve must be larger than $M_{G(\text{max})}$.

![Figure 2. LLC Gain Curve for Selected $L_N$ and $Q_E$](image-url)
The relationship between $M_{G(\text{peak})}$ and $Q_E$ with respect to $L_N$ is shown in Figure 3:

![Figure 3. $M_{G(\text{peak})}$ and $Q_E$ With Respect to $L_N$](image)

$L_N = 6$

$Q_E = 0.32$

Use the spreadsheet to get optimized values of $L_N$ and $Q_E$.

### 2.3.2.5 Switching Frequency

The wide switching frequency of the UCC256301 is from 35 kHz to 1 MHz, which makes this reference design more flexible. To make the transformer and inductor with a smaller size and LLC converter, always work under resonant frequency with a 12-V DC output at full load. The second resonant frequency is chosen to be 100 kHz.

$f_0 = 100$ kHz

### 2.3.2.6 Determine Component Parameters for LLC Resonant Circuit

The resonant tank parameters can be calculated using the following:

\[
C_r = \frac{1}{2\pi \times Q_E \times f_0 \times R_E} = \frac{1}{2\pi \times 0.32 \times 100 \text{ kHz} \times 159 \Omega} = 0.03 \mu F
\]

\[
L_r = \frac{1}{(2\pi \times f_0)^2 \times C_r} = \frac{1}{(2\pi \times 100 \text{ kHz})^2 \times 0.03 \mu F} = 84.5 \mu H
\]

\[
L_m = L_N \times L_r = 6 \times 84.5 \mu H = 507 \mu H
\]

After the preliminary parameters are selected, find the closest actual component value that is available, recheck the gain curve with the selected parameters, and then run the time domain simulation to verify the circuit operation. This results in the following resonant tank parameters:

- $C_r = 0.03 \mu F$
- $L_r = 85 \mu H$
- $L_m = 510 \mu H$

Based on the final resonant tank parameters, the resonant frequency can be calculated as follows:

\[
f_0 = \frac{1}{2\pi \sqrt{C_r \times L_r}} = \frac{1}{2\pi \sqrt{0.03 \mu F \times 85 \mu H}} = 99.72 \text{ kHz}
\]
Based on the new LLC gain curve, the normalized switching frequency at maximum and minimum gain are:

- \( F_n(M_{\text{gainmax}}) = 0.65 \)
- \( F_n(M_{\text{gainmin}}) = 0.99 \)

The maximum and minimum switching frequencies are:

- \( f_{SW(\text{min})} = 64.8 \text{ kHz} \)
- \( f_{SW(\text{max})} = 98.7 \text{ kHz} \)

### 2.3.2.7 LLC Primary-Side Currents

The primary-side RMS load current \( I_{\text{pri}} \) with full load is determined using Equation 32:

\[
I_{\text{pri}} = \frac{\pi}{2\sqrt{2}} \times \left( \frac{1}{n} \right) \times \left( \frac{16.67}{16.5} \right) = 1.1214 \text{ A}
\]

The RMS magnetizing current \( I_m \) at \( f_{SW(\text{min})} = 64.8 \text{ kHz} \) is determined using Equation 33:

\[
I_m = \left( \frac{2\sqrt{2}}{\pi} \right) \times \left( \frac{n \times V_{\text{OUT}}}{2\pi \times f_{SW(\text{min})} \times L_m} \right) = \left( \frac{2\sqrt{2}}{\pi} \right) \times \left( \frac{16.5 \times 12}{2\pi \times 64.8 \text{ kHz} \times 510 \mu\text{H}} \right) = 0.859 \text{ A}
\]

The current of the resonant circuit \( I_r \) is determined using Equation 34:

\[
I_r = \sqrt{I_m^2 + I_{\text{pri}}^2} = \sqrt{1.1214^2 + 0.859^2} = 1.412 \text{ A}
\]

This is also the transformer’s primary winding current at \( f_{SW(\text{min})} \).

### 2.3.2.8 Determine Secondary-Side Currents

The total secondary-side RMS load current is the current referred from the primary-side current \( I_{\text{pri}} \) to the secondary side.

\[
I_{\text{sec}} = n \times I_{\text{pri}} = 16.5 \times 1.1214 = 18.5 \text{ A}
\]

Because the transformer’s secondary side has a center-tapped configuration, this current is split equally into two transformer windings on the secondary side. The current of each winding is then calculated using Equation 36:

\[
I_{\text{SW}} = \frac{\sqrt{2} \times I_{\text{sec}}}{2} = \frac{\sqrt{2} \times 18.5}{2} = 13.083 \text{ A}
\]

The corresponding half-wave average current is:

\[
I_{\text{avg}} = \frac{\sqrt{2} \times I_{\text{sec}}}{\pi} = \frac{\sqrt{2} \times 18.5}{\pi} = 8.33 \text{ A}
\]

### 2.3.2.9 Select the Transformer

The transformer can be built or purchased from a catalog. The specifications for this example are as follows:

- Turns ratio (n): 16.5
- Primary terminal voltage: 450-V AC
- Primary winding’s rated current, \( I_{\text{wp}} \): 1.412 A
- Secondary winding’s rated current, \( I_{\text{ws}} \): 14 A (center-tapped configuration)
- Frequency at full load: 95 kHz
- Insulation between primary and secondary sides: IEC 60950 reinforced insulation
2.3.2.10 **Select the Resonant Inductor**

The inductor can be built or purchased from a catalog with these specifications:
- Series resonant inductance, $L_r$: 85 μH
- Rated current, $I_L$: 1.412 A
- Terminal AC voltage: 48.84 V

$$V_{lr} = \omega \times L_r \times I_r = 2\pi \times 64.8 \text{ kHz} \times 85 \mu\text{H} \times 1.412 \text{ A} = 48.84 \text{ V} \quad (38)$$

2.3.2.11 **Select the LLC Resonant Capacitor**

This capacitor carries the full-primary current at a high frequency. A low dissipation factor part is needed to prevent overheating in the part.

The AC voltage across the resonant capacitor is given by its impedance times the current.

$$V_{CR} = \frac{I}{\omega \times C_r} = \frac{1.412}{2\pi \times 64.8 \text{ kHz} \times 0.03 \mu\text{F}} = 115.65 \text{ V} \quad (39)$$

$$V_{CR(rms)} = \left(\frac{V_{IN(max)^2}}{2}\right)^{1/2} + V_{CR}^2 = \sqrt{\left(\frac{410}{2}\right)^2 + 74.9^2} = 235.37 \text{ V} \quad (40)$$

$$V_{CR(rms)} = \frac{V_{IN(max)}}{2} + \sqrt{2} \times V_{CR} = \frac{410}{2} + \sqrt{2} \times 115.65 = 368.5 \text{ V} \quad (41)$$

$$V_{CR(valley)} = \frac{V_{IN(max)}}{2} - \sqrt{2} \times V_{CR} = \frac{410}{2} - \sqrt{2} \times 74.9 = 41.47 \text{ V} \quad (42)$$

Rated current $I_r = 1.412$ A

2.3.2.12 **Select the Primary-Side MOSFETs**

Each MOSFET sees the input voltage as its maximum applied voltage: Choose the MOSFET voltage rating to be 1.5 times of the maximum bulk voltage.

$$V_{DS} = 1.5 \times V_{INDC\_max} = 1.5 \times 410 = 615 \text{ V} \quad (43)$$

Choose the MOSFET current rating to be 1.1 times of the maximum primary side RMS current.

$$I_D = 1.1 \times I_r = 1.1 \times 1.412 = 1.5532 \text{ A} \quad (44)$$

For LLC power stage working in ZVS, the turn-on losses can be neglected. The choice of the MOSFET must be based on $R_{DS\_ON}$ and Coss. Optimizing the Coss helps in minimizing the dead time required for achieving ZVS, thereby minimizing duty cycle loss.

This reference design uses the IPP60R190P6 MOSFET. The feature that optimizes the adaptive dead time of the UCC256301’s helps in maximizing the duty cycle, thereby improving efficiency.

2.3.2.13 **Select the Secondary-Side MOSFETs**

The secondary-side rectifier voltage rating is determined using Equation 45:

$$V_{ds\_max\_sec} = 1.2 \times 2 \times V_{out\_max} = 1.2 \times 2 \times 12 = 28.8 \text{ V} \quad (45)$$

The current rating of the secondary-side MOSFET is determined using Equation 46:

$$I_{mosfet\_sec} = 8.33 \text{ A} \quad (46)$$

This reference design uses TI’s 80-V NexFET CSD18511Q5A with its low $R_{DS\_ON} (< 5.5 \text{ mΩ})$ and $Q_g (< 38 \text{ nC})$. The very low $R_{DS\_ON}$ of the TI NexFET helps in reducing the overall loss in the synchronous rectifier.
2.3.2.14 LLC Output Capacitors

The LLC converter topology does not require an output filter although a small second-stage filter inductor can be useful in reducing peak-to-peak output noise. Assuming that the output capacitors carry the full wave output current of the rectifier, the capacitor ripple current rating is:

\[ I_{\text{RECT}} = \frac{\pi}{2\sqrt{2}} I_o = 1.11 \times 16.67 = 18.5 \text{ A} \]  

(47)

Use a 20-V rating for a 12-V output voltage:

\[ V_{\text{LCap}} = 20 \text{ V} \]

The RMS current rating of the capacitor is:

\[ I_{\text{c(out)}} = \sqrt{\left(\frac{\pi}{2\sqrt{2}} I_o \right)^2 - I_o^2} = \sqrt{\left(\frac{3.14}{2\sqrt{2}} \times 16.67 \right)^2 - 16.67^2} = 8.04 \text{ A} \]  

(48)

The ripple current rating for a single capacitor may not be sufficient, so multiple capacitors are often connected in parallel.

\[ ESR_{\text{max}} = \frac{V_{\text{OUT(pk-pk)}}}{I_{\text{RECT(pk)}}} = \frac{0.12}{2 \frac{\pi}{4} \times 16.67} = 4.58 \text{ m}\Omega \]  

(49)

The capacitor specifications are:

- Voltage rating: 20 V
- Ripple current rating: 8.04 A
- ESR < 4.58 mΩ

2.3.2.15 BLK Pin Voltage Divider

The BLK pin senses the LLC input voltage and determines when to turn on and off the LLC converter. Different versions of the UCC256301 have different BLK thresholds.

Choose the bulk startup voltage at 340 V, then the BLK resistor divider ratio can be calculated using Equation 50:

\[ k_{\text{BLK}} = \frac{340 \text{ V}}{3.05 \text{ V}} = 111.47 \]  

(50)

The desired power consumption of the BLK pin resistor is \( P_{\text{BLKsns}} = 10 \text{ mW} \). The total value of the BLK sense resistor is given by Equation 51:

\[ R_{\text{BLKsns}} = \frac{V_{\text{IN(nom)}}^2}{P_{\text{BLKsns}}} = \frac{397^2}{0.01} = 15.7 \text{ MΩ} \]  

(51)

The lower BLK divider resistor value is given by:

\[ R_{\text{BLKlower}} = \frac{R_{\text{BLKsns}}}{k_{\text{BLK}}} = \frac{15.7 \text{ MΩ}}{111.47} = 140.84 \text{ kΩ} \]  

(52)

The actual value used is 141.38 kΩ

The higher BLK divider resistor value is given by:

\[ R_{\text{BLKupper}} = R_{\text{BLKsns}} - R_{\text{BLKlower}} = \frac{397^2}{0.01} - 140.84 \text{ kΩ} = 15.5 \text{ MΩ} \]  

(53)

Actual value used is 11.7 MΩ

2.3.2.16 BW Pin Voltage Divider

The BW pin senses the output voltage through the bias winding and protects the power stage from overvoltage.
\[
V_{\text{BiasWindingNom}} = 15.2 \text{ V}
\]

The desired OVP threshold in this reference design is 130% of the nominal value. The OVP threshold level in the UCC256301 device is 4 V, so the nominal BW pin voltage is given by:

\[
V_{\text{BWnom}} = \frac{4 \text{ V}}{130\%} = 3.07 \text{ V}
\]  

Choose the lower resistor of the BW resistor divider to be 10 kΩ.

\[
R_{\text{BWlower}} = 10 \text{ kΩ}
\]

The upper resistor can be calculated using Equation 55:

\[
R_{\text{BWupper}} = R_{\text{BWlower}} \times \left( \frac{V_{\text{BiasWindingNom}} - V_{\text{BWnom}}}{V_{\text{BWnom}}} \right) = 10 \text{ kΩ} \times \left( \frac{15.2 - 3.07}{3.07} \right) = 38.85 \text{ kΩ}
\]  

The actual value used is 42.2 kΩ.

2.3.2.17 Soft Start

The soft-start capacitor sets the speed of the soft-start ramp. The soft-start time varies with load condition. At full load or overload condition, the soft-start time is the longest. It is not easy to calculate the exact soft-start time value; however, it can be estimated that under full load condition. The longest possible soft start time is given by:

\[
T_{\text{SS}} = \frac{7 \text{ V} \times C_{\text{SS}}}{25 \text{ μA}}
\]  

Using a 150-nF soft-start capacitor gives the longest possible soft-start time as 42 ms.

2.3.2.18 Current Sense Circuit (ISNS Pin)

The ISNS pin sets the over current protection level. OCP1 is peak current protection level; OCP2 and OCP3 are average current protection levels. The threshold voltages are 0.6 V, 0.8 V, and 4 V, respectively. Set OCP3 level at 150% of full load. Thus, the sensed average input current level at full load is given by:

\[
V_{\text{ISNSfullload}} = \frac{0.6 \text{ V}}{130\%} = 0.4 \text{ V}
\]  

The current sense ratio can then be calculated using Equation 58:

\[
k_{\text{ISNS}} = \frac{V_{\text{ISNSfullload}}}{\frac{P_{\text{OUT}}}{\eta} \times \frac{1}{V_{\text{bulknom}}}} = \frac{0.4 \text{ V}}{\frac{200}{0.97} \times \frac{1}{397}} = 0.77 \Omega
\]  

Select a current sense capacitor first because there are fewer high-voltage capacitor choices than resistors.

\[
C_{\text{ISNS}} = 150 \text{ pF}
\]

Then calculate the required ISNS resistor value:

\[
R_{\text{ISNS}} = \frac{k_{\text{ISNS}} C_{\text{r}}}{C_{\text{ISNS}}} = \frac{0.77 \times 30 \text{ n}}{150 \text{ p}} = 154 \Omega
\]  

The actual value of the current sense resistor used is 160 Ω.

2.3.3 Auxiliary PSU

This reference design does not need an additional auxiliary PSU. The UCC256301 includes a high-voltage startup JFET to initially charge the VCC capacitor to provide the energy needed to start the PFC and LLC power system. Once running, power for the PFC and LLC controllers is derived from a bias winding on the LLC transformer.
3 Hardware, Testing Requirements, and Test Results

3.1 Required Hardware

3.1.1 Testing Conditions

- Input conditions: $V_{\text{in}}$: 85-V to 265-V AC. Set the input current limit to 3 A.
- Output conditions: Electronic load, 0 to 16 V, 330 W

3.1.2 Equipment Needed

- Isolated AC source
- Single-phase power analyzer
- Digital oscilloscope
- Multimeters
- Electronic load

3.1.3 Procedure

1. Connect input terminals (connector J1) of the reference board to the AC power.
2. Connect output terminals (pads marked as $+12 \text{ V}$ and SGND) to electronic load, maintaining correct polarity.
3. Set minimum load of about 50 mA.
4. Gradually increase the input voltage from 0 V to a turn-on voltage of 85-V AC. As the input voltage crosses 85 V, the PFC section start working and boosts the PFC output to 390-V DC.
5. Observe that the output voltage across the load terminals has risen to about 12 V.
6. Increase the load and observe the smooth switching waveforms.
7. Compare the results with those presented in this design guide.
3.2 Testing and Results

3.2.1 Efficiency and Regulation

3.2.1.1 Performance Data

This section shows the efficiency, power factor, iTHD, and load regulation results at 115-V and 230-V AC input conditions.

Table 4 shows the data for $V_{\text{IN}} = 115$-V AC

<table>
<thead>
<tr>
<th>$V_{\text{INAC}}$ (V)</th>
<th>$I_{\text{INAC}}$ (A)</th>
<th>PF</th>
<th>$P_{\text{INAC}}$ (W)</th>
<th>iTHD (%)</th>
<th>$V_{\text{OUT}}$ (V)</th>
<th>$I_{\text{OUT}}$ (A)</th>
<th>$P_{\text{OUT}}$ (W)</th>
<th>EFF (%)</th>
<th>% REG</th>
<th>POWER LOSS (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>115.24</td>
<td>0.37</td>
<td>0.85</td>
<td>35.9</td>
<td>6.83</td>
<td>12.119</td>
<td>2.51</td>
<td>30.4</td>
<td>84.7</td>
<td>0.00</td>
<td>5.63</td>
</tr>
<tr>
<td>115.24</td>
<td>0.61</td>
<td>0.99</td>
<td>69.2</td>
<td>7.62</td>
<td>12.119</td>
<td>5.00</td>
<td>60.6</td>
<td>87.69</td>
<td>0.00</td>
<td>8.58</td>
</tr>
<tr>
<td>115.24</td>
<td>0.89</td>
<td>1.00</td>
<td>101.4</td>
<td>8.76</td>
<td>12.120</td>
<td>7.51</td>
<td>91.0</td>
<td>89.70</td>
<td>0.01</td>
<td>14.79</td>
</tr>
<tr>
<td>115.24</td>
<td>1.18</td>
<td>0.99</td>
<td>134.2</td>
<td>11.45</td>
<td>12.120</td>
<td>10.00</td>
<td>121.2</td>
<td>90.35</td>
<td>0.01</td>
<td>14.70</td>
</tr>
<tr>
<td>115.24</td>
<td>1.47</td>
<td>0.99</td>
<td>167.5</td>
<td>10.03</td>
<td>12.120</td>
<td>12.51</td>
<td>151.6</td>
<td>90.47</td>
<td>0.01</td>
<td>19.64</td>
</tr>
<tr>
<td>115.24</td>
<td>1.71</td>
<td>0.99</td>
<td>194.2</td>
<td>9.28</td>
<td>12.120</td>
<td>14.51</td>
<td>175.8</td>
<td>90.51</td>
<td>0.01</td>
<td>21.12</td>
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<td>115.24</td>
<td>1.97</td>
<td>0.99</td>
<td>223.5</td>
<td>7.01</td>
<td>12.119</td>
<td>16.67</td>
<td>202.0</td>
<td>90.37</td>
<td>0.00</td>
<td>24.10</td>
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<tr>
<td>115.24</td>
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<td>248.7</td>
<td>7.25</td>
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<td>18.50</td>
<td>224.2</td>
<td>90.17</td>
<td>0.01</td>
<td>27.42</td>
</tr>
</tbody>
</table>

Table 5 shows the data for $V_{\text{IN}} = 230$-V AC.

<table>
<thead>
<tr>
<th>$V_{\text{INAC}}$ (V)</th>
<th>$I_{\text{INAC}}$ (A)</th>
<th>PF</th>
<th>$P_{\text{INAC}}$ (W)</th>
<th>iTHD (%)</th>
<th>$V_{\text{OUT}}$ (V)</th>
<th>$I_{\text{OUT}}$ (A)</th>
<th>$P_{\text{OUT}}$ (W)</th>
<th>EFF (%)</th>
<th>% REG</th>
<th>POWER LOSS (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>230</td>
<td>0.20</td>
<td>0.76</td>
<td>34.5</td>
<td>7.46</td>
<td>12.121</td>
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<td>87.9</td>
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<td>4.16</td>
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<td>230</td>
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<td>67.0</td>
<td>4.74</td>
<td>12.122</td>
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<td>60.7</td>
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<td>0.98</td>
<td>98.9</td>
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<td>91.0</td>
<td>91.98</td>
<td>0.00</td>
<td>7.94</td>
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<td>0.99</td>
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<td>4.16</td>
<td>12.122</td>
<td>10.01</td>
<td>121.3</td>
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<td>9.96</td>
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<td>0.99</td>
<td>163.9</td>
<td>4.90</td>
<td>12.123</td>
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<td>151.6</td>
<td>92.47</td>
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<td>12.35</td>
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<td>16.67</td>
<td>202.2</td>
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<td>18.52</td>
<td>224.5</td>
<td>92.12</td>
<td>0.00</td>
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Table 6 shows the readings for $V_{\text{IN}} = 115$-V AC and 230-V AC at a light load with burst mode extended to 105 W.

Table 6. Efficiency at Light Loads

<table>
<thead>
<tr>
<th>OUTPUT POWER (W)</th>
<th>EFF MEASURED (%) at 115-V AC</th>
<th>EFF MEASURED (%) at 230-V AC</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.25</td>
<td>58.40</td>
<td>59.20</td>
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<tr>
<td>0.6</td>
<td>72.30</td>
<td>76.30</td>
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<td>1.5</td>
<td>77.50</td>
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<tr>
<td>2.1</td>
<td>79.30</td>
<td>79.60</td>
</tr>
<tr>
<td>3</td>
<td>80.70</td>
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</tr>
<tr>
<td>4</td>
<td>81.10</td>
<td>81.70</td>
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</table>
Table 7 shows the standby power consumption at \( V_{IN} = 115\text{-V AC} \) and 230-V AC.

### Table 7. Standby Power

<table>
<thead>
<tr>
<th>INPUT VOLTAGE</th>
<th>STANDBY POWER</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>WITHOUT SYNCHRONOUS RECTIFIERS</td>
</tr>
<tr>
<td>115-V AC</td>
<td>55 mW</td>
</tr>
<tr>
<td>230-V AC</td>
<td>71 mW</td>
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</tbody>
</table>

#### 3.2.1.2 Performance Curves

The following figures show the graphs for efficiency, power factor, iTHD, and load regulation, respectively.

![Figure 4. Efficiency](image)

![Figure 5. Power Factor](image)

![Figure 6. iTHD](image)

![Figure 7. Load Regulation](image)
3.2.2 Switching Waveforms

3.2.2.1 PFC Stage Switching Waveforms

This section shows the PFC stage switching waveforms at an input voltage of 115-V AC and 230-V AC at different load conditions.

NOTE: Red trace: PFC switch node voltage; Green trace: PFC inductor current

Figure 8. PFC Switching Node Waveform and Inductor Current at $V_{INAC} = 115$-V AC, Half Load

Figure 9. PFC Switching Node Waveform and Inductor Current at $V_{INAC} = 115$-V AC, Full Load

Figure 10. PFC Switching Node Waveform and Inductor Current at $V_{INAC} = 230$-V AC, Half Load

Figure 11. PFC Switching Node Waveform and Inductor Current at $V_{INAC} = 230$-V AC, Full Load
3.2.2.2 **LLC Stage Switching Waveforms**

This section shows the LLC stage switching waveforms at an input voltage of 230-V AC at different load conditions.

---

**NOTE:**
Red trace: LLC switch node voltage; Green trace: LLC inductor current

---

**Figure 12. Switching Node Waveform and Inductor Current at** $V_{INAC} = 230$-V AC, Half Load

---

**Figure 13. LLC Switching Node Waveform and Inductor Current at** $V_{INAC} = 230$-V AC, Full Load
3.2.3 Input Waveforms

*Figure 14* and *Figure 15* show the input current waveform at 115-V AC at 100-W and 175-W conditions, respectively.

**NOTE:** Red trace: Input AC voltage; Green trace: Input AC current

*Figure 14*. Input Voltage and Current Waveforms at $V_{INAC} = 115$-V AC, 100-W Load

*Figure 15*. Input Voltage and Current Waveforms at $V_{INAC} = 115$-V AC, 175-W Load

*Figure 14* and *Figure 15* show the input current waveform at 230-V AC at 100 W and 200 W conditions, respectively.

**NOTE:** Red trace: Input AC voltage; Green trace: Input AC current

*Figure 16*. Input Voltage and Current Waveforms at $V_{INAC} = 230$-V AC, 100-W Load

*Figure 17*. Input Voltage and Current Waveforms at $V_{INAC} = 230$-V AC, 200-W Load
3.2.4 Hold-up Time Characteristics

Hold-up time is observed at 230-V AC at 80% (~13 A) load conditions. The unit can support full load operation for ~40 ms at 230-V AC operation.

NOTE: Red trace: Output voltage; Yellow trace: Input AC voltage

Figure 18. Holdup With $V_{INAC} = 230$-V AC at 80% Load
3.2.5  Brown-in Turnon and Brownout Turnoff Characteristics

Figure 19 and Figure 20 show the characteristics for brown-in turnon and brownout turnoff, respectively.

**NOTE:** Green trace: Output voltage; Red trace: Input AC voltage

---

**Figure 19. Brown-in Turnon**

**Figure 20. Brownout Turnoff**
### 3.2.6 Inrush Current Waveform

Inrush current drawn by the system is observed and recorded at a maximum input voltage of 230-V AC. Figure 21 shows the corresponding waveform.

**NOTE:** Green trace: Input current; Red trace: Input AC voltage

---

![Figure 21. Inrush Current With \( V_{INAC} = 230\text{-V AC} \)](image-url)
3.2.7 Start-up Time Characteristics

Startup time is observed at 230-V AC under half load (100 W) and no load conditions. Figure 22 and Figure 23 show the start-up time measured.

NOTE: Red trace: Output voltage

![Figure 22. Startup Waveform at V<sub>INAC</sub> = 230-V AC With 100-W Load](image)

![Figure 23. Startup Waveform at V<sub>INAC</sub> = 230-V AC With No Load](image)

3.2.8 Start-up Delay Characteristics

Startup delay is observed at 230-V AC under half load (100 W) and no load conditions. Figure 24 and Figure 25 show the delay measured.

![Figure 24. Startup Waveform at V<sub>INAC</sub> = 230-V AC With 100-W Load](image)

![Figure 25. Startup Waveform at V<sub>INAC</sub> = 230-V AC With No Load](image)
3.2.9 Dynamic Load Characteristics

Load transient performance is observed using an electronic load.

A load step from 1 to 15 A and vice-versa is applied at the output when the converter is operating at an input voltage of 230-V AC and an output voltage of 12-V DC. Figure 26 and Figure 27 show the output voltage transients under load step-up and load step-down, respectively.

NOTE: Red trace: Output voltage; Green trace: Output current

A pulsating load changing from 15 A to 1 A at 110 Hz is applied at the output when the converter is operating at an input voltage of 230-V AC and an output voltage of 12-V DC. Figure 28 shows the response under these conditions.

Figure 26. Step Change of 1 A to 15 A With \( V_{INAC} = 230-V \) AC

Figure 27. Step Change of 15 A to 1 A With \( V_{INAC} = 230-V \) AC

Figure 28. Pulsating Load Change of 15 A to 1 A With \( V_{INAC} = 230-V \) AC
The converter is driven to an overload condition by applying a step change in load from a 60% load to a 120% load. Figure 29 shows the performance of the converter output observed.

3.2.10 Output Ripple

Figure 30 and Figure 31 show the output voltage ripple under 0.3 A (at a 5-ms cycle) and 200 W (at a 10-μs cycle) load conditions at a 230-V AC input, respectively.
### 3.2.11 Short-Circuit Response

A short is applied to observe the output turnoff. When the short is applied, the converter shuts down. Figure 32 shows the output voltage and current waveform under short circuit at an input voltage of 230-V AC and output voltage of 12-V DC.

**NOTE:** Red trace: Output voltage; Green trace: Output current

![Figure 32. Short-Circuit Response](image-url)
4 Design Files

4.1 Schematics
To download the schematics, see the design files at TIDA-01557.

4.2 Bill of Materials
To download the bill of materials (BOM), see the design files at TIDA-01557.

4.3 PCB Layout Recommendations

4.3.1 Power Stage Specific Guidelines
Key guidelines for routing power stage components:

- Minimize the loop area and trace length of the power path circuits, which contain high-frequency switching currents, on both the primary and secondary sides of the converter. This helps reduce EMI and improve converter overall performance.
- Keep traces with high dV/dt potential and high dI/dt capability away from or shielded from sensitive signal.
- Keep power ground and control ground separately for each power supply stage. If they are electrically connected, tie them together at one point near DC input return or output return of the given stage correspondingly.
- When multiple capacitors are used in parallel for current sharing, the layout must be symmetrical across both leads of the capacitors. If the layout is not identical, the capacitor with the lower series trace impedance will see higher currents and become hotter.
- Tie the heat-sinks of all the power switching components to their respective power grounds.
- Place protection devices such as TVS, snubbers, capacitors, or diodes physically close to the device. The devices are intended for protection and hence need to be routed with short traces to reduce inductance.
- Choose the width of PCB traces based on acceptable temperature rise at the rated current per IPC2152 as well as acceptable DC and AC impedances. Also, the traces must withstand the fault currents (such as short-circuit current) before the activation of electronic protection such as fuse or circuit breaker.
- Determine the distances between various circuits according to the requirements of applicable standards such as the UL60950.
- Adapt thermal management to fit the end-equipment requirements.

4.3.2 Controller Specific Guidelines

For the PFC controller UCC28056:

- The VBULK pin is a high-impedance connection and must be shielded by a ground plane from any high-voltage switching nets. The copper area connecting the VBULK pin to the lower resistor or filter capacitor and the last resistor in the high-side divider chain must be kept to a minimum to reduce parasitic capacitance to any nearby switching nets. The bottom resistor in the divider network and filter capacitor must be placed close to the VBULK pin.
- Locate all of the controller support components at specific signal pins (VOSNS, COMP, ZCD/CS, DRV) close to their connection pin. Connect the other end of the component to the SGND with the shortest trace length.
- The trace routing for the voltage sensing and current sensing circuit components to the device must be as short as possible to reduce parasitic effects on the current limit, current monitoring accuracy, and voltage monitoring accuracy. These traces must not have any coupling-to-switching signals on the board.
- The optimum placement for a decoupling capacitor is close to the VCC and GND terminals of the device. Take care to minimize the loop area formed by the bypass-capacitor connection and the GND terminal of the device.
• Take care when placing components and routing at the ZCD/CS pin: Switching edge spikes imposed on the signal feeding this pin can cause its internal ESD structures to conduct causing offset voltage to appear on the capacitive divider feeding this pin. To limit this risk, the voltage divider must be located close to the ZCD/CS pin and away from the region of fast changing magnetic field. Keep all nets between the resistors or capacitors in the divider small to limit capacitive pickup within the divider chain. Connections between the current sense resistor and the UCC28056 must run directly to the terminals of resistor and not be shared with power circuit traces. When laying out the PCB, start with the ZCD/CS pin divider placement and routing to ensure that the needs of this pin come first.

For LLC controller UCC256301:
• Put a 2.2-μF ceramic capacitor on VCC pin in addition to the energy storage electrolytic capacitor. Place the 2.2-μF ceramic capacitor as close as possible to the VCC pin.
• RVCC pin must have a bypass capacitor of 4.7 μF or more. It is recommended to add a 0.1-μF ceramic capacitor in addition to the 4.7 μF. Place the capacitors as close as possible to the RVCC pin. The RVCC cap needs to be at least five times that of the boot capacitor.
• The minimum recommended boot capacitor is 0.1 μF. The minimum value of the boot capacitor needs to be determined by the minimum burst frequency. The boot capacitor must be large enough to hold the bootstrap voltage during the lowest burst frequency. Please refer to the boot leakage current in the electrical table
• Use large copper pour around the GND pin.
• Place the filtering capacitor on BW, ISNS, and BLK as close as possible to the pin.
• FB trace must be as short as possible.
• Place a soft-start capacitor as close as possible to the LL/SS pin.
• Use a film capacitor or C0G, NP0 ceramic capacitor on the VCR divider and ISNS capacitor for low distortion.
• It is recommended that ISNS resistor is less than 500 Ω to keep the node impedance low.
• Add necessary filtering capacitors on the BW pin to filter out the high spikes on the bias winding waveform.
• It is critical to filter out the high spikes because internally the signal is peak detected and then sampled at the low-side turnoff edge.
• Do not put any capacitors on the HV pin to ground. The layout of this pin should result in low parasitic capacitance (< 60 pF) from the HV pin to ground.
• Keep necessary high voltage clearance.

4.3.3 Layout Prints
To download the layer plots, see the design files at TIDA-01557.

4.4 Altium Project
To download the Altium project files, see the design files at TIDA-01557.

4.5 Gerber Files
To download the Gerber files, see the design files at TIDA-01557.

4.6 Assembly Drawings
To download the assembly drawings, see the design files at TIDA-01557.
5 Related Documentation
1. Texas Instruments, *UCC25630x Practical Design Guidelines Application Report*
2. Texas Instruments, *UCC25630x Selection Guide*

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6 About the Authors
LATIF AMEER BABU is a systems architect at Texas Instruments, where he is responsible for developing reference design solutions for the industrial segment. Latif brings to this role his extensive experience in power electronics, high-frequency DC/DC converter, and analog circuit design. Latif earned his master of technology in power electronics and power systems from Indian Institute of Technology, Mumbai, India. Latif is a member of the Institute of Electrical and Electronics Engineers (IEEE) and has one US patent.

YAMINI SHARMA is a systems engineer at Texas Instruments, where she is responsible for developing reference design solutions for the power delivery, industrial segment. Yamini earned her bachelor of technology degree in electronics and communication from Delhi Technological University (formerly DCE), Delhi.
Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (January 2018) to A Revision

<table>
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<td>• Changed standby power from $&lt; 125$ mW to $&lt; 100$ mW</td>
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<td>• Changed no-load power consumption from $&lt; 125$ mW to $&lt; 75$ mW (without synchronous rectifiers) to $&lt; 75$ mW (with synchronous rectifiers)</td>
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<td>• Added Table 7: Standby Power</td>
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