**TI Designs: TIDA-01599**

**Redundant Dual-Channel Reference Design for Safe Torque Off in Variable Speed Drives**

**Description**

This reference design implements safe torque off (STO) functionality in variable speed drives (per IEC61800-5-2) by using dual-channel, isolated STO signals to control the inverter that supplies power to the motor. This design accomplishes STO functionality by enabling or disabling the power to the isolated gate-driver integrated circuit (IC) through the load switches on VCC1 and VCC2. The two switches provide a redundant option to disconnect the primary and secondary side power to the gate driver, respectively. This reference design also provides diagnostic coverage for detecting various faults, which increases the safe failure fraction.

**Resources**

- TIDA-01599 Design Folder
- TIDA-00199 Design Folder
- ISO1212 Product Folder
- TPS27S100 Product Folder
- TPS22860 Product Folder
- ISO5852S Product Folder
- LMZ14201 Product Folder
- TVS3300 Product Folder
- SN74HC7001 Product Folder

**Features**

- Implements Safe Torque Off (STO) to Accomplish Stop Category 0 as Specified in IEC 61800-5-2
- Dual-Channel STO Signals With Multiple Options to Prevent Generation of Torque in Motor:
  - Disconnect Power from Gate Driver IC (on Both Low-Voltage- and High-Voltage Domains)
  - Generate Hardware Trip Signals to terminate PWM Generation Inside MCU
- Self-Diagnostics Coverage Includes Monitoring Safety Pulses and Detecting Various Faults Within Circuit
- ±60-V Input Tolerance With Reverse Polarity Protection Helps Ensures Protection of STO Pins in Case of Faults
- Accurate Output Current Monitoring by High-Side Smart Switch
- Detection of Input and Output UVLO of Gate Driver With RDY Pin Indication
- Option of Latching STO Signals for Additional Protection

**Applications**

- AC Inverter and VF Drives
- Servo Drives

**Important Notice**

An IMPORTANT NOTICE at the end of this TI reference design addresses authorized use, intellectual property matters and other important disclaimers and information.
1 System Description

Motor drives are used in a wide range of applications, such as computer numerical control (CNC) lathes, machining centers, grinders, process control, and so forth. These systems involve the control of machinery, for which safety is always a concern. These applications use drive-based safety functions to reduce the risk from unexpected and hazardous movement. The integrated safety functions within a drive can replace the time-consuming and expensive installation of external safety components like mains contactors or motor contactors. In addition, electronic switching times are significantly quicker than electromechanical devices, such as contactors or relays. The integrated safety functions reduce the risk of personal damage in hazard areas and reduce installation requirements. The function “Safe torque off” (STO) is one such functional safety provision. The STO can be requested or triggered by an error. The built-in STO function does not disconnect the motor from the power supply, but prevents the creation of a rotating magnetic field by disconnecting the control of power semiconductors.

IEC 61800-5-2 defines STO as a function that prevents torque-producing power from supplying the motor. Figure 1 shows implementation of the redundant dual-channel STO. This safety sub-function corresponds to an uncontrolled stop in accordance with stop category 0 of IEC 60204-1. Category 0 defines stopping by immediate removal of power to the machine actuators, that is, an uncontrolled stop. The STO safety function is also useful where power removal is required to prevent an unexpected start-up.

This reference design implements STO using two redundant channels to ensure that the torque-generating energy can be controlled to the motor when the STO inputs have been properly utilized in accordance with IEC/EN 61800-5-2. As long as a logic 1 (+24-V DC) is present at both STO inputs, the motor is operable. If there is a logic 0 (0-V DC) at one or both of the STO inputs, the voltage supply to the motors is interrupted. The STO inputs are of equal value, which means that the sequence in which they are connected does not matter. The controller monitors the status of the STO inputs and switches off the driver supply for the output stages as soon as logic 0 (0 V) is present at one of the STO inputs. Removing the supply voltage to the gate driver IC disables the insulated-gate bipolar transistors (IGBTs) and thus the torque-producing energy. A microcontroller (MCU) runs diagnostics on the STO safety function and monitors the STO signals as well as the health of the safety circuit.

This reference design deals with the circuit-level implementation of two isolated STO signals to turn off the VCC1 and VCC2 of the gate driver. Monitoring has been provided at various points for fault detection. This design guide validates the functionality of the design specifications through data extracted from various test results.

Figure 1. Implementation of Dual-Channel Redundant STO
### 1.1 Key System Specifications

#### Table 1. Key System Specifications

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SPECIFICATIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Absolute maximum input voltage</td>
<td>±60 V</td>
</tr>
<tr>
<td>STO Input</td>
<td>24-V DC (nominal)</td>
</tr>
<tr>
<td>Input logic level</td>
<td>15- to 30-V DC: STO function not engaged (motion allowed)</td>
</tr>
<tr>
<td>Maximum reaction time</td>
<td>&lt; 10 ms</td>
</tr>
<tr>
<td>Maximum duration of test pulse</td>
<td>1 ms</td>
</tr>
<tr>
<td>Maximum frequency of test pulses</td>
<td>500 Hz</td>
</tr>
<tr>
<td>Latching of STO inputs</td>
<td>Yes (through MCU)</td>
</tr>
<tr>
<td>STO feedback</td>
<td>Yes (through MCU)</td>
</tr>
<tr>
<td>Operation ambient temperature</td>
<td>65°C</td>
</tr>
<tr>
<td>Hardware redundancy</td>
<td>1</td>
</tr>
<tr>
<td>Form factor</td>
<td>102 mm × 51 mm</td>
</tr>
</tbody>
</table>
2 System Overview

2.1 Block Diagram

The ISO1212 is a digital input receiver, which accepts the STO inputs. The STO inputs have a ±60-V input tolerance with reverse polarity protection that is compliant to IEC 61131-2 Type 1, 2, and 3 characteristics. The use of ISO1212 reduces the requirement for external discrete components at the input stage. In this design, ISO1212 accepts the 24-V input STO signal and supplies 3.3 V at the output.

As listed in the specifications, the system should reject the STO pulses of less than 1 ms. A low-pass filter has been added to incorporate this requirement. The ANDing of output signals from the ISO1212 device with the MCU enables self-diagnostics to detect various faults.

The TPS27S100 is a high-side switch capable of powering gate drive supplies in drives with ratings up to megawatts (MW) of power. The high-accuracy current monitoring feature of the TPS27S100 enables intelligent control of the load. An adjustable current-limit function greatly improves the reliability of the whole system. The switch is controlled by STO input 2 and supplies power to the TIDA-00199 board, which is an isolated gate driver power supply. The TIDA-00199 board accepts the 24-V, ±20% input range and provides four isolated sets (15 V, –8 V) of bias voltage. In this design, TIDA-00199 is used to provide the bipolar supply to the secondary side of the gate driver.

The TPS22860 is a load switch which is controlled by the STO input 1 and supplies power to the primary side of the gate driver. This switch can support a maximum continuous current of 200 mA. The switch is controlled by an on and off input (ON), which is capable of interfacing directly with low-voltage control signals. This design uses the TPS22860 to provide a supply to the primary side of the gate driver.
2.2 Highlighted Products

2.2.1 ISO1212

Figure 3 shows the pin diagram of the ISO1212. The ISO1212 devices are isolated, 24- to 60-V digital input receivers. These receivers are compliant to IEC 61131-2 Type 1, 2, and 3 characteristics and suitable for programmable logic controllers (PLCs) and motor-control digital input modules. Unlike traditional optocoupler solutions with discrete, imprecise current-limiting circuitry, the ISO121x devices provide a simple, low-power solution with an accurate current limit to enable the design of compact and high-density I/O modules. These devices do not require field-side power.

![ISO1212 Pin Diagram](image-url)
2.2.2 TPS27S100

Figure 4 shows the TPS27S100 functional block diagram. The TPS27S100 is a single-channel, fully-protected, high-side switch with an integrated NMOS and charge pump. An adjustable current-limit function greatly improves the reliability of the whole system. The device diagnostic reporting has two versions to support both digital fault status and analog current monitor output. Accurate current monitor and adjustable current limit features differentiate this device from alternatives in the market.

![Figure 4. TPS27S100 Functional Block Diagram](image)

2.2.3 TPS22860

Figure 5 shows the TPS22860 functional block diagram. The TPS22860 is a small, ultra-low leakage current, single-channel bidirectional load switch. The device requires a $V_{BIAS}$ voltage and can operate over an input voltage range of 0 V to $V_{BIAS}$. The device can support a maximum continuous current of 200 mA. The switch is controlled by an on and off input (ON), which is capable of interfacing directly with low-voltage control signals.

![Figure 5. TPS22860 Functional Block Diagram](image)
2.2.4 ISO5852S

The ISO5852S is an isolated gate driver for IGBTs and MOSFETs. The input CMOS logic and output power stage are separated by a silicon dioxide (SiO$_2$) capacitive isolation. Figure 6 shows the ISO5852S functional block diagram.

![ISO5852S Functional Block Diagram](image)

The I/O circuitry on the input side interfaces with an MCU and consists of gate drive control (IN+/IN–) inputs, RESET (RST) input, READY (RDY) alarm output, and FAULT (FLT) alarm output. The power stage consists of power transistors which supply 2.5-A pullup and 5-A pulldown currents to drive the capacitive load of the external power transistors, as well as the DESAT detection circuitry to monitor the IGBT for collector-emitter overvoltage during short-circuit events. The capacitive isolation core consists of transmit circuitry to couple signals across the capacitive isolation barrier and receive the circuitry to convert the resulting low-swing signals into CMOS levels. The ISO5852S also contains undervoltage lockout (UVLO) circuitry to prevent insufficient gate drive to the external IGBT. Additionally, the ISO5852S offers an active output pulldown feature, which ensures that the gate-driver output is held low if the output supply voltage is absent. The ISO5852S also has an active Miller clamp function which can be used to prevent parasitic turn-on of the external power transistor, due to the Miller effect, for unipolar supply operation.
2.3 Dual-Channel Monitoring

The STO function is realized through two channels, which adds redundancy to the design (see Figure 7). STO1 and STO2, respectively, trigger the removal of power from VCC1 and VCC2 of the gate driver. In a safety unit, if one of the STO signals is removed, then the status changes to “STO triggered”. The unit then waits for a fixed amount of monitoring time to check if both inputs are switched off. If the same signal is not present on both the inputs after the session, then the system signals an error. The PLC performs the monitoring by periodically checking the two stop paths for errors. The PLC performs these checks by sending check pulses of 1-ms duration. The design rejects these 1-ms pulses and the VCC1 and VCC2 of the gate driver does not fall below the UVLO threshold of the device during this time period. For these reasons, this design utilizes an RC low-pass filter to reject the 1-ms pulses from the PLC.

![Figure 7. Dual-Channel Isolated STO](image)

<table>
<thead>
<tr>
<th>STO1</th>
<th>STO2</th>
<th>DESCRIPTION OF STATE</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>STO is triggered and there is no error in STO function.</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>STO is triggered and monitoring for error starts. After some time, error is signaled.</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>STO is triggered and monitoring for error starts. After some time, error is signaled.</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>STO not triggered.</td>
</tr>
</tbody>
</table>

2.4 Diagnostics Coverage

2.4.1 Checking ISO1212 Functionality

As previously addressed, the PLC sends 1-ms pulses to the input of the ISO1212 device. The MCU monitors the output of the device to ensure that the digital isolator is functioning properly. The signals at the output of the MCU, MCU_OUT1 and MCU_OUT2, perform this function.

2.4.2 Checking TPS27S100 Functionality

The MCU interface periodically sends 200-µs pulses for diagnostic purposes. The output of the switch is connected to the general-purpose input/outputs (GPIOs) of the MCU (Monitor_2), as Figure 8 shows by using a resistor divider network.
Figure 8. STO2 Signal Flow Path

The gate driver does not power off during these periodic pulses. This reference design uses a 20-µF capacitor to hold the 24-V secondary supply voltage. The TPS27S100 switch provides full diagnostics by accurately monitoring the output current. The output current is translated into voltage, which is then fed back to the MCU. This feature enables intelligent control of the load.

2.4.3 Checking TPS22860 Functionality

For diagnostic purposes, the MCU interface periodically sends 200-µs pulses. The output of the switch is connected to the GPIOs of the MCU (Monitor_1), as Figure 9 shows. The gate driver not power off during these periodic pulses. A 0.47-µF capacitor is used to hold the 3.3-V primary supply voltage.

Figure 9. Signal Flow Path

2.4.4 RDY Pin of ISO5852S

The I/O circuitry of the ISO5852S device interfaces with an MCU and consists of gate drive control (IN+/IN–) inputs, RESET (RST) input, READY (RDY) alarm output, and FAULT (FLT) alarm output. The output of the gate driver turns off if the VCC1 supply drops below VIT– (UVLO1), irrespective of IN+, IN–, and RST inputs, until VCC1 rises above VIT+ (UVLO1). In a similar manner, the output of the gate driver turns off if the VCC2 supply drops below VIT– (UVLO2), irrespective of IN+, IN–, and RST inputs, until VCC2 rises above VIT+ (UVLO2).

The ready (RDY) pin indicates the status of the UVLO internal protection feature for the input and output sides. If either side of the device has an insufficient supply (VCC1 or VCC2), the RDY pin output goes low; otherwise, the RDY pin output is high. By checking the status of the RDY pin, the signal path from STO1 and STO2 to VCC1 and VCC2 can be monitored.
2.5 PWM Trip Using STO

The trip is generated externally through the hardware and adds redundancy on the STO signal. When the trip is activated, the PWM signal remains low unless a software RESET operation is performed.

Power switching devices can be difficult to control when operating in the proportional region, but are easy to control in the saturation and cutoff regions. PWM is a digital signal by nature and easy for an MCU to generate, which make it ideal for use with power switching devices. Essentially, PWM performs a digital-to-analog converter (DAC) function, where the duty cycle is equivalent to the DAC analog amplitude value. The F2837xD ePWM modules are highly programmable, extremely flexible, and easy to use, while being capable of generating complex pulse width waveforms with minimal CPU overhead or intervention. Each ePWM module is identical with two PWM outputs, EPWMxA and EPWMxB, and multiple modules can be synchronized for simultaneous operation as required by the system application design. The ePWM module consists of eight submodules: time-base, counter-compare, action-qualifier, dead-band generator, PWM chopper, trip-zone, digital-compare, and event-trigger, as Figure 10 shows.

Figure 10. Submodules of PWM Module
2.6 System Design Theory

2.6.1 Digital Input Receiver for STO

The ISO1212 receives 24-V digital signals and provides isolated digital outputs, without the requirement of a field-side power supply. External resistors on the input signal path (R12 and R21) precisely set the limit for the current drawn from the field input. This current limit helps to minimize the power dissipated in the system. The current limit can be set for Type 1, 2, or 3 operation. The voltage transition thresholds are compliant with Type 1, 2, and 3 and can be increased further using an external resistor, R22 and R15.

Figure 11 shows a schematic of the ISO1212 receiver.

As per the specifications of the design, the voltage limits defined for an input voltage of 24 V is as follows:

1. 15- to 30-V DC: STO function not engaged (motion allowed)
2. 0- to 5-V DC: STO function engaged (motion inhibited)

These design requirements comply with Type 1 characteristics.

As the previous Figure 11 shows, Type 1 operation uses a value of $560 \, \Omega$ for R12 and R21 and results in a current limit of 2.25 mA (typical). The relationship between the $R_{\text{SENSE}}$ resistor and the typical current limit ($I_L$) is given by Equation 1.

$$I_L = \frac{2.25 \, \text{mA} \times 562 \, \Omega}{R_{\text{SENSE}}} = \frac{2.25 \, \text{mA} \times 562 \, \Omega}{560 \, \Omega} = 2.25 \, \text{mA}$$

(1)

Resistors R22 and R15 set the voltage thresholds (VIH and VIL) in addition to limiting the surge current. Use a resistor of 2.5 kΩ for R22 and R15 for a Type 1 system. Equation 2 and Equation 3 are used to calculate the typical VIH and VIL values, respectively.
Time Constant $R \times C = 1 \text{ K} \times 3.3 \text{ µF} = 3.3 \text{ µsec}$

As per the design specifications, low STO pulses that are less than 1 ms are rejected. Address this rejection by placing a low-pass filter at the output signals of the ISO1212 device. To meet the design requirements, place an RC combination with $R = 1 \text{ K}$ and $C = 3.3 \text{ µF}$ (see Equation 4).

The cutoff frequency of this filter is 48 Hz, where:

- $V(t) = 3.3$,
- At $t = 1 \text{ ms}$,
- $V(t) = 2.8 \text{ V}$, which is within the logic threshold high range of the AND gate.

### 2.6.2 STO2 Signal Flow Path

#### 2.6.2.1 High-Side Switch for Controlling Secondary-Side Supply Voltage of Gate Driver

The TPS27S100x is a single-channel, fully-protected, high-side switch with an integrated NMOS and charge pump. An external adjustable current limit improves the reliability of the whole system by clamping the inrush or overload current. Figure 12 shows the schematic design of the TPS27S100.

![Figure 12. TPS27S100 Schematic](image)

Equation 5 calculates the value of resistor R4, which is required to keep the 1-A nominal current in the 0-to 3.3-V current-sense range. To achieve better current-sense accuracy, a 1% tolerance or better resistor is preferred.

$$R4 = \frac{V_{(IMON)} \times K_{(IMON)}}{I_{OUT}} = \frac{3.3 \text{ V} \times 500}{1 \text{ A}} = 1.65 \text{ k}$$

The value of resistor R4 is selected as 1.65 K.

To set the adjustable current limit value at 1 A, calculate R7 using Equation 6.

$$R7 = \frac{VLIM_{(TH)} \times K_{(LIM)}}{I_{OUT}} = \frac{1.233 \text{ V} \times 2000}{1 \text{ A}} = 2.47 \text{ K}$$

The enable pin is permanently connected to 3.3 V to enable continuous diagnostic monitoring.

#### 2.6.2.2 Powering up Secondary Side: VCC2 of Gate Driver

The output of the smart switch is connected to J4 for powering up the TIDA-00199 board. The TIDA-00199 design generates a bipolar supply of +15 V, 0 V and –8 V, which powers up the secondary side of the isolated gate driver, ISO5852S on the TIDA-01599 board. For a detailed design procedure, see Wide-Input Isolated IGBT Gate-Drive Fly-Buck™ Power Supply for Three-Phase Inverters.
2.6.3 STO1 Signal Flow Path for Controlling VCC1

The TPS22860 is a small, ultra-low leakage current, single-channel load switch. Figure 13 shows the schematic design of the TPS22860.

![Figure 13. TPS22860 Schematic](image)

The device operates at a bias voltage of 3.3 V and can operate over an input voltage 0 V to V\textsubscript{BIAS}. To limit the voltage drop on the input supply, which is caused by transient inrush currents when the switch turns on into a discharged load capacitor, a ceramic capacitor of 1 µF is placed between the VIN and GND pins. The output of the switch is connected to the primary 3.3-V supply of the gate driver.

2.6.4 Gate Driver Design

Figure 14 shows the schematic design of the isolated gate driver. VCC1 and GND1 are the supply pins for the input side of the ISO5852S device. The supply voltage at VCC1 can range from 3.0 V to 5.5 V with respect to GND1. VCC2 and GND2 are the supply pins for the output side of the ISO5852S device. VEE2 is the supply return for the output driver and GND2 is the reference for the logic circuitry. The supply voltage at VCC2 can range from 15 V up to 30 V with respect to VEE2. The PWM is applied across the IN+ and IN– pins of the gate driver.

![Figure 14. ISO5852S Schematic](image)
On the secondary-side of the gate driver, gate resistors R27 and R28 control the gate current of the switching device. The DESAT fault detection prevents any destruction resulting from excessive collector currents during a short-circuit fault. To prevent damage to the switching device, the ISO5852S slowly turns off the IGBT in the event of a fault detection. A slow turnoff ensures the overcurrent is reduced in a controlled manner during the fault condition. The DESAT diode D3 conducts the bias current from the gate driver, which allows sensing of the IGBT-saturated collector-to-emitter voltage when the IGBT is in the ON condition. D1 blocks high voltage when the IGBT is in the OFF condition. In this reference design, D1 blocks a maximum of 1200 V during the IGBT OFF condition. Switching inductive loads causes large, instantaneous forward-voltage transients across the freewheeling diodes of IGBTs. These transients result in a large negative spike in the DESAT pin, which draws substantial current out of the device. To limit this current below damaging levels, a 1-kΩ resistor is connected in series with the DESAT diode. A 220-pF blanking capacitor C10 is required, which disables the DESAT detection during the OFF-to-ON transition of the power device. For a detailed design procedure, see Isolated IGBT Gate Driver Evaluation Platform for 3-Phase Inverter System.

2.6.5 Generation of 3.3-V Power Rail

The LMZ14201 is a step-down DC-to-DC power module. This device is typically used to convert a higher DC voltage to a lower DC voltage with a maximum output current of 1 A. This design uses the LMZ14201 to convert the 24-V input to 3.3 V. Figure 15 shows the schematic design of the LMZ14201.

The output voltage is determined by a divider of two resistors connected between V\text{O} and ground. The midpoint of the divider is connected to the FB input. The voltage at FB is compared to a 0.8-V internal reference. In normal operation, an ON-time cycle is initiated when the voltage on the FB pin falls below 0.8 V. The main MOSFET ON-time cycle causes the output voltage to rise and the voltage at the FB to exceed 0.8 V. As long as the voltage at FB is above 0.8 V, ON-time cycles will not occur.

Equation 7 calculates the regulated output voltage determined by the external divider resistors R26 and R42.

\[
V_O = 0.8 \, V \times \left(1 + \frac{R26}{R42}\right)
\]

Choose these resistors from values in the range of 1.0 kΩ to 10.0 kΩ.

The TIDA-01599 reference design uses R26 as 3.32 k and R22 as 1.07 k to generate the 3.3-V output voltage.
3 Hardware, Software, Testing Requirements, and Test Results

3.1 Getting Started Hardware

3.1.1 PCB Overview

Figure 16 shows a top view of the printed-circuit board (PCB).

The TIDA-01599 board is very compact with 102×51-mm dimensions.

J5 is a six-pin connector, which provides an input to the two 24-V STO signals. J1 is a 24-V connector, which powers up the high-side load switch. The 3.3-V rail is generated on the board, which supplies power to the digital isolator, AND gate, low-side switch, and MCU. J4 and J8 are the connectors which supply 24 V and 3.3 V, respectively, from the output of the two switches.

J6 and J7 are female connectors, which have been set 52-mm apart for interfacing to the C2000™ MCU LaunchPad™ Development Kit.
3.2 Testing and Results

3.2.1 Logic High and Logic Low STO Thresholds

Figure 17, Figure 18, and Figure 19 show the input logic high and low thresholds of the ISO1212. Note that the VIH (min) is 14.20 V and VIL (max) is 11.20 V, which correlates with the typical values calculated in Section 2.6.1.

Figure 17. Logic Threshold for Digital Isolator

Figure 18. Logic Thresholds for Digital Isolator—Falling Edges

Figure 19. Logic Thresholds for Digital Isolator—Rising Edges
3.2.2 Validation of STO1 Signal

3.2.2.1 Propagation of STO1 to VCC1 of Gate Driver

The STO1 signal goes low for a period of 15 ms. As Figure 20 and Figure 21 show, the response time measured between the STO signal going low to the activation of the RDY pin is 2.7 ms. The response time is a function of the capacitance C16 at the output of the load switch. Vary the response time by changing the value of capacitance. As the VCC1 goes below the UVLO threshold, the RDY pin is activated. The UVLO+ threshold for ISO5852S is 2.25 V.

![Figure 20. Propagation of STO1 to VCC1 of Gate Driver](image)

![Figure 21. Indication of RDY Signal (Active Low) When VCC1 Turns OFF](image)

3.2.2.2 1-ms STO Pulse Rejection

The low-pass filter at the output of the digital isolator rejects the STO low pulse of 1 ms, as Figure 22 and Figure 23 show.

![Figure 22. Rejection of 1-ms Pulse by LPF on STO1 Signal Path](image)

![Figure 23. Rejection of 1-ms Pulse by LPF on STO1 Signal Path—RDY Pin Remains High](image)
3.2.2.3 Diagnostic Pulses from MCU Interface

The MCU periodically sends low pulses of 100 µs. The VCC1 does not fall much below the UVLO of the gate driver during this time period. A capacitor of 0.47 µF ensures that VCC_1 does not fall below the UVLO threshold. Use a higher value of capacitance to minimize the voltage drop in VCC1 during the 100-µs STO pulses. Figure 24 shows the test results.

![Figure 24. Effect of Diagnostic Pulses From MCU Interface on STO1 Signal Path](image)

3.2.3 Validation of STO2 Signals

3.2.3.1 Propagation of STO2 to VCC2 of Gate Driver

The STO2 signal goes low for a period of 15 ms. As Figure 25 and Figure 26 show, the response time measured between the STO signal going low to the activation of the RDY pin is 7.4 ms. As the VCC2 goes below the UVLO threshold, the RDY pin is activated. The UVLO+ threshold for ISO5852S is 12 V. The response time is a function of the capacitance C7 at the output of the smart switch. Vary the response time by changing the value of capacitance.

![Figure 25. Indication of RDY Signal (Active Low) When VCC_2 Turns OFF](image)

![Figure 26. Propagation of STO2 to VCC2 of Gate Driver](image)
### 3.2.3.2 1-ms Pulse Rejection

The low-pass filter at the output of the digital isolator rejects the STO low pulse of 1 ms, as Figure 27 and Figure 28 show.

![Figure 27. Rejection of 1-ms Pulse by LPF on STO2 Signal Path—RDY Pin Remains High](image)

![Figure 28. Rejection of 1-ms Pulse by LPF on STO2 Signal Path](image)

### 3.2.3.3 Diagnostic Pulses From MCU

The MCU periodically sends low pulses of 100 µs. The VCC1 does not fall much below the UVLO of the gate driver during this time period. This has been taken care of by using a capacitor C7 of 10 uF at the output of the switch. Figure 29 shows the test results. Use a higher value of capacitance to minimize the voltage drop in VCC2 during the 100-µs STO pulses.

![Figure 29. Effect of Diagnostic Pulses From MCU Interface on STO2 Signal Path](image)

### 3.2.3.4 Inrush Current Measurement

The current limit can be set by the TPS27S00 device. As mentioned in Section 2.6, the current limit is set to 1 A. The current during the peaks is limited to 1 A, as calculated in the following Equation 8.

\[
I_{\text{OUT}} = \frac{V_{\text{(MON)}} \times K_{\text{(MON)}}}{R4} = \frac{3.3 \, \text{V} \times 500}{1.65 \, \text{K}} = 1 \, \text{A}
\]  

(8)

The current in the switch during the ON state can be calculated as follows in Equation 9.

\[
I_{\text{OUT}} = \frac{V_{\text{(MON)}} \times K_{\text{(MON)}}}{R4} = \frac{0.3 \, \text{V} \times 500}{1.65 \, \text{K}} = 90 \, \text{mA}
\]  

(9)
This calculated value for $I_{OUT}$ matches well with the value measured by the multimeter (see Figure 30 and Figure 31).

The two peaks that Figure 30 and Figure 31 show during the transition state corresponds to the current limit due to the input and output capacitance of the TIDA-00199 board. Path 1 and path 2 in Figure 32 shows the two capacitances charging on the TIDA-00199 board.

![Diagram](Figure 32. Charging of Input and Output Capacitors of TIDA-00199)

### 3.2.4 3.3-V Voltage Rail From Switcher

Figure 33 and Figure 34 show the ripple voltage on the 3.3-V rail at a load current of 13 mA. The peak-to-peak ripple voltage at 13 mA is 27.75 mV.
Figure 35 and Figure 36 show the ripple voltage on the 3.3-V rail at a load current of 40 mA. The peak-to-peak ripple voltage at 40 mA is 33 mV.

![Figure 35. Ripple Voltage at Load Current of 40 mA](image1)

![Figure 36. Zoomed-in Ripple Voltage at Load Current of 40 mA](image2)

3.2.5 60-V Input Voltage and Reverse Polarity Protection

Figure 37 and Figure 38 show that, when a positive and negative voltage of 60 V is applied at the input of the digital isolator, the output remains unaffected.

![Figure 37. 60-V Input Voltage Protection](image3)

![Figure 38. 60-V Reverse Polarity Protection](image4)
3.2.6 Validation of Trip Zone Functionality

Figure 39 shows the implementation of the trip feature. As the STO goes low, the trip starts to fall. Within a time period of 1.52 ms, the input PWM to the gate driver (and hence the output to the gate of the switching device) is terminated.

![Figure 39. Validation of Trip Zone Functionality Through STO2](image)

Figure 39. Validation of Trip Zone Functionality Through STO2

Figure 40 shows the rejection of a 1-ms STO low pulse by the design.

![Figure 40. Effect of Rejection: 1-ms Pulse on Trip](image)

Figure 40. Effect of Rejection: 1-ms Pulse on Trip
4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01599.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01599.

4.3 PCB Layout Recommendations

4.3.1 Splitting Ground and Power Plane

Figure 41 and Figure 42 show the split in the ground and power plane. The ground is split into two planes: DGND and GND_S. DGND serves as the ground for the secondary side of the ISO1212, LMZ1420, TPS27S100, TPS22860, and SN74HC7001 devices and the primary side of the ISO5852S device. GND_S is the reference for the logic circuitry on the secondary side of the isolated gate driver.

Figure 41. Split in Ground Plane of Layout
The power plane has been divided as shown in Figure 41 as a 3.3-, 24-, –8-, and 15-V plane.

4.3.2 Layout Recommendations for ISO1212

Figure 43 shows the layout of the isolated digital input receiver. Sense resistors R21 and R12 are placed on the field side. Input capacitors C8, C11 and resistors R22, R15 are placed on the top layer. The capacitor $C_{IN}$ is placed as close to the ISO1212 device as possible. The SUB1 and SUB2 pins on the ISO1212 device are left disconnected. The voltage must not be placed within 4 mm of the ISO12112 device pins or the CIN and RSENSE pins to avoid flashover during electromagnetic compatibility (EMC) tests. The decoupling capacitor, C14, is placed on the top layer of the board.
4.3.3 Layout Recommendations for ISO5852S

Figure 44 shows the top and bottom layer with the power plane for the isolated gate driver.

Figure 44. Isolated Gate Driver—Top and Bottom Layer

Be sure to consider the following points when performing the layout for the isolated gate driver:

- Maintain a minimum spacing of 8 mm between the primary and secondary sides to ensure reinforced isolation.
- The bypass capacitors on the primary and secondary side of the gate driver must be placed as close to the supply pins as possible.
- Routing the high-current or sensitive traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the gate driver, MCU, and power transistors. Gate driver control input, gate driver output OUTH/L, and DESAT must be routed in the top layer.
- Routing the slower-speed control signals on the bottom layer allows for greater flexibility because these signal links usually have enough margin to tolerate discontinuities such as vias.

4.3.4 Layout Prints

To download the layer plots, see the design files at TIDA-01599.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-01599.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01599.
4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01599.

5 Related Documentation

1. Texas Instruments, *Wide-Input Isolated IGBT Gate-Drive Fly-Buck™ Power Supply for Three-Phase Inverters*
2. Texas Instruments, *Three-Phase High PWM Frequency GaN Inverter Reference Design for 200-V AC Servo Drives*

5.1 Trademarks

E2E, Fly-Buck, C2000, LaunchPad are trademarks of Texas Instruments.

6 About the Author

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7 Recognition

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