High-Efficiency, 1.6-kW High-Density GaN-Based 1-MHz CrM Totem-Pole PFC Converter Reference Design

Description

High-frequency, critical-conduction-mode (CrM), totem-pole power factor correction (PFC) is a simple approach for designing high-density power solutions using GaN. This reference design uses TI's 600-V GaN power stage LMG3410, and TI's Piccolo™ F280049 controller. This high-density (165 × 84 × 40 mm) two-stage interleaved 1.6-kW design is ideal for many space-constrained applications, such as servers, telecom, and industrial power supplies. Interleaving of the power stages reduces input and output ripple currents.

Features

- Compact Power Stage of Size 65 × 40 × 40 mm With Power Density of Greater Than 250 W/in³
- Super High Efficiency of 98.7% at Full Load and 230-V AC Input
- TI's LMG3410 GaN Power Stage With Integrated Driver and Protection Ensures Circuit Reliability and Eases Design
- Full Digital Control Using TI's Piccolo™ F280049 Controller
- Wide Operating Input Range: 85-V to 265-V AC
- High Power Factor Greater Than 0.99 and Low THD; Meets Current THD Regulations as per IEC 61000-3-2
- Protects for Output Overcurrent, Overvoltage, and Undervoltage Conditions
- External Cooling Not Required; up to 55°C Ambient Operation for Loads ≤ 800 W
- Built-in 10-W Supply for Housekeeping Power Needs and System Fan Driving

Applications

- Server and Network Power Supplies
- Telecom Rectifiers
- Industrial Power Supplies

Resources

- TIDA-00961 Design Folder
- LMG3410-HB-EVM Design Folder
- TMDXDOCK280049C Design Folder
- UCC27712 Product Folder
- TLV3502 Product Folder
- OPA237 Product Folder
- LMV612 Product Folder
- SN74LVC1G3157 Product Folder
- CD74HC74 Product Folder
- TPS62153 Product Folder
- UCC28740 Product Folder
- TLV431A Product Folder
- TS3V330 Product Folder
- LP2986 Product Folder

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# System Description

The main power supplies used in telecom, server, and industrial power supply unit (PSU) systems convert AC line power to an isolated constant DC voltage output suitable for the loads they power: typically, 12 V for server PSUs, 48 V for telecom rectifiers, and 24 V for industrial PSUs. These main power supply systems range typically from 1 kW to 5 kW. All of these systems require a front-end power factor correction (PFC) circuit to shape the input current of the power supply, so as to meet the power factor and current total harmonic distortion (THD) norms defined in IEC61000-2-3.

In this design, the PFC circuit shapes the input current of the power supply to be in phase with the mains voltage, and helps maximize the real power drawn from the mains. The PFC front end also offers several benefits, which include the reduction in input root mean square (RMS) current, facilitation of hold-up during brief power interruptions, improvement of efficiency of downstream converters, and reduction of current stresses in neutral conductors in Y-connected three-phase systems. Figure 1 shows the typical location of the PFC circuit within the main PSU.

**Figure 1. Block Diagram of Main Power Stage of Network and Server PSU**

Requirements for PFC front ends have undergone considerable changes over the last few years due to increasing demands for smaller size and higher efficiency. The challenge to meet premium levels of 80 plus standards calls for very-high efficiency over wide operating ranges of input and output. This need for high efficiency has generated considerable interest in bridgeless topologies for the PFC stage that can push the efficiency above 99%. Because of the need for both smaller size and higher efficiency, simpler topologies that use fewer components and are capable of switching at higher frequencies are the current requirement in the PFC front end. The adoption of topologies using GaN power devices is relevant in this context. The Gallium-Nitride (GaN) power stage allows the implementation of bridgeless totem-pole topologies for PFC, which would be difficult to implement using silicon MOSFETs. The transition mode operation of the totem-pole power stage, when extended to zero voltage switching, lets the switching frequency increase into the MHz range.

This reference design is an attempt to meet the above challenges of telecom, server, and industrial power supplies. This design uses the fast switching capability of the driver-integrated GaN field-effect transistor (FET) from TI (LMG3410) and the advanced features of TI’s C2000™ Piccolo™ TMS320F280049 microcontroller (MCU) to realize a totem-pole PFC with fast switching (up to 1 MHz) and zero-voltage switching-on (ZVS) transition capability. Two-channel interleaving is used to demonstrate the design’s capability to cater to higher power applications by adding parallel interleaved power stages. High efficiency of above 99% is demonstrated, though it is possible to further improve it by optimizing the design of the magnetics. The design can meet the power factor (PF) and current THD requirements applicable to the systems addressed. The main features of this reference design are the high switching frequency (made possible due to the LMG3410 GaN power switches), ZVS operation (made easier by the advanced features of F280049), bridgeless transition-mode totem-pole operation, and interleaving the transition mode operation.
# 1.1 Key System Specifications

Table 1. Key System Specifications

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
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<tr>
<td><strong>INPUT CONDITIONS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Input voltage (V&lt;sub&gt;INAC&lt;/sub&gt;)</td>
<td>—</td>
<td>85</td>
<td>230</td>
<td>265</td>
<td>V AC</td>
</tr>
<tr>
<td>Frequency (f&lt;sub&gt;LIN&lt;/sub&gt;)</td>
<td>—</td>
<td>47</td>
<td>50/60</td>
<td>63</td>
<td>Hz</td>
</tr>
<tr>
<td>No load power (P&lt;sub&gt;NL&lt;/sub&gt;)</td>
<td>V&lt;sub&gt;INAC&lt;/sub&gt; = 230 V, I&lt;sub&gt;OUT&lt;/sub&gt; = 0 A</td>
<td>—</td>
<td>—</td>
<td>1</td>
<td>W</td>
</tr>
<tr>
<td><strong>OUTPUT CONDITIONS</strong></td>
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<td>V DC</td>
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<td>4.1</td>
<td>A</td>
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<td>Line regulation</td>
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<td>—</td>
<td>—</td>
<td>0.5%</td>
<td></td>
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<td>Load regulation</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>0.5%</td>
<td></td>
</tr>
<tr>
<td>Output ripple</td>
<td>Peak-to-peak</td>
<td>25</td>
<td>—</td>
<td></td>
<td>V</td>
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<tr>
<td>Output power</td>
<td>V&lt;sub&gt;INAC&lt;/sub&gt; = 230 V</td>
<td>—</td>
<td>1600</td>
<td>—</td>
<td>W</td>
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<td></td>
<td>V&lt;sub&gt;INAC&lt;/sub&gt; = 120 V</td>
<td>—</td>
<td>1200</td>
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<td>W</td>
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<td><strong>SYSTEM CHARACTERISTICS</strong></td>
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<tr>
<td>Efficiency (η)</td>
<td>V&lt;sub&gt;N&lt;/sub&gt; = V&lt;sub&gt;NOM&lt;/sub&gt; and full load</td>
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<td>Operating ambient</td>
<td>Open frame, 200LFM</td>
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<td>25</td>
<td>55</td>
<td>°C</td>
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<td>Power line harmonics</td>
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<tr>
<td>Board size</td>
<td>Length × width × height</td>
<td>165 × 84 × 40</td>
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<td>mm</td>
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</table>
2 System Overview

2.1 Block Diagram

Figure 2. Block Diagram of 1.6-kW PFC Regulator

Figure 2 shows the high-level block diagram of the design. Use the TMS320F280049 C2000 Piccolo control card and two LMG3410 GaN daughter cards with the TIDA-00961 power stage. Daughter cards are used for each of the half-bridge switching power stages and the controller. An onboard auxiliary power supply for housekeeping and fan is implemented using the UCC28740. A silicon MOSFET-based synchronous rectifier driven by the UCC27712 half-bridge driver reduces power loss in the low-frequency half bridge at the input. The input current is sensed by a Hall-effect sensor, the output of which is processed by a variable-gain amplifier stage built using an OPA237 amplifier to get better accuracy at low current levels.

2.2 Highlighted Products

This reference design features the following devices, selected based on their specifications and relevance for this design. For more information on each of these devices, see their respective product folders at TI.com; linked below Resources.

2.2.1 TMS320F280049—C2000™ Piccolo™ controlCARD

The F280049C Experimenter’s Kit from Texas Instruments is an ideal kit for software development and evaluation of the TMS320F280049C MCU. It is a board-level module that uses the HSEC controlCARD form factor, a common interface used in C2000 kits, and can be used in conjunction with other C2000 application kits.

The Piccolo TMS320F28004x series is a powerful 32-bit floating-point MCU that lets designers incorporate crucial control peripherals, differentiated analog, and nonvolatile memory on a single device.
The real-time control subsystem is based on TI’s 32-bit C28x CPU, which provides 100 MHz of signal processing performance. The C28x central processing unit (CPU) is further boosted by the new Trigonometric Math Unit (TMU) extended instruction set, which enables fast execution of algorithms with trigonometric operations commonly found in transforms and torque-loop calculations. The Control Law Accelerator (CLA) allows offloading of common tasks from the C28x CPU. The CLA is an independent, 32-bit, floating-point math accelerator that executes in parallel with the CPU. Additionally, the CLA has its own dedicated memory resources and can directly access the key peripherals required in a typical control system. Support of a subset of ANSI C is standard, as are key features such as hardware breakpoints and hardware task-switching.

The F28004x supports up to 256KB of flash memory divided into two 128KB banks, which enable programming and execution in parallel. Up to 100KB of on-chip SRAM is also available in blocks of 4KB and 16KB for efficient system partitioning. Flash ECC, SRAM ECC/parity, and dual-zone security are also supported.

High-performance analog blocks are integrated on the F28004x MCU to further enable system consolidation. Three separate 12-bit ADCs provide precise and efficient management of multiple analog signals, which boosts system throughput. Seven programmable gain amplifiers on the analog front end (AFE) enable on-chip voltage scaling before conversion. Seven analog comparator modules provide continuous monitoring of input voltage levels for trip conditions.

C2000 Piccolo microcontrollers contain industry-leading control peripherals with frequency-independent ePWM/HRPWM, and eCAP allows for a best-in-class level of control to the system. The built-in, four-channel sigma-delta filter module (SDFM) allows for seamless integration of an oversampling sigma-delta modulator across an isolation barrier.

Connectivity is supported through various industry-standard communication ports (such as SPI, SCI, I2C, LIN, and CAN), and offers multiplexing options for optimal signal placement in a variety of applications. New to the C2000 Piccolo platform is the fully compliant PMBus.

### 2.2.2 LMG3410 Daughter Card

The LMG3410-HB-EVM configures two LMG3410 GaN FETs in a half bridge, with all the necessary auxiliary peripheral circuitry. The LMG3410 Single-Channel Gallium-Nitride (GaN) Power Stage contains a 70-μΩ, 600-V GaN power transistor and specialized driver in an 8 mm × 8 mm QFN package. TI’s Direct Drive architecture is used to create a normally-off device while providing the native switching performance of the GaN power transistor. When the LMG3410 is unpowered, an integrated low-voltage silicon MOSFET turns the GaN device off through its source. In normal operation, the low-voltage silicon MOSFET is held on continuously, while the GaN device is gated directly from an internally-generated negative voltage supply.

The integrated driver provides additional protection and convenience features. Fast overcurrent, overtemperature, and undervoltage lockout (UVLO) protections help create a fail-safe system; the device status is indicated by the FAULT output. An internal 5-V low-dropout regulator can provide up to 5 mA to supply external signal isolators. An externally-adjustable slew rate and a low-inductance QFN package minimize switching loss, drain ringing, and electrical noise generation.

### 2.2.3 UCC27712—620-V, 1.8-A, 2.8-A High-Side Low-Side Gate Driver

The UCC27712 is a 620-V high-side and low-side gate driver with 1.8-A source and a 2.8-A sink current, targeted to drive power MOSFETs or IGBTs.

The device consists of one ground-referenced channel (LO) and one floating channel (HO), which are designed for operating with bootstrap or isolated power supplies. The device features fast propagation delays and excellent delay matching between both channels. On the UCC27712, each channel is controlled by its respective input pins, HI and LI.

### 2.2.4 OPA237—Single-Supply Operational Amplifier

The OPA237 op amp family is one of TI’s MicroAmplifier™ series of miniature products. In addition to small size, these devices feature low offset voltage, low quiescent current, low bias current, and a wide supply range. They are ideal for single-supply applications. When operated from a single supply, the input common-mode range extends below ground and the output can swing to within 10 mV of ground.
2.2.5 ISO7740 and 20—High-Speed, Low-Power, Robust EMC Digital Isolators

The ISO77xx devices are high-performance, quad-channel digital isolators with 5000 V_{RMS} (DW package) and 2500 V_{RMS} (DBQ package) isolation ratings per UL 1577. This family of devices has reinforced insulation ratings according to the following certifications: VDE, CSA, TUV, and CQC.

The ISO774x devices provide high electromagnetic immunity and low emissions at low power consumption, while isolating CMOS or LVCMOS digital I/Os. Each isolation channel has a logic input and output buffer, separated by silicon dioxide (SiO$_2$) insulation barrier. Used in conjunction with isolated power supplies, this device helps prevent noise currents on a data bus, or other circuits from entering the local ground and interfering with or damaging sensitive circuitry.

2.3 System Design Theory

This reference design is a 1.6-kW boost power factor converter, operating in transition mode and implemented using the Piccolo F28004x microcontroller. The design is specifically tailored to suit the compact form factor requirements of the telecom, server, and industrial power supplies. The highest efficiency and power density that these applications require demands the use of bridgeless topologies. Even though the continuous-conduction-mode (CCM) totem-pole bridgeless PFC topology can obtain good efficiencies with the use of GaN power stages at switching frequencies around 150 kHz, operation beyond this frequency (to reduce the size of inductors used) requires zero voltage switching. It is possible to get zero voltage switching naturally in transition mode operation, for input voltages below half of the output voltage. For input voltages above half the output voltage, some extension of the synchronous FET conduction time is required to generate enough negative current in the inductor, so that zero voltage switching of the main FET can be achieved. This design incorporates the extension of synchronous FET conduction time to achieve ZVS over the entire input voltage range of 85 V to 265 V AC. This feature has helped to achieve above 99% peak efficiency for this design. The TIDA-00961 includes several protections embedded into the design, which include input overcurrent protection and output overvoltage protection. The design also provides precise information of the power consumption of the unit.

2.3.1 PFC Circuit Component Design

The F280049 MCU uses a triple control loop algorithm to support the operation of the PFC circuit in transition mode. The voltage loop sets the constant on-time (with some profiling to correct for error close to zero crossings); the current loop further adjusts the on-time to correct the current waveform, according to the input voltage waveform, and a third ZVS loop adjusts the off-time to get zero voltage switching. The difficult task of maintaining the interleaving between the two phases while the operating frequency is continually varying, and handled effectively by the controller. The following subsections highlight the design process and component selection for this design. The power components can be calculated assuming interleaved transition mode operation; the small change in off-time adjustment can be neglected.
2.3.1.1 Design Goal Parameters

Table 2 shows the design goal parameters. These parameters are used in further calculations when selecting components.

Table 2. Design Goal Parameters

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
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<tr>
<td>INPUT CONDITIONS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input voltage (V_{INAC})</td>
<td>—</td>
<td>85</td>
<td>230</td>
<td>265</td>
<td>V AC</td>
</tr>
<tr>
<td>Frequency (f_{LINE})</td>
<td>—</td>
<td>47</td>
<td>50/60</td>
<td>63</td>
<td>Hz</td>
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<td>—</td>
<td>1</td>
<td>W</td>
</tr>
<tr>
<td>OUTPUT CONDITIONS</td>
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<td></td>
<td></td>
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<td>—</td>
<td>390</td>
<td>V DC</td>
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<td>—</td>
<td>—</td>
<td>4.1</td>
<td>A</td>
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<td>Line regulation</td>
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<td>—</td>
<td>0.5%</td>
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<tr>
<td>Load regulation</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>0.5%</td>
<td></td>
</tr>
<tr>
<td>Output ripple</td>
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<td>25</td>
<td>—</td>
<td>V</td>
</tr>
<tr>
<td>Output power</td>
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<td>1600</td>
<td>—</td>
<td>W</td>
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<td></td>
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<tr>
<td>Efficiency (\eta)</td>
<td>V_{IN} = V_{NOM} and full load</td>
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<td>99%</td>
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<td>Operating ambient</td>
<td>Open frame, 200LFM</td>
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<td>55</td>
<td>°C</td>
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<td>Power line harmonics</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td></td>
</tr>
</tbody>
</table>

2.3.1.2 Current Calculations

The input fuse, bridge rectifier, and input capacitor are selected based upon the input current calculations. First, determine the maximum average output current, I_{OUT(MAX)}:

\[
I_{OUT(MAX)} = \frac{P_{OUT(MAX)}}{V_{OUT}}
\]  

(1)

With P_{OUT(MAX)} = 1600 W and V_{OUT} = 390 V, the value of I_{OUT(MAX)} is 4.1 A.

The maximum input RMS line current (I_{IN(RMS)(MAX)}) is calculated using the parameters from Table 2. Derating below 160 V to half the power at 85 V, the initial assumptions of efficiency and power factor are:

\[
I_{IN(RMS)(MAX)} = \frac{P_{OUT(MAX)}}{\eta \times V_{IN(MIN)} \times PF}
\]  

(2)

With a desired efficiency of 0.99, V_{IN(MIN)} = 160 V, a PF of 0.99, and P_{OUT(MAX)} = 1600 W, I_{IN(RMS)(MAX)} is 10.2 A.

The maximum input current (I_{IN(MAX)}) can be determined based upon the calculated RMS value and assuming the waveform is sinusoidal:

\[
I_{IN(MAX)} = \sqrt{2} \times I_{IN(RMS)(MAX)}
\]  

(3)

After inputting the earlier calculated value of I_{IN(RMS)(MAX)}, the I_{IN(MAX)} can be determined as 14.42 A.

2.3.1.3 Boost Inductor

The boost inductor is selected based on the inductor ripple current requirements at the peak of low line (in this case, at the low line voltage at full power). Selecting the inductor requires calculating the boost converter duty cycle at the peak of low line (D_{PEAK_LL}), as shown in Equation 4.

\[
D_{PEAK_LL} = \frac{V_{OUT} - \sqrt{2} \times V_{IN(MIN)}}{V_{OUT}}
\]  

(4)
With $V_{OUT} = 390$ V, $V_{IN(MIN)} = 160$ V, $D_{PEAK(LL)}$ can be calculated as 0.42.

The minimum switching frequency of the converter ($F_{MIN}$) under low line conditions occurs at the peak of low line. For this design example, $F_{MIN}$ is set to 450 kHz, so that at high line the frequency will be around 1 MHz, which is a good balance between a small sized inductor and a lower switching loss. For a two-phase interleaved design, the boost inductors are determined as calculated in Equation 5.

$$L_1 = L_2 = \frac{\eta \times V_{IN(MIN)}^2 \times D_{PEAK(LL)}}{P_{OUT} \times F_{MIN}}$$

(5)

As stated earlier, the desired efficiency is 0.99, $V_{IN(MIN)} = 160$ V, $D_{PEAK(LL)} = 0.42$, $P_{OUT} = 1600$ W and $F_{MIN} = 450$ kHz, the calculated value of $L_1$ and $L_2$ are 14.78 µH.

The value of the boost inductor was rounded off to 15 µH.

The inductor peak and RMS currents are given by:

$$I_{L\_PEAK} = \frac{\sqrt{2} \times P_{OUT}}{V_{IN(MIN)} \times \eta}$$

(6)

After inputting the earlier stated values, $I_{L\_PEAK}$ is calculated to be 14.28 A.

$$I_{L\_RMS} = \frac{I_{L\_PEAK}}{\sqrt{6}} = \frac{14.28 \text{ A}}{\sqrt{6}} = 5.83 \text{ A}$$

(7)

### 2.3.1.4 Switching Elements

Each of the GaN FETs act as the main switching device during one half cycle, and as the boost diode during the other half cycle. Thus, the inductor current can be assumed to split equally between the two FETs connected to it.

Thus, the RMS current ($I_{D\_RMS}$) through each GaN FET is calculated as in Equation 8.

$$I_{D\_RMS} = \frac{I_{L\_PEAK}}{2 \times \sqrt{6}} = \frac{14.28 \text{ A}}{2 \times \sqrt{6}} = 2.92 \text{ A}$$

(8)

The integrated GaN FET LMG3410 is selected for the current design, as it offers low losses and ease of layout. The standard daughter card LMG3410-HB-EVM was selected for each half bridge to simplify layout.

### 2.3.1.5 Output Capacitor

The output capacitor, $C_{OUT}$, is sized to meet holdup requirements of the converter and the output ripple. In this design, the sizes of the output capacitors are based on a voltage ripple of less than 3% of the output DC voltage.

$$C_{OUT(MIN)} \geq \frac{I_{OUT}}{\pi \times 4 \times f_{LINE\_MIN} \times V_{RIPPLE}}$$

(9)

Where $V_{RIPPLE} = 0.03 \times 390$ V (assuming 3% voltage ripple), $I_{OUT} = 4.1$ A, $f_{line\_min} = 47$ Hz, minimum value of $C_{OUT}$ is 593 µF.

The actual capacitor used is 660 µF.

The required ripple current rating at twice the line frequency is equal to:

$$I_{COUT\_2\_LINE} = \frac{I_{OUT(MAX)}}{\sqrt{2} \times \eta}$$

(10)

Again with $I_{OUT(MAX)} = 4.1$ A, efficiency of 0.99, $I_{COUT\_2\_LINE} = 2.93$ A.
There is a high-frequency ripple current through the output capacitor:

\[ I_{\text{COUT\_HF}} = \sqrt{\frac{P_{\text{OUT}} \times 2\sqrt{2}}{2 \times \eta \times V_{\text{IN\_MIN}}} \left(\frac{4\sqrt{2} \times V_{\text{IN\_MIN}}}{9\pi \times V_{\text{OUT}}} \right)^2 - \left(I_{\text{COUT\_2\_LINE}}\right)^2} \]  

(11)

With earlier mentioned and calculated values, the \( I_{\text{COUT\_HF}} \) is 2.86 A.

The total ripple current in the output capacitor is the combination of both, and the output capacitor must be selected accordingly:

\[ I_{\text{COUT\_RMS}} = \sqrt{\left(I_{\text{COUT\_2\_LINE}}\right)^2 + \left(I_{\text{COUT\_HF}}\right)^2} \]  

(12)

With \( I_{\text{COUT\_2\_LINE}} = 2.93 \) A and \( I_{\text{COUT\_HF}} = 2.86 \) A, \( I_{\text{COUT\_RMS}} \) is calculated to be 4.09 A.

### 2.3.1.6 Current and Voltage Sense

The input voltage is sensed through two resistive dividers, individually sensing both the input terminals with respect to output return (which is the ground reference for all the control circuits). These are then buffered through one LMV612 before routing to the C2000 Piccolo controlCARD, which senses it differentially. Two comparators sense the polarity of AC cycle and AC drop, which are used by the controlCARD. Output voltage sensing is done directly through a single-ended resistive divider.

A Hall-effect sensor is used for input current sensing. Individual channel currents are not sensed. Only the overall current waveform is sensed for controlling the current loop to obtain a low THD. As the maximum input current is around 15 A, a 25-A rated sensor (ACS716KLATR-12CB-NL-T) is used. Because the sensitivity is only 18.5 mV/A, a programmable gain stage using OPA237 and SN74LVC1G3157 are used to scale the output to scale up to a level suitable for the controlCARD.

### 2.3.1.7 Low Frequency FET Rectifier

To maximize the efficiency, reduce the loss in the low frequency rectifier section of the circuit to a minimum. Thus, two low on-resistance Silicon MOSFETs (STY105NM50N) are used instead of diodes. The total power loss in these FETs is calculated using the input RMS current and the \( R_{DS(on)} \) of the MOSFET:

\[ P_{\text{RECT}} = I_{\text{IN\_RMS\(\text{MAX}\)}}^2 \times R_{DS(on)} \]  

(13)

With earlier calculated value of \( I_{\text{IN\_RMS\(\text{MAX}\)}} = 10.2 \) A, \( R_{DS(on)} \) at 100°C is 1.7 × 0.019 Ω, the power loss in rectifier, \( P_{\text{RECT}} \) can be calculated as 3.36 W.

These FETs are driven using a half-bridge gate driver UCC27712. Carefully select the bootstrap capacitor. As the switching is very slow, it must hold its charge for a long time (~11 ms) before it is replenished. Thus, its value depends more on the leakage during the on-time than on the actual gate charge switched. The required capacitance can be found out from the high-side driver quiescent current \( (I_{\text{QBS}}) \), the bootstrap supply leakage current \( (I_{\text{BL}}) \), the line switching period \( (T_{\text{Line}}) \), the total gate charge of the FET \( (Q_G) \), and the allowable voltage drop \( (\triangle V_{\text{BOOT}}) \):

\[ C_{\text{BOOT}} = \frac{Q_G + T_{\text{LINE}} \times (I_{\text{QBS}} + I_{\text{BL}})}{\triangle V_{\text{BOOT}}} \]  

(14)

\( Q_G \) of the FET chosen is 326 nC, \( T_{\text{Line}} = 11 \) ms, \( I_{\text{QBS}} = 100 \) μA, \( I_{\text{BL}} = 20 \) μA and \( \triangle V_{\text{BOOT}} = 0.5 \) V, the calculated value of \( C_{\text{BOOT}} \) is 3.29 μF.

A 10-μF capacitor was selected to account for variations due to DC bias and temperature.
2.3.2 Bias Power

An auxiliary housekeeping power supply is needed to power the F280049 controlCARD, GaN daughter card, UCC27712 Gate Driver, and Inrush current-limiting bypass relay. In addition, external cooling is required when the converter is operated at power ≥500 W. To address each of these needs, an add-on auxiliary power supply based on UCC28740 rated for 10 W is used. This power supply is based on a Flyback design using the constant-voltage, constant-current Flyback Controller UCC28740. The power for the TIDA-00961 is taken out of the non-isolated 12-V output of this power supply. The 5-V output needed for the GaN and C2000 Piccolo controlCARDs is generated using a DC/DC converter based on the TPS62153. The 3.3-V output for signal processing is derived using a linear regulator LP2986.

Table 3. Maximum Current Rating of Different Blocks on Design

<table>
<thead>
<tr>
<th>DEVICE</th>
<th>VOLTAGE</th>
<th>MAX CURRENT</th>
</tr>
</thead>
<tbody>
<tr>
<td>TMS320F280049 control card</td>
<td>5 V</td>
<td>150.00 mA</td>
</tr>
<tr>
<td>GaN daughter cards</td>
<td>5 V</td>
<td>50.00 mA</td>
</tr>
<tr>
<td>Signal processing</td>
<td>3.3 V</td>
<td>20.00 mA</td>
</tr>
<tr>
<td>Relay + gate driver</td>
<td>12 V</td>
<td>40.00 mA</td>
</tr>
<tr>
<td>Fan</td>
<td>12 V</td>
<td>200.00 mA</td>
</tr>
</tbody>
</table>

2.3.3 Firmware on the C2000™ Piccolo™ controlCard

The controlCARD included with the TMDXDOCK280049 F280049 Experimenter's Kit can be used with the TIDA-00961. It is a board-level module that utilizes the HSEC controlCARD form factor, a common interface used in C2000 Piccolo evaluation modules, and can be used in conjunction with other C2000 Piccolo application kits. For more details on this controlCARD, see Piccolo F280049C controlCARD Information Guide.

The firmware for the design can be downloaded from http://www.ti.com/tool/c2000ware-digitalpower-sdk which requires the user to login to ti.com through myTI account. After downloading and installing the SDK, a step-by-step guide can be found within the directory where SDK is installed at - C2000Ware_DigitalPower_SDK_1_00_01_00/solutions/tida_00961/docs. This document covers the hardware interface, voltage loop and current loop implementation, system protection, firmware structure, internal state machines, and other advanced features. A graphical user interface (GUI) and a guide for tuning the coefficients of a PFC system are also presented in the guide.
3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware and Software

3.1.1 Hardware

This section details the necessary equipment, test setup, and procedure instructions for the TIDA-00961 board testing and validation.

3.1.1.1 Test Conditions

For input, the power supply source ($V_{IN}$) must range from 85 V to 265-V AC.

Set the input current limit of the input AC source to 15 A.

For output, use an electronic variable load or a variable resistive load, which must be rated for $\geq$ 400 V and must vary the load current from 0 A to 5 A.

3.1.1.2 Test Equipment Required for Board Validation

• Isolated AC source
• Single-phase power analyzer
• Digital oscilloscope
• Multimeters
• Electronic or resistive load

3.1.1.3 Test Procedure

1. Connect the two GaN daughter cards and C2000 Piccolo controlCard to the TIDA-00961 board as follows:
   a. One daughter card at connectors J201, J202, J203, and J204
   b. One daughter card at connectors J206, J207, J208, and J209
   c. C2000 Piccolo controlCard at connector J205; the details of the connections to each pin of the connectors can be found in the schematic of the TIDA-00961 design

2. Connect input terminals (Pin-1 and Pin-3 of connector J101) of the reference board to the AC power source.

3. Connect output terminals (Pin-1 and Pin-2 of connector J2) to the electronic load, maintaining correct polarity. Pin-2 is the VDC output and Pin-1 is the GND terminal.

4. Set and maintain a minimum load of approximately 50 mA.

5. Increase gradually the input voltage from 0 V to turnon voltage of 85-V AC.

6. Start the load to draw current from the output terminals of the PFC.

7. Observe startup conditions for smooth switching waveforms.
3.2 Testing and Results

The test results are divided in multiple sections that cover the steady state performance, functional performance waveforms and test data, transient performance waveforms, and thermal measurements.

3.2.1 Performance Data

3.2.1.1 Efficiency and Regulation With Load Variation

Table 4 shows the data at a 120-V AC input.

<table>
<thead>
<tr>
<th>$P_{\text{OUT}}$ (W)</th>
<th>$P_{\text{IN}}$ (W)</th>
<th>EFFICIENCY</th>
<th>POWER FACTOR (PF)</th>
<th>$I_{\text{THD}}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>223.36</td>
<td>227.81</td>
<td>98.05%</td>
<td>0.99329</td>
<td>6.16%</td>
</tr>
<tr>
<td>296.84</td>
<td>302.46</td>
<td>98.14%</td>
<td>0.99699</td>
<td>5.18%</td>
</tr>
<tr>
<td>372.38</td>
<td>379.94</td>
<td>98.15%</td>
<td>0.99835</td>
<td>4.69%</td>
</tr>
<tr>
<td>444.63</td>
<td>453.23</td>
<td>98.10%</td>
<td>0.99835</td>
<td>3.36%</td>
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<tr>
<td>504.5</td>
<td>515.5</td>
<td>98.01%</td>
<td>0.999</td>
<td>3.87%</td>
</tr>
<tr>
<td>592.01</td>
<td>604.88</td>
<td>97.87%</td>
<td>0.9992</td>
<td>3.63%</td>
</tr>
<tr>
<td>661.35</td>
<td>676.8</td>
<td>97.72%</td>
<td>0.9992</td>
<td>3.41%</td>
</tr>
<tr>
<td>733.57</td>
<td>751.75</td>
<td>97.58%</td>
<td>0.99934</td>
<td>3.17%</td>
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<tr>
<td>811.84</td>
<td>833.67</td>
<td>97.38%</td>
<td>0.99939</td>
<td>2.98%</td>
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<tr>
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<td>96.90%</td>
<td>0.99939</td>
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<td>0.99933</td>
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<tr>
<td>1098.27</td>
<td>1122.19</td>
<td>97.87%</td>
<td>0.99865</td>
<td>3.81%</td>
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<tr>
<td>1171.38</td>
<td>1197.79</td>
<td>97.80%</td>
<td>0.99872</td>
<td>3.71%</td>
</tr>
</tbody>
</table>

Table 5 shows the data at a 230-V AC input.

<table>
<thead>
<tr>
<th>$P_{\text{OUT}}$ (W)</th>
<th>$P_{\text{IN}}$ (W)</th>
<th>EFFICIENCY</th>
<th>POWER FACTOR (PF)</th>
<th>$I_{\text{THD}}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>290.88</td>
<td>296.79</td>
<td>98.00%</td>
<td>0.9787</td>
<td>8.32%</td>
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<tr>
<td>365.69</td>
<td>371.25</td>
<td>98.50%</td>
<td>0.9862</td>
<td>6.51%</td>
</tr>
<tr>
<td>438.67</td>
<td>444.44</td>
<td>98.70%</td>
<td>0.99</td>
<td>5.62%</td>
</tr>
<tr>
<td>512.78</td>
<td>519.11</td>
<td>98.78%</td>
<td>0.99256</td>
<td>5.62%</td>
</tr>
<tr>
<td>584.92</td>
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<td>4.58%</td>
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<tr>
<td>660.4</td>
<td>667.97</td>
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<tr>
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<td>10.12%</td>
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<td>0.99314</td>
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</tr>
<tr>
<td>952.8</td>
<td>965.68</td>
<td>98.66%</td>
<td>0.995</td>
<td>8.84%</td>
</tr>
<tr>
<td>1026.81</td>
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<td>1173.48</td>
<td>1187.97</td>
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<td>0.99646</td>
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<tr>
<td>1319.22</td>
<td>1335.51</td>
<td>98.78%</td>
<td>0.99707</td>
<td>7.05%</td>
</tr>
</tbody>
</table>
3.2.2 Performance Curves

3.2.2.1 Efficiency and Power Factor With Load and Line Variation

Figure 3 and Figure 4 show the measured efficiency and power factor, respectively, in the system with AC input voltage variation.

3.2.2.2 Input THD With Load and Line Regulation

Figure 5 shows the measured input THD of the system with AC input voltage variation and Figure 6 shows the measured load regulation of the output with AC input voltage variation.
# 3.2.3 Functional Waveforms

## 3.2.3.1 Switching Node Waveforms

The waveforms at both switching nodes were observed, along with the input voltage and current at 230-V AC under a 1600-W load (4.1 A), and at 120-V AC under a 1200-W load.

**NOTE:** Blue trace: Input voltage, 500 V/div; Green trace: Input current, 10 A/div; Red trace: Phase1 voltage, 200 V/div; Pink trace: Phase2 voltage, 200 V/div

**Figure 7. SW Node Waveform at $V_{INAC} = 230$-V AC, Positive Half, 1600-W Load**

**NOTE:** Blue trace: Input voltage, 500 V/div; Green trace: Input current, 10 A/div; Red trace: Phase1 voltage, 200 V/div; Pink trace: Phase2 voltage, 200 V/div

**Figure 8. SW Node Waveform at $V_{INAC} = 230$-V AC, Negative Half, 1600-W Load**

**NOTE:** Blue trace: Input voltage, 250 V/div; Green trace: Input current, 10 A/div; Red trace: Phase1 voltage, 200 V/div; Pink trace: Phase2 voltage, 200 V/div
Figure 9. SW Node Waveform at $V_{INAC} = 120$-V AC, Positive Half, 1200-W Load

Figure 10. SW Node Waveform at $V_{INAC} = 120$-V AC, Negative Half, 1200-W Load
3.2.3.2 **Input Voltage and Current Waveform**

Figure 11 to Figure 14 show the input current waveforms at various line and load conditions.

**NOTE:** Blue trace: Input voltage, 250 V/div; Green trace: Input current, 10 A/div; Red trace: Phase1 voltage, 200 V/div; Pink trace: Phase2 voltage, 200 V/div

**Figure 11. Input Voltage and Input Current at V_{INAC} = 230-V AC, 1650-W Load**

**NOTE:** Blue trace: Input voltage, 250 V/div; Green trace: Input current, 2 A/div; Red trace: Phase1 voltage, 200 V/div; Pink trace: Phase2 voltage, 200 V/div

**Figure 12. Input Voltage and Input Current at V_{INAC} = 230-V AC, 600-W Load**

**NOTE:** Blue trace: Input voltage, 250 V/div; Green trace: Input current, 5 A/div; Red trace: Phase1 voltage, 200 V/div; Pink trace: Phase2 voltage, 200 V/div

**Figure 13.**
Figure 14. Input Voltage and Input Current at $V_{INAC} = 120$-V AC, 1350-W Load

**NOTE:** Blue trace: Input voltage, 250 V/div; Green trace: Input current, 5 A/div; Red trace: Phase1 voltage, 200 V/div; Pink trace: Phase2 voltage, 200 V/div

Figure 15. Input Voltage and Input Current at $V_{INAC} = 120$-V AC, 400-W Load
3.2.3.3 Output Ripple

The ripple was observed at a 390-V DC output loaded to 4.1 A at 230-V AC.

Figure 16. Output Voltage Ripple at $V_{INAC} = 230$ V, Full Load

3.2.3.4 Turnon Characteristics

The 390-V output turnon at full load (4.1 A) was recorded at 230-V AC.

NOTE: Blue trace: Input voltage, 500 V/div; Green trace: Input current, 10 A/div; Red trace: Output voltage, 200 V/div

Figure 17. Output Turnon Waveform at $V_{INAC} = 230$ V With Light Load of 0.8 A
3.2.4 Thermal Image

Figure 19 and Figure 20 show the thermal images at a 900-W load without airflow.
4 Design Files

4.1 Schematics
To download the schematics, see the design files at TIDA-00961.

4.2 Bill of Materials
To download the bill of materials (BOM), see the design files at TIDA-00961.

4.3 PCB Layout Recommendations
A careful PCB layout is critical in a high-current fast-switching circuit to provide appropriate device operation and design robustness. As with all switching power supplies, pay attention to detail in the layout to save time in troubleshooting.

4.3.1 Power Stage Specific Guidelines
Follow these key guidelines to route the power stage components:
- Minimize the loop area and trace length of the power path circuits, which contain high frequency switching currents. This will help reduce EMI and improve the converter's overall performance.
- Keep the switch node as short as possible. A short and optimal trace width helps reduce induced ringing caused by parasitic inductance.
- Keep traces with high dV/dt potential and high di/dt capability away from or shielded from sensitive signal traces with adequate clearance and ground shielding.
- Keep power ground and control ground separate for each power supply stage. Tie them together (if they are electrically connected) in one point near the DC input return or output return of the given stage.
- When multiple capacitors are used in parallel for current sharing, the layout should be symmetrical across both capacitor leads. If the layout is not identical, the capacitor with the lower series trace impedance will see higher peak currents, and become hotter (i2R).
- Tie the heat sinks of all the power switching components to their respective power grounds.
- Place protection devices such as TVS, snubbers, capacitors, or diodes physically close to the device they are intended to protect, and route with short traces to reduce inductance.
- Choose the width of PCB traces based on an acceptable temperature rise at the rated current as per IPC2152, as well as acceptable DC and AC impedances. The traces should withstand the fault currents (such as short circuit current) before electronic protection devices, such as fuses or circuit breakers, are activated.
- Determine the distances between various traces of the circuit, according to the requirements of applicable standards. For this design, the UL 60950-1 safety standard is followed to maintain the creepage and clearance from live line to neutral line and to safety ground, as defined in the Tables 2K through 2N of this standard.
- Adapt the thermal management to fit the end-equipment requirements.

4.3.2 Gate Driver Specific Guidelines
Follow these key guidelines to route the high-frequency high-current gate driver:
- Place the driver device as close as possible to the power device to minimize the length of high current traces between the output pins of gate drive and the gate of the power device.
- Locate the VDD bypass capacitors between VDD and GND as close as possible to the driver with minimal trace length to improve the noise filtering. These capacitors support high-peak current being drawn from VDD.
- Minimize the turn-on and turn-off current-loop paths (driver device, power MOSFET, and VDD bypass capacitor) as much as possible to keep the stray inductance to a minimum.
- Minimize noise coupling with star point grounding from one current loop to another. Connect the driver GND to the other circuit nodes, such as the power switch source or the PWM controller ground, at one
single point. The connected paths must be as short as possible to reduce inductance, and be as wide as possible to reduce resistance.

4.3.3 Layout Prints
To download the layer plots, see the design files at TIDA-00961.

4.4 Altium Project
To download the Altium project files, see the design files at TIDA-00961.

4.5 Gerber Files
To download the Gerber files, see the design files at TIDA-00961.

4.6 Assembly Drawings
To download the assembly drawings, see the design files at TIDA-00961.

5 Software Files
To download the software files, see the design files at TIDA-00961.

6 Related Documentation
1. Texas Instruments, *LMG3410 600-V 12-A Integrated GaN Power Stage*
2. Texas Instruments, *TMS320F28004x Piccolo™ Microcontrollers*
3. Texas Instruments, *UCC27712 620-V, 1.8-A, 2.8-A High-Side Low-Side Gate Driver with Interlock*
4. Texas Instruments, *An Interleaved PFC Preregulator for High-Power Converters*
6. Texas Instruments, *PFC THD Reduction and Efficiency Improvement by ZVS or Valley Switching*

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IGOR AN is a Central FAE in Shanghai, working for C2000 based digital power and motor control solutions. Focusing on digital power and motor control algorithm development. He graduated Nanjing university of aeronautics and astronautics for automatic control theory master, and got the Engineer diploma from Supélec France for automatic in 2006.
Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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<th>Page</th>
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