White Paper

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TI's Compact Power Solution for Virtex™-6 FPGAs

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This application report describes how a new, integrated FET dc-to-dc converter can meet the power requirements of a new, high-performance FPGA from Xilinx in a very compact and board-space-saving design.

1 Introduction

Today's high-performance processors require choosing power solutions much earlier in the design cycle. This is because power is now a system issue as opposed to when providing a 5-V rail was the only concern. Today's 40-nanometer technology requires lower voltages that increase the critical nature of the tolerance window. Requirements for both *static and dynamic* power are becoming more challenging with many application reports devoted to meeting the required transient response for high-

end processors. Further complicating the design effort is the number of low-voltage rails that a typical design with DDR memory and termination requires.

This can be seen in some of the power specifications for Xilinx's new Virtex™-6 family of FPGAs. The recommended operating conditions are as follows: V_{ccint}, 0.95 V to 1.05 V; V_{ccaux}, 2.375 V to 2.625 V; and V_{cco} from 1.14 V to 2.7 V. Because accurate current calculations often are not known until the design is finished, good estimations are very important. The currents can be calculated using the XPower Estimator (XPE) available at http://www.xilinx.com/power. This spreadsheet allows the designer to estimate the current after entering all the necessary operating characteristics of the FPGA design.

This makes the new TPS54620 an excellent choice for powering the new Virtex-6 line. TI also has solutions from 1.5 A up to 10 A in this integrated FET SWIFT™ product line.

The 4.5-V to 17-V input supply of the TPS54620 allows the designer the freedom to use a 5-V bus, or as is more common in higher power applications, a 12-V bus.

Looking at power from the total-system standpoint, the adjustable switching frequency provides flexibility to move out of areas of interference in sensitive circuits. Also, external frequencies can be synchronized to eliminate beat frequencies or to run 180° out-of-phase to cancel reflective noise on the bus.

2 Synchronizing Benefits

Providing 6 A in a synchronous buck converter, the TPS54620 is a high-efficiency, full-featured solution. The very low E_{DSon} of 26 mW for the high-side FET and the 19-mW E_{DSon} for the low-side FET provide a peak of 95 percent efficiency for a best-of-class rating.

Looking at the Virtex-6 family it can be seen that the quiescent V_{ccint} supply current varies from 927 mA for the XC6VLX75T to 5227 mA for the XC6VSX475T.

Figure 2 shows these effects of beat frequencies:

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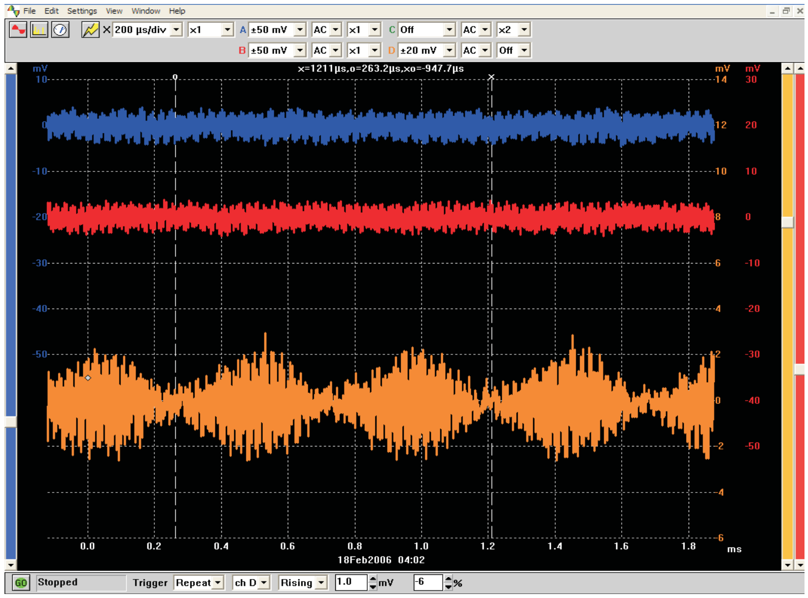

Figure 1. Two Rails Synchronized at 180° Out-of-Phase

The blue line and the red line are two switching converters in a system that is not frequency synchronized. The bottom yellow line is the reflected ripple showing the low-frequency component generated from the beat frequency function.

Figure 2 shows the effect of synchronizing the switching frequency at 180° out-of-phase operation. This results in the absence of the beat frequency that is seen in Figure 1. This solution also can eliminate an input inductor for the low-frequency noise that can be generated from this interaction.

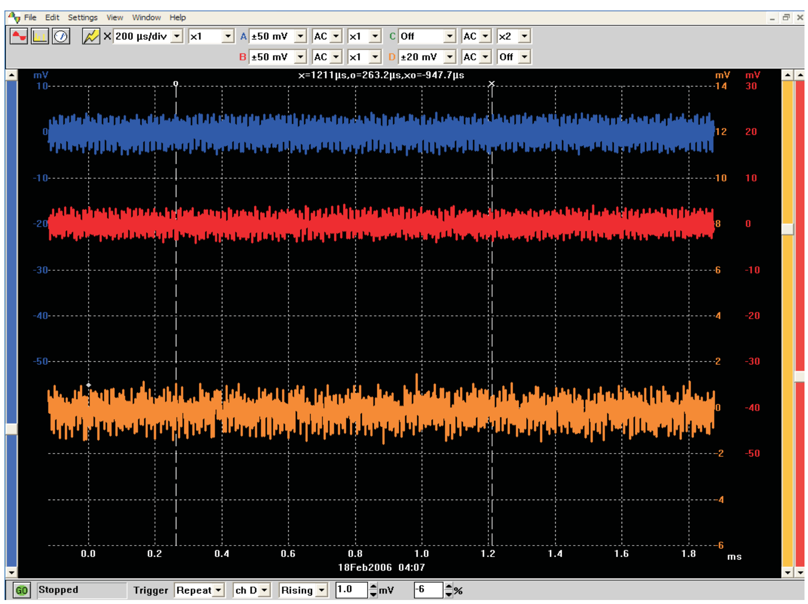

Figure 2. Two Rails Nonsynchronized

3 Advantages of Tracking Voltage Rails

Another important feature of this new buck converter is the built-in tracking function. The TPS54620 allows several types of sequencing schemes: sequential, ratiometric, and simultaneous. Virtex-6 devices require a sequential power up of V_{ccint}, then V_{ccaux}, and then V_{cco} (pages 3 and 4 of Xilinx datasheet DS152). The track pin of the TPS54620 is dual functioned in that it also allows adjustable soft start which can help meet the 20-ms to 50-ms required ramp time for the Virtex-6 family. This allows multiple TPS54620s to track each other in the prescribed ramp rates meeting the Virtex-6 specifications without adding additional external devices.

Advantages from sequencing the rails also include the reduced inrush current needed when staggering power-up times. Reduced total inrush current means a smaller capacitor bank may be required and the size of some components may be reduces. The high switching frequency of the converter allows smaller output inductor and capacitors, allowing further reduction of board components.

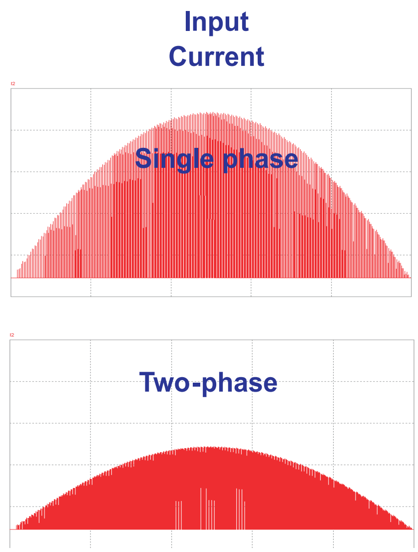

Figure 3. Inrush Current for Single-Phase and Two-Phase Operations

Figure 3 shows the reduced inrush current from operating in a 180° out-of-phase operation, allowing board space savings and component count. The reduced stresses on the input rail make this technique a good solution to consider. Balancing the currents on both phases provides the most effective results.

Best of all the features for the nonpower supply expert is the availability of design software to create your new design with SwitcherPro™ software. This Web-based or downloadable tool is available at http://www.ti.com/swift. Figure 4 shows a typical circuit with the few external parts required for a complete TPS54620 solution.

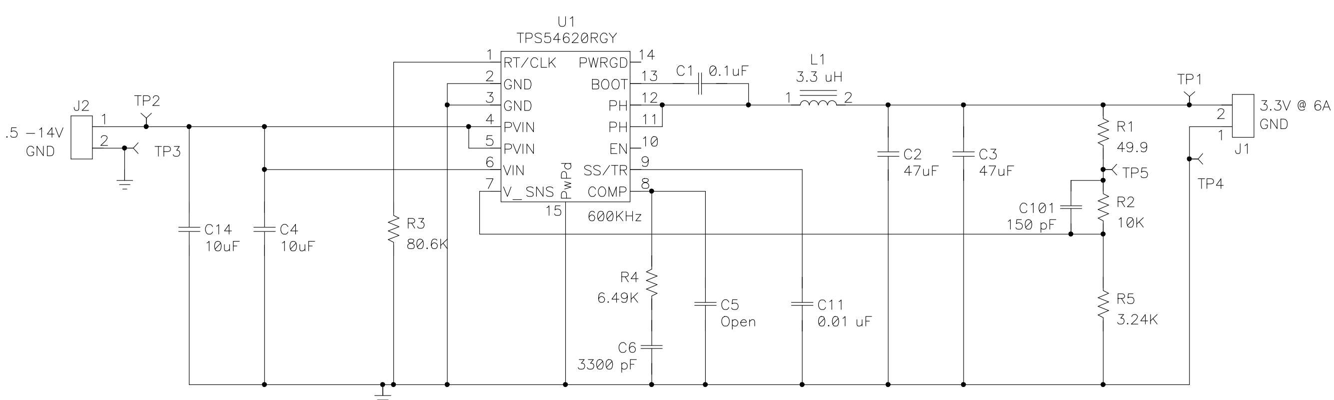

Figure 4. TPS54620 Solution Schematic

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