

**ADC12DL040,ADC12DL065,ADC12DL080,
ADC14L020,ADC14L040,CLC5903,LMH6550,
LMH6551**

Intermediate Frequency (IF) Sampling Receiver Concepts



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Intermediate Frequency (IF) Sampling Receiver Concepts

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This article will discuss Intermediate Frequency (IF) sampling concepts of sub-sampling (or under sampling), noise processing gain, and the effects of interfering signals. Examples will be based on the GSM/EDGE communications standard where the channel bandwidth is 200 kHz and the sample rate is typically a multiple of 13 MHz.

Sub-Sampling

Nyquist's sampling theorem states that if a signal is sampled at least twice as fast as the highest sampled frequency component, no information will be lost when the signal is reconstructed. The sample rate divided by two ($F_s/2$) is known as the Nyquist frequency and the frequency range from DC (or 0 Hz) to $F_s/2$ is called the first Nyquist zone.

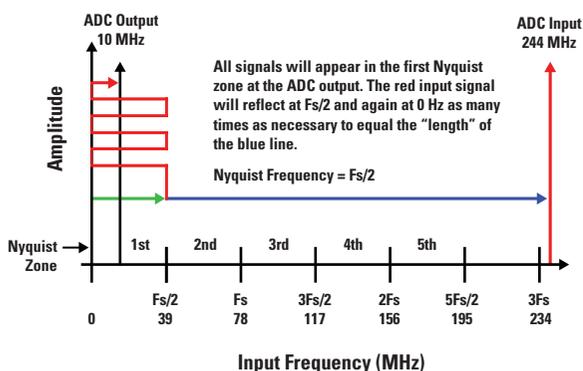


Figure 1. Nyquist Sampling Example

We'll use National's high-speed ADC12DL080 as an example. Clocking the ADC12DL080 at $6 * 13$ MHz or 78 Mega-Samples Per Second (MSPS) places the Nyquist frequency at 39 MHz. All the signal information that falls in the first Nyquist zone is over sampled and can be recovered. If the sampled signal moves into the second Nyquist

zone from 39 MHz to 78 MHz, it can still be recovered but the absolute frequency information is lost. When the input signal moves above $F_s/2$, it has been sub-sampled and 'reflects' or 'folds' at $F_s/2$ and moves back toward 0 Hz at the ADC output. If $F_s/2 = 39$ MSPS, an input signal at 40 MHz will fold back to 38 MHz. Folding will occur in each Nyquist zone. For example, a 244 MHz IF at 78 MSPS will result in a 10 MHz signal at the ADC output. The folded (or aliased) frequency is calculated by finding the closest multiple of F_s to the desired input frequency (F_{IN} , 244 MHz), then subtracting the two frequencies:

$$F_{IN} = (n * F_s) \text{ or } 244 \text{ MHz} - (3 * 78 \text{ MHz}) \\ = 244 \text{ MHz} - 234 \text{ MHz} = 10 \text{ MHz}$$

Signals at 10 MHz, 68 MHz, 88 MHz, 146 MHz, and beyond will all appear at 10 MHz. There is no way to determine the original IF since the Nyquist criteria has been violated.

Sub-sampling systems take advantage of this folding or mixing function to reduce the IF frequency prior to a final digital tuner like National's CLC5903. If the desired signal Bandwidth (BW) is less than $F_s/2$, all of the signal information can still be recovered. A channel filter should be placed in front of the ADC to remove any undesired signals from other Nyquist zones. This filter will also limit the amount of noise at the ADC input to only one Nyquist zone.

Noise Processing Gain

As the ADC input frequency increases, the Signal-to-Noise Ratio (SNR) for large signals will decrease due to clock jitter. Small signal SNR is not affected. For the ADC12DL080, the large signal SNR will be 65 dBFS (dB relative to Full Scale) at a 244 MHz IF. When the

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Featured Products

ADC12DL080 Dual, 12-bit, 80 MSPS Analog-to-Digital Converter for High-IF Sampling

The ADC12DL080 is a dual, low-power monolithic CMOS analog-to-digital converter. This device is capable of converting an analog input signal into 12-bit digital words at rates up to 80 Mega-Samples Per Second (MSPS). The ADC12DL080 is designed with 600 MHz full-power input bandwidth and low aperture jitter to allow sampling of high-frequency IF inputs. Operating on a single 3.3V supply, the ADC12DL080 achieves 11.0 effective bits at Nyquist and consumes just 450 mW at 80 MSPS. A power-down feature reduces power consumption to 100 mW.

The ADC12DL080 may be used either with an external reference voltage (1.0V nominal, 0.8V to 1.5V allowed) or with an internal precision 1.0V refer-



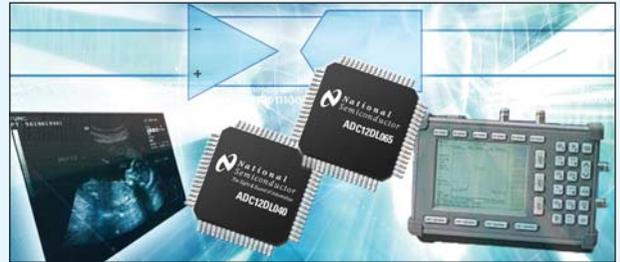
ence. The differential inputs provide a full-scale differential input swing equal to two times the reference voltage with the possibility of a single-ended input. Duty cycle stabilization is applied to the input clock to provide an internal duty cycle of 50%. The output data can be set for offset binary or two's complement.

Features

- Single 3.3V supply operation
- Outputs 2.4V to 3.6V compatible
- Low power consumption
- Power-down mode
- Duty cycle stabilizer
- External or internal selectable reference
- Pin-compatible with ADC12DL040, ADC12DL065, and ADC12DL066

For input frequencies as high as 200 MHz, the ADC12DL080 provides an impressive 67 dB SNR and 81 dB SFDR, making it ideal for high-IF sampling receivers, test and measurement equipment, radar, and medical imaging applications. The ADC12DL080 is offered in a TQFP-64 package and operates over the industrial temperature range of -40°C to +85°C.

For FREE samples, datasheets, and more, visit www.national.com/pf/DC/ADC12DL080.html



ADC12DL040/65 Dual, 12-Bit A/D Converters for Excellent Signal Conditioning and Acquisition

The ADC12DL040 and ADC12DL065 are dual, low-power 12-bit Analog-to-Digital Converters (ADC) capable of converting analog input signals at 40 and 65 Mega-Samples Per Second (MSPS), respectively. These ADCs provide excellent dynamic performance and 250 MHz full-power bandwidth. The ADC12DL040 achieves 11.1 effective bits and consumes just 210 mW at 40 MSPS and the ADC12DL065 achieves 11.0 effective bits and consumes 360 mW at 65 MSPS.

The differential inputs provide a full-scale differential input swing equal to two times the reference voltage with the possibility of a single-ended input. The digital outputs from the two ADCs are available on a single multiplexed 12-bit bus or on two separate buses. Duty cycle stabilization is applied to the input clock to provide an internal duty cycle of 50%. The output data can be set for offset binary or two's complement.

Features

- Single 3.0V (ADC12DL040) and 3.3V (ADC12DL065) supply operation
- Internal reference
- Outputs 2.4V to 3.6V compatible
- Low power consumption
- Power-down mode
- Duty cycle stabilizer
- Multiplexed output mode

The ADC12DL040/65 provide an impressive 68.5 dB SNR and 85 dB SFDR at Nyquist while consuming just 210 mW and 360 mW, respectively. These converters are ideal for portable instrumentation, medical imaging, communications receivers, and wireless infrastructure equipment. These ADCs are available in TQFP-64 packaging and operate over the industrial temperature range of -40°C to +85°C.

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www.national.com/pf/DC/ADC12DL065.html

IF Sampling Receiver Concepts

input is reduced to -10 dBFS or less, the SNR will increase to 70 dBFS. If the desired channel bandwidth is over sampled, a digital channel filter can further improve the SNR. When an ADC's SNR is measured, it is normally specified as the SNR in the first Nyquist zone. In other words, all the noise from DC to $F_s/2$ is summed to get the SNR relative to the ADC's full-scale input. A digital channel filter can remove the ADC output noise except in the channel bandwidth. The output noise is integrated over a smaller frequency range. This improvement is called noise processing gain and can be calculated with the following equation:

$$\text{Processing Gain} = -10 * \text{LOG} (\text{Channel BW/Nyquist BW})$$

For a 200 kHz narrow-band system:

$$\text{Processing Gain} = -10 * \text{LOG} (200 \text{ kHz}/39 \text{ MHz}) = 22.9 \text{ dB}$$

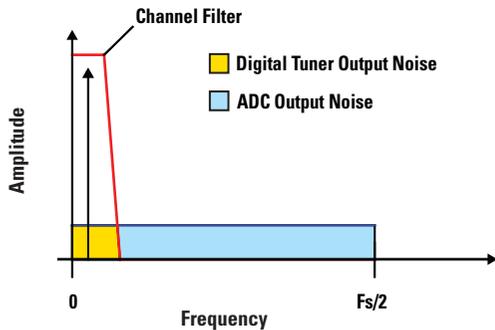


Figure 2. Noise Processing Gain

Processing gain can also be calculated by finding the noise floor of the ADC in dBm/Hz. With an IF of 244 MHz at -1 dBFS, the SNR of the ADC12DL080 is 65 dBFS or -55 dBm since full scale is +10 dBm into 50Ω. To translate into dBm/Hz, take $10 * \text{LOG} (F_s/2)$ and subtract it from -55 dBm. $10 * \text{LOG} (39 \text{ MHz}) = 75.9 \text{ dB}$, therefore the ADC12DL080 noise floor in this example is -130.9 dBm/Hz. Now if the channel bandwidth is 200 kHz, add back $10 * \text{LOG} (200 \text{ kHz})$ or 53 dB to get a noise floor of -77.9 dBm in 200 kHz, which is 22.9 dB better than the ADC by itself. Translating back to dBFS, the total SNR is 87.9 dB in a 200 kHz channel. This is similar to decreasing the resolution bandwidth on a spectrum analyzer; the noise floor has been lowered, but the ADC's resolution has not been increased.

Interfering Signals

GSM systems require the receiver to operate with signals from -13 dBm to -104 dBm when there are no interfering signals. Typical receivers need some extra margin to demodulate the received signal. This is called the Carrier-to-

Interferer (C/I) ratio and is 9 dB for GSM. This means that the noise floor must be below -113 dBm, resulting in a dynamic range of greater than 100 dB, which is more than our ADC can provide. Normally a Variable Gain Amplifier (VGA) is added to the system to scale the input signal to the ADC.

Adding a VGA works well until a large interfering signal is present. In GSM systems, this condition can occur when one subscriber is close to the basestation and one is far away. The close subscriber may actually be talking to a more distant basestation on an adjacent channel, which can block the reception of the weak signal. Hence, the large signal is known as a blocker. The blocker can be up to -13 dBm while the weak signal can be as low as -101 dBm. Considering the 9 dB C/I ratio, the overall dynamic range requirement is now -13 dBm - (-110 dBm) or 97 dB with a blocking signal. If the blocker causes the VGA gain to decrease to prevent clipping the ADC input, the weak signal can be lost in the noise.

The channel filter in front of the ADC will reduce the level of the blocking signal, but the ADC will still operate near full scale. Clock jitter and the large signal will degrade the SNR causing a loss of sensitivity if the filter rejection of the blocker is not sufficient.

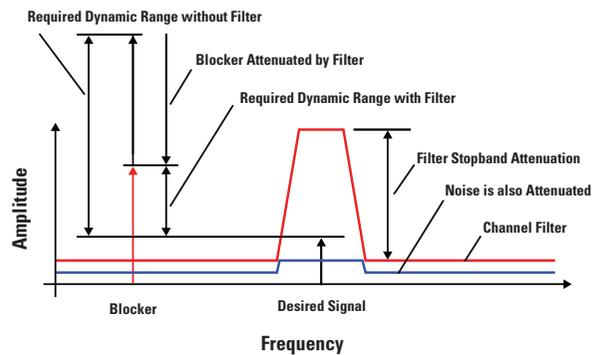


Figure 3. Channel Filter

Summary

High-speed ADCs such as the ADC12DL080 combined with a digital tuner such as the CLC5903 can simplify receiver design and provide excellent performance for high dynamic range signals. More information on this topic is available in the user's guide for the CLC-LDRCS-PCASM evaluation board at www.national.com/store#DataAcquisition. ■

Featured Products

Differential, High-Speed Op Amps

The LMH6550 and LMH6551 are high-performance voltage feedback differential amplifiers. The fully differential topology allows balanced inputs to the ADCs and can be used as



single-ended-to-differential or used as differential-to-differential. These amplifiers also have the high speed and low distortion necessary for driving high-performance ADCs, as well as the current-handling capability to drive signals over balanced transmission lines like CAT-5 data cables.

With external gain set resistors, the LMH6550/51 can be used at any desired gain. Gain flexibility coupled with high speed makes these amplifiers suitable for use as IF amplifiers in high-performance communications equipment.

LMH6550 Features

- 400 MHz, -3 dB Bandwidth ($V_{OUT} = 0.5 V_{P-P}$)
- 90 MHz, 0.1 dB Bandwidth
- -92/-103 dB HD2/HD3 at 5 MHz
- 3000 V/ μ s Slew rate
- -68 dB Balance error ($V_{OUT} = 1.0 V_{P-P}$, 10 MHz)
- 10 ns Shutdown/enable

LMH6551 Features

- 370 MHz, -3 dB Bandwidth ($V_{OUT} = 0.5 V_{P-P}$)
- 50 MHz, 0.1 dB Bandwidth
- -94/-96 dB HD2/HD3 at 5 MHz
- 2400 V/ μ s Slew rate
- -70 dB Balance error ($V_{OUT} = 0.5 V_{P-P}$, 10 MHz)
- Single +3.3V, +5V, or \pm 5V supply voltages

The LMH6550/51 are ideal for use in applications requiring a differential A/D driver, video twisted pair, differential line driver, single-ended-to-differential converter, high-speed differential signaling, IF/RF amplifier, or SAW filter buffer/driver.

The LMH6550/51 are available in the space-saving SOIC-8 and MSOP-8 packaging.

For FREE samples, datasheets, and more, visit www.national.com/pf/LM/LMH6550.html
www.national.com/pf/LM/LMH6551.html



ADC14L020/40 14-Bit, 20 and 40 MSPS ADCs

The ADC14L020 and the ADC14L040 are low-power, monolithic 14-bit 20 and 40 Mega-Samples Per Second (MSPS) Analog-to-Digital Converters (ADC). These ADCs provide excellent dynamic performance and 150 MHz full-power bandwidth. The ADC14L020 achieves 12.0 effective bits and consumes 150 mW at 20 MSPS. The ADC14L040 achieves 11.9 effective bits and consumes 235 mW at 40 MSPS. The power-down feature on both products reduces power consumption to 15 mW.

The differential inputs provide a full-scale differential input swing equal to two times the reference voltage with the possibility of a single-ended input. Duty cycle stabilization is applied to the input clock to provide an internal duty cycle of 50%. The output data can be set for offset binary or two's complement.

To ease interfacing to lower voltage systems, the digital output driver power pins of the ADC14L020/40 can be connected to a separate supply voltage in the range of 2.4V to the analog supply voltage.



Features

- Single 3.3V supply operation
- Outputs 2.4V to 3.6V compatible
- Low power consumption
- Duty cycle stabilizer
- Internal reference
- Power-down mode

The ADC14L020/40 provide an impressive 74 dB SNR and 93 dB SFDR at Nyquist while consuming just 150 mW, making them ideal for portable medical imaging, instrumentation, home gateways, and communications receivers. These converters are available in LQFP-32 packages and operate over the industrial temperature range of -40°C to +85°C.

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