

***Supervisory IC Protects System Against Overvoltage Conditions***



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# Technology Edge

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## Supervisory IC Protects System Against Overvoltage Conditions

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Careful design limits overvoltage on the supply input of integrated circuits, and avoids compromising an IC's specifications. Overvoltage damage can cause an immediate failure, or accelerate an early-life reliability failure. Older technology CMOS circuits can withstand up to 6 V without damage. But some present-day circuits on low-voltage/high-speed processes may not tolerate even 5 V.

Most often, overvoltage damage occurs when integrated devices (transistors or resistors) go into breakdown, which produces high current flow. The product of high current flow and overvoltage may exceed a given device's internal power-dissipation limit. Even a temporary pulse of heat can send internal temperatures well beyond the specified maximum junction temperature. The resulting thermal overstress could degrade or damage multiple integrated devices and possibly shift the IC's specifications.

One approach to an over-voltage protection circuit uses a combined PMOS switch and supervisory circuit to disconnect the main circuitry (Fig. 1). The R1-R2 divider sets the desired overvoltage trip point. In addition to opening and closing switch M1, IC2 illuminates LED2 during an overvoltage condition, flashes LED1 to indicate "good" power, and continuously illuminates LED1 to indicate undervoltage. The following equation controls the overvoltage set point:

$$V_{IN}(\text{overvoltage}) = 1.225 V \times (R1 + R2) / R2.$$

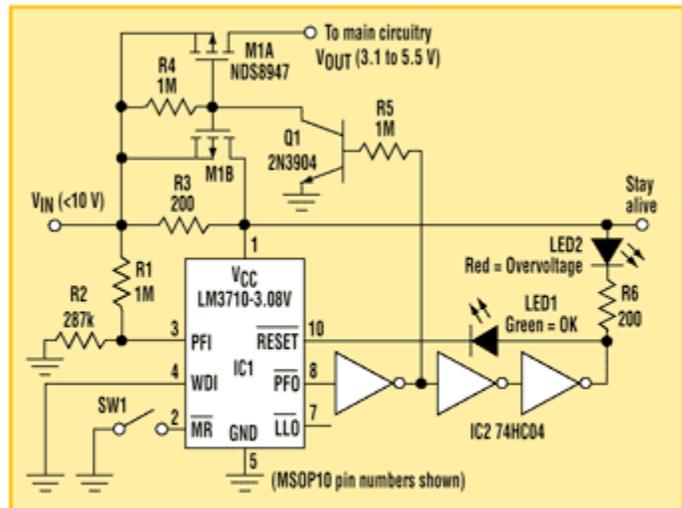
The R1-R2 resistor divider, along with IC1's PFI input threshold of 1.225 V, set the fault level. When  $V_{IN}$  exceeds the overvoltage set point, IC1's PFO pin indirectly drives LED2 continuously, and opens switch M1. IC2 inverts the signal from PFO and isolates Q1's input from LED2. With LED2 being turned ON, the stay-alive voltage at IC1's  $V_{CC}$  input

is clamped to below 6 V by the forward voltage of LED2 and the voltage drop across R6. Other critical circuits, including IC2, can be connected to this node as long as their current requirement is less than 1 mA.

R3 isolates  $V_{IN}$  from the stay-alive voltage with M1 open. It must be small enough to keep LED2 illuminated.

With  $V_{IN}$  below the overvoltage level and in the "good" range, LED1 blinks repetitively. IC1's internal reset timeout pulses LED1 ON for 200 ms, and pulses OFF for 25.6 s. This long OFF duty cycle saves power. IC1's watchdog timeout period controls LED1's OFF period by monitoring transitions at WDI. If there are no voltage transitions at WDI, then IC1's reset engages.

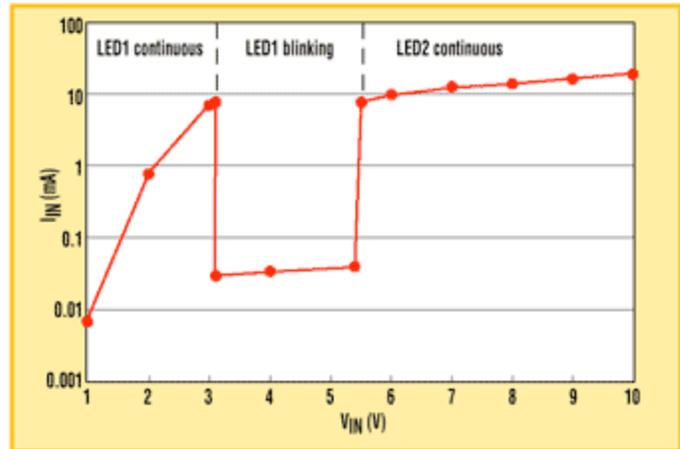
The WDI input in Figure 1 is grounded to prevent any transitions. So the reset timeout and watchdog timeout of IC1 form two one-shots that produce a repetitive pulse train. The power dissipation of this flashing technique is the ratio of these two time periods, producing a low current drain on  $V_{IN}$ . Pressing the momentary switch, SW1, short cycles the 25.6-s pause between LED1 flashes. This will also illuminate LED1.



**1. IC1 and a dual PMOS transistor form an overvoltage disconnect. This prevents harmful voltages from destroying low-voltage ICs that are connected to the main-circuitry power port.**

During the brief time before  $V_{IN}$  reaches the "good" level, LED1 remains ON continuously. This serves as an undervoltage indicator. Figure 2 shows the circuit's current-voltage waveform.

Adjust R4, R5, and R6 to meet your specific application temperature range and component variations. R4 is a pullup resistor across M1's VGS. R5 is Q1's base-current limiting resistor, while R6 is LED2's forward-current limiting resistor. The reset output of IC2 will restrict LED1's current to about 8 mA.



**2.** The power-saving mode blinks LED1 when  $V_{IN}$  is between 3.1 and 5.5 V.

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