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Abstract

To protect capital investment, improve operating efficiency and reduce damage and injury caused by electrical faults and outages, power protection systems are being built into a wide range of industrial and commercial power networks. A power protection system is a remote device located outside of a building that monitors the power line for surges. If a surge is detected, information will be sent to a control office and some action will be taken. These products must have powerful signal-processing capability, a rich set of I/O peripherals to support high data rates, an intuitive graphical user interface (GUI), low power consumption to assure a long lifetime in a high-heat environment and high-quality baseline software to speed system design and time-to-market. As in most applications, system designers benefit when much of this functionality is integrated into a single chip. However, making a cost-effective, easy-to-use single-chip solution can be a challenge so Texas Instruments Incorporated (TI) created a system architecture, design methodology and system-on-chip (SoC) solution based on its OMAP-L13x processors.

Power Protection System: Design considerations for cost-effective, easy-to-integrate SoC-based power line protection equipment

Power interruptions have many causes including load imbalance, component damage and unanticipated spikes in demand. Failures can be costly in terms of capital investment, operating efficiency and even injury. To minimize the impact of outages, power protection systems are needed to monitor and analyze the power network in real time and advise human operators of network abnormalities that can potentially lead to failure.

Power protection systems must collect and analyze large amounts of widely varying analog data in real time. Data analysis requires a powerful digital signal processor (DSP) core. Some of the capabilities required include harmonics analysis, measuring the static differences for voltage and current, peak voltage/current fluctuation, power factor calculation and phase asymmetry detection.

Kernel algorithms for analyzing these parameters include Digital Fourier Transform (DFT), Fast Fourier Transform (FFT), Digital Wavelet Transform (DWT) and Finite Impulse Response (FIR) filtering. The DSP also needs to support floating-point arithmetic due to the wide data range during calculation.

Although signal processing is a key requirement, the CPU core has to manage all the I/O activities and the GUI, which are traditionally MCU functionalities. As a result, a dual-core CPU is the most cost-effective solution to guarantee the real-time property.

The SoC also has other important functions to perform including data storage and high-speed data communication. Figure 1 on the following page shows the functional blocks of a typical power protection system.

The blocks that involve important SoC design considerations are:

- High-speed analog-to-digital conversion is essential for this application. The A/D interface needs to be flexible to support various data bus, clock control and frequency measurement signals.
 - The data interface can either be serial or parallel depending on factors such as cost, precision requirement, speed requirement, implementation complexity and the user's familiarity. Serial interfaces are typically SPI or UART but there is no standard for parallel A/Ds. Customers can choose multiple GPIO pins or an FPGA.

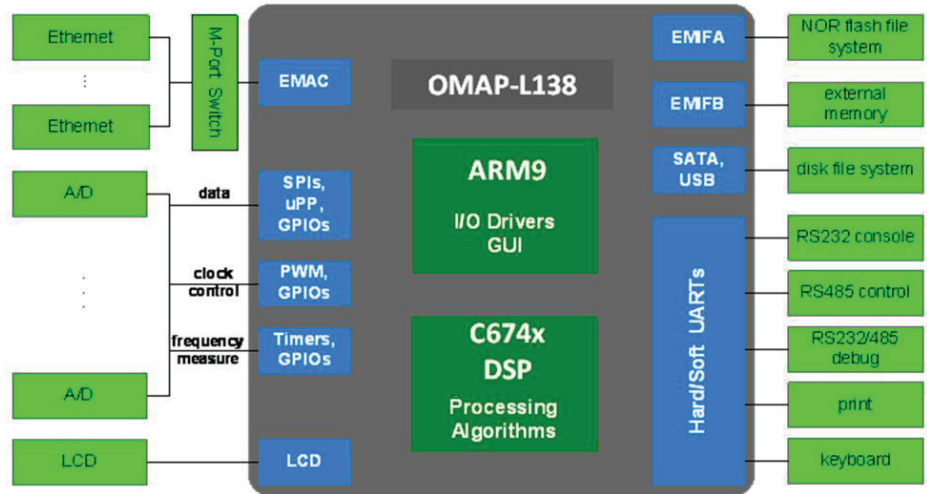


Figure 1. Power protection system block diagram

- The clock control interface is best realized by on-chip PWM. Otherwise a GPIO pin with timer and software involvement can realize the same function.
- The frequency measurement interface requires both GPIO and timer. The clock pulse from A/D is captured by GPIO and compared with the timer counter periodically to ensure the A/D clock is in synchronization with the processor.
- A Flash-based file system stores both the raw and output data after analysis. The reliability and speed of NOR Flash make it a good choice. In some applications, a disk-based backup system is also desirable.
- Multiple UART-based serial interfaces are needed for the terminal console, debugging port, external device control (over RS-485 bus), printer port and keyboard. Although customers typically need a subset of functions, SoCs must be designed to handle the entire application domain.
- Multiple Ethernet connections are required for fault-tolerance purposes and to handle communication between the equipment and the central office. Data traffic follows independent paths to avoid failure after a component failure or network storm in one path.
- The LCD display usually requires a 16-bit data interface (RGB565 format) at VGA (640×480) resolution.
- An external memory interface is needed to handle data that exceeds the capacity of on-chip memory. The interface should support popular interfaces including SDRAM, DDR and DDR2.
- The dual-core CPU was discussed earlier.

Chip design challenges

Such a high-performance complex system poses several challenges for chipmakers.

- The large number of possible peripherals would increase the die size and the number of exposed pins to the extent that vendors could not create an SoC at acceptable cost. Two external memory interfaces and

32 GPIO pins alone would require more than 90 pins. Additional pins would be required to implement FPGA and LCD interfaces as well as UARTs and SPIs and power pins.

- The data rate traffic from the A/D interface can exceed 50Mb/s and the data rate pumping to LCD can be as high as 35Mb/s. The Ethernet ports might hit 60Mb/s when an alarm is encountered.
- Since software is a major consideration for design teams, it must also be a major concern of semiconductor companies. Sophisticated evaluation modules, development tools and libraries can speed a design tremendously. The operating system (OS) is equally important because design teams rightfully want to leverage their legacy code. As a result, IC companies support various OSes as much as possible. Real-time capability is another key factor because power protection systems require it. Cost is also important and most customers also like to see a large set of open source code/applications for the OS. They also want a clear roadmap to assure them that the OS will evolve with technology.

TI's SoC solution

Power protection systems have contradictory requirements because on one hand they require a pre-emptible, real-time OS for receiving and monitoring data. This set of requirements is best served by a thin client. But tasks such as file system maintenance, GUI control and I/O work best with a full-featured, non-pre-emptible OS. Trying to accomplish all the tasks with a single core adds a great deal of complexity to the software. On the other hand, TI's dual-core architecture – the OMAP-L13x processor which contains a TI TMS320C674x DSP core and an ARM9™ core – neatly resolves these issues.

Real-time tasks are partitioned to DSP and its OS – TI DSP/BIOS™ Real-Time Kernel – and is free. Non-real-time tasks are partitioned to the ARM® core. Widely accepted by the industry, it supports many popular OSes, including Linux, Windows® Embedded CE and VxWorks. Its flexibility enables customers to quickly port legacy applications/frameworks to the new hardware platform.

TI has also brought innovative solutions of on-chip data management. The high data rates typical of power network monitoring make it difficult for CPU cores to handle data movement. Instead, TI's solution utilizes the following enhanced DMA technology:

- Synchronizes directly with all the peripherals on chip.
- Supports multiple data streams (channels) simultaneously.
- Supports programmable indexing and can transfer two-dimensional or three-dimensional data arrays.

High data rates also strain the commutation links between the DMA and on-chip peripherals. TI's solution reduces overhead by adding FIFO to all critical peripherals. This reduces synchronization frequency from 1:1 to 1:M where M is the FIFO size. The UART baud rate that could sustain a bit rate of around 115.2K without FIFO, soars to 3M by adding a 16-Byte FIFO.

Inter-processor communication

Using two cores complicates the SoC design to the extent that the cores must communicate reliably and in real time. Of the variety of approaches available (see Figure 2), TI has chosen a shared-memory architecture shown in Figure 2(b). Unlike the direct-link architecture shown in Figure 2(a), the shared memory architecture does not require FIFOs in each core and avoids the cost and communication overhead imposed to be sure the FIFO is not overwritten.

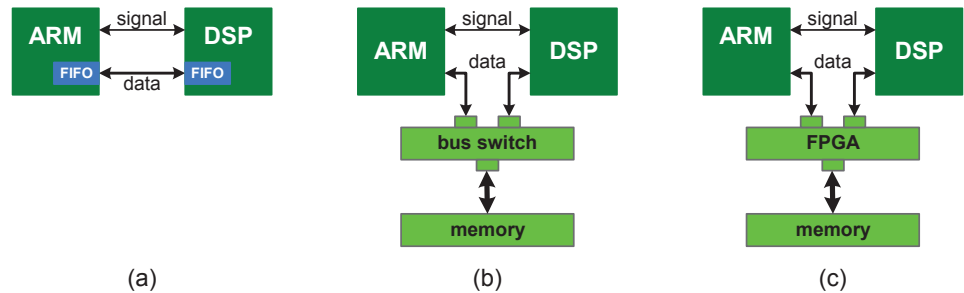


Figure 2. Inter-processor link options

TI guarantees the data throughput at the bus switch by carefully designing the bus protocol. The shared memory architecture is also scalable: adding one more shared slave device(s) (memory or peripheral) or one more master(s) (CPU core or DMA) is as simple as adding a port to the bus switch.

An undesirable option is a two-processor solution with an FPGA to control the traffic as shown in Figure 2(c). Using the FPGA can be expensive and painful, and high data rate is difficult to be realized.

On-chip memory architecture

Designs that depend on solid real-time performance usually require a large on-chip memory. Off-chip accesses are slower, which impacts interrupt responses, and adds worst-case execution time and even makes the set of real-time tasks un-schedulable.

On the other hand, on-chip memory can be expensive and utilizing a large array of level-1 RAM might even be impossible due to long address decoding time or high power consumption. TI's approach is to implement two or three levels of memory hierarchy on chip to allow the user to tradeoff speed vs. size. DSPs can integrate 64KB – 128KB of L1 memory, 128KB to – 2MB of L2 memory and even some L3 memory. The on-chip memory is flexible enough to allow engineers to choose various partitions between RAM and cache, and the cache controller automatically maintains CACHE coherency across all L1 and L2 levels.

Power management

Power protection systems must run continuously for 10 years in an industrial environment in which operating temperatures are already high. This makes power consumption critically important. Compared to a system-on-package (SoP) or a dual-processor solution, an SoC typically consumes much less power.

TI has kept both active and static power consumption at very low levels for its SoC solution. Fabricating in a 65-nm process reduces transistor size and active power but tends to increase static (leakage) power consumption. The effects of leakage power have been mitigated by these techniques:

- Dynamic voltage and frequency scaling (DVFS): Frequency and voltage can be scaled just enough by the application to meet the real-time requirement. This reduces the percentage of CPU idle time and saves energy.
- Clock gating: Turning off the clock of the unused peripherals to save power from unnecessary clock toggling.
- For certain high-power components on the chip, i.e., USB PHY, the SoC can be carefully designed to allow cutting off the power supply to the component.

Peripherals

TI's SoC solution integrates the following peripherals:

- Three UARTs for control, terminal access, printer access, debug and user-selected functions.
- Two SPIs to connect serial A/Ds.
- Two external memory interfaces (EMIFs) – one for external RAM and the other for NOR memory.
- Eight timers – at least two timers for OS timestamp operations and the others for frequency measurement/synchronization
- Two USB and two MMC/SD interfaces for external disk(s)
- One LCD for display
- At least 32 GPIOs which can be used for connection with parallel A/D, A/D control, frequency measurement, etc.
- One Ethernet MAC – a virtual LAN (VLAN) technology which will be described below can emulate multiple Ethernet ports on a single EMAC.
- One – two PWMs to control A/D.
- One universal parallel port (uPP) which offers high-speed connection to two data converters up to 16-bit data width and seamless bi-directional interface to FPGAs.
- One Integrated Serial Advanced Technology Attachment (SATA) which offers high-speed interface to data storage devices at 1.5 Gbits/sec and 3.0 Gbits/sec.

Although the peripherals listed above are sufficient to satisfy 90 percent of TI's customers who design power protection systems, there are always instances that require more. Interestingly, simple peripherals are usually all that is required. SoC designers realized that the behavior of an UART or SPI is simple enough so that it can be emulated by software driving unused pins. Multiple low-cost MCUs have been integrated for this function.

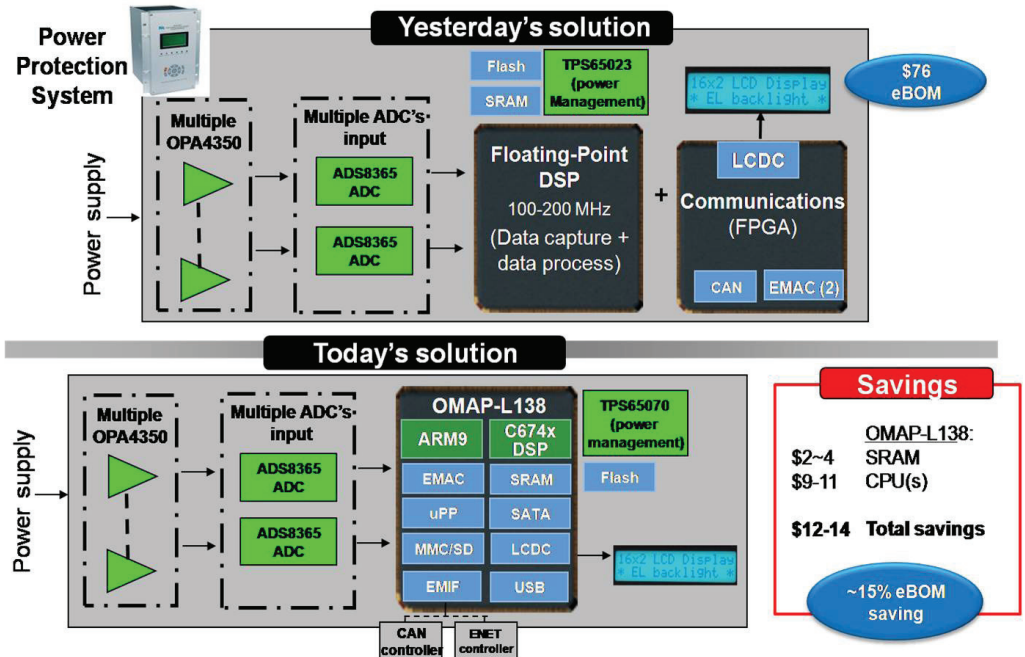


Figure 3. Before and after designs for a power protection system

Implementing virtual Ethernets

Having multiple Ethernet ports is a hard requirement for a power protection system to achieve fault tolerance. Data bandwidth, on the other hand, is not an issue because the summed bandwidth of all the Ethernet ports is not expected to exceed 60Mb/s.

Since a single 100Mb/s EMAC is sufficient, a VLAN technique is used to emulate multiple Ethernet ports. This technique avoids the expense of implementing multiple EMACs to serve multiple networks and the extended development time and cost involved in utilizing FPGA technology.

Software

TI provides and supports the following software:

- Linux kernel and associated peripheral drivers for the ARM® core
- RTOS and associated peripheral drivers for the DSP
- The inter-processor communication software between the ARM and DSP
- Microcontroller library for emulating simple peripherals
- Power management software

Software integration and application-specific algorithm development are performed by the customer but TI also provides evaluation modules and software to make that process as efficient as possible.

Conclusion Environmental factors such as global warming and economic factors such as rising energy costs and the financial implications of power outages are driving interest in power protection systems. To be cost effective, these systems should be based on single-chip solutions. TI's analysis of the required functionality has lead to a unique SoC architecture with two processor cores, a shared memory interface and several innovative capabilities such as emulating multiple virtual Ethernet ports and integration of on-chip MCUs to expand serial peripherals.

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