Integrating fixed- and floating-point capability in the same DSP core enables a fundamental change in the way algorithms for embedded systems are developed and deployed. This may sound overstated, but it is true. The amount of effort that has been spent on implementing algorithms in fixed point digital systems is enormous. The “need for speed” mandated the effort because fast floating-point DSPs simply weren’t available until now. Algorithms developed with floating-point tools like Matlab can be ported simply and easily to the DSP without a laborious conversion to fixed point. With TI’s new C66x DSP floating-point computation capabilities, most of this effort is no longer necessary.

A review of the binary representations of numbers

All digital processors, including TI’s DSPs, represent numbers in binary with a series of bits (0’s and 1’s). The accuracy with which we can represent numbers is dependent on both the number of bits used and also on the format of the representation.

Fixed-point systems use the bits to represent a fixed range of values, either integers or with a fixed number of integer and fractional bits. The dynamic range of values is therefore quite limited and values outside of the set range must be saturated to the endpoints. Fixed-point processors usually quote their 16-bit performance in terms of the number of such multiplies per second. To take full advantage of the processing capability (i.e. to get the full entitlement of the quoted performance) algorithms developed for these processors have to operate on a set of data that stays within the pre-determined range. Data sets that are unpredictable or subject to wide variation do not perform well in fixed-point implementations.

Floating-point representations provide more dynamic range by representing numbers in scientific notation, using a mantissa (or significand) and an exponent. The C66x core implements single precision floating-point operations where numbers are represented in 32 bits as: \((-1)^s \times M \times 2^{N-127}\), where S is the sign bit, M is the mantissa or significand, and N is the exponent. S is one bit, N is represented in 8 bits and M is represented with 23 bits. In this way numbers in the range \(2^{-127} - 2^{128}\) can be represented with 24 bits of precision in the significand. By contrast, a fixed-point algorithm with 16 bits can only represent a range of \(2^{16}\) values (the numbers 0 – 65535) so there is much less dynamic range inherent in the numerical representation. Floating-point representation is therefore preferred when the data sets, or the algorithms working on the data sets, are unpredictable or have wide variation in dynamic range.
range. The other important point is that the significand always has a ‘1’ as its first digit so the values always retain 24 bits of precision.

How TI innovation integrated fixed- and floating-point in a single core

The New C66x DSP Core – Figure 1 shows TI’s C64x+ DSP, the predecessor to the new C66x DSP. The core is composed of two symmetrical sides (A & B) each with four functional units. The .M unit contains the multipliers and there are four, sixteen bit multipliers in each of the .M units.

Figure 2 shows TI’s new C66x core with the same basic A & B structure of the C64x+ core. Note that the .M unit has been increased to sixteen, sixteen bit multipliers per functional unit resulting in a quadrupling of the core’s raw computational capability. The C66x DSP’s breakthrough innovation allows each cluster of four multipliers to join together to implement a single precision floating-point multiplication.
Up to eight, floating-point multiplies can run simultaneously on a C66x DSP core. Combining this with clock frequencies of up to 1.25 GHz results in the highest performance floating-point DSP in the market. Multiple C66x DSP cores have been combined to create multicore system-on-chip (SoC) devices with astonishing performance.

To achieve this optimal performance of both the fixed- and floating-point elements, TI developed new floating- and fixed-point instructions for this new C66x core, all of which are critical to efficient wireless signal processing. There have always been separate fixed- and floating-point processors due to the extra computational complexity when using floating-point notation. In fixed point, the basic operations like addition and multiplication are straightforward and simple to implement. In floating point, the basic operations require more work. Consider multiplying two floating numbers:

\[(M_1 \times 2^{N_1}) \times (M_2 \times 2^{N_2}) = (M_1 \times M_2) \times 2^{N_1 + N_2}\]

Note that the exponents need to be added together and the mantissas need to be multiplied. Then the resulting \((M_1 \times M_2)\) value needs to be scaled to 23 bits, which may require a change to the exponent value as well. There are additional operations required for all the basic operations when using floating point.

This added complexity of floating-point computation is the reason why many algorithms use only fixed-point representations and fixed-point math. Embedded processors can run fixed-point math faster and in many instances, fixed-point algorithms are all that is required. For example, a C66x DSP core can execute 16 fixed-point multiplies or four floating-point multiplies per cycle.

To achieve this optimal performance of both the fixed- and floating-point elements, TI developed new floating- and fixed-point instructions for this new C66x DSP core, all of which are very important to wireless base station signal processing. The floating-point instructions, FP_i, include:

1. Single precision complex multiplication
2. Vector multiplication
3. Single precision vector addition and subtraction
4. Vector conversion of single-precision floating-point to/from integer
5. Double-precision floating-point arithmetic (addition, subtraction, multiplication, division, and conversion to/from integer) supported and fully pipelinable

The new fixed-point instructions provide for optimal vector signal processing, VSP_i, and include:

1. Complex vector and matrix multiplications, such as DCMPY for vector, and CMATMPYR1 for matrix multiplications
2. Real vector multiplications
3. Enhanced dot product calculation
4. Vector addition and subtraction
5. Vector shift
6. Vector comparison
7. Vector packing and unpacking
Although DSPs can implement fixed-point processing faster than floating-point processing, there is a price to pay in terms of development time for certain algorithms. A typical design flow for a communications system is to first develop algorithms based on computer models and use these for initial system deployments. As the deployments grow in scope and usage, engineers gather real-world data and bring this back to the lab to improve the system performance by tweaking the algorithms. These new algorithms are often developed using Matlab or other inherently floating-point tools. The challenge then lies in translating these floating-point algorithms to fixed-point algorithms while retaining the performance of both the algorithm and of the system. Unwieldy or complex algorithms can use up a disproportionate amount of system resources thereby lowering the overall performance of the system. It is not uncommon for the process of porting code from Matlab to a real system to take weeks or months when complicated processing is involved. With native floating-point support on TI’s new architecture, the entire conversion from floating point to fixed point is unnecessary. Code is easily ported from tools like Matlab using floating-point instructions on the C66x DSP and compiling directly onto TI’s DSP as shown in Figure 3.

Wireless phones are evolving into complex media platforms requiring high capacity data transmission to support streaming video and other high bandwidth applications. To meet these needs, the wireless industry is deploying new, 4G technologies like WiMAX and LTE in basestations to bring more data throughput to the end user. These 4G basestations make use of multi-antenna signal processing to improve their performance with algorithms such as MIMO and Beamforming. These algorithms typically rely on matrix inversion techniques which are inherently susceptible to the quantization and scaling problems associated with fixed point processing. Implementing these algorithms with floating point improves both the speed and the accuracy of the system, resulting in higher performance and ultimately, a better experience for the mobile phone user.
While previously we have discussed how floating-point processing takes longer since each basic math operation takes longer, this does not apply when algorithms require high dynamic range to operate. In the matrix inversion operations of 4G processing, there is no simple way to use fixed-point operations and therefore the algorithms running on fixed point processors (without native floating-point support) are basically forced to emulate floating point. Since the processor is not taking advantage of its fixed-point capabilities, these algorithms run much slower than when run using a processor that supports floating-point operations. Having native floating point on the C66x DSP removes this performance robbing encumbrance. For example, the C66x DSP core runs MIMO and other key multi-antenna signal processing algorithms 4x faster than the same algorithms running in fixed point on the C64x+ DSP.

Across mission critical applications such as defense, public safety infrastructure and avionics, floating point provides ease of development and performance lift. Not only does floating point shorten development lifecycle by being able to use code directly out of MATLAB, but also floating-point implementations of many algorithms take fewer cycles to execute than fixed-point code (such as large FFT). For example, radar, navigation and guidance systems process data that is acquired using arrays of sensors. The varying energy pattern across the many sensor elements provides the information relevant to the location and tracking of the target. This array of data must be processed as a set of linear equations to extract the desired information. Solution methods include math functions such as matrix inverse, factorization, adaptive filtering, etc. The greater precision of output required, along with the need for larger dynamic range, make these functions perform significantly better on a 1.25-GHz floating-point engine like the C66x. In addition the SIMD enhancements and the 1.25-GHz 32 MAC/cycle fixed-point capability of the C66x, give designers tremendous flexibility in finding the right fixed- and floating-point combination to suit their applications.

Image recognition, used for medical imaging such as ultrasound, as well as machine vision and industrial automation, also requires a high degree of accuracy and thus benefits from floating point. In ultrasound, signals from sound sources must be defined and processed to create output images that provide useful diagnostic information. The greater precision, afforded by the C66x ISA, enables imaging systems to achieve a much higher level of recognition and definition for the user.

A well known application area for floating-point use is in audio processing, where a high sampling rate, coupled with very tight latency requirements, can force filtering and other noise reduction algorithms towards the higher precision and larger dynamic range provided by floating point. Wide dynamic range also plays a part in robotic design. Unpredictable events can occur on an assembly line. The wide dynamic range of a floating-point DSP, enables the robot control circuitry to deal with unpredictable circumstances in a predictable manner.
Conclusion

TI’s new C66x core enables an innovative category of DSP-based embedded processors and SoCs where there is no longer a trade-off between choosing a fixed-point processor or a floating-point processor. This revolutionary step forward will fundamentally change the way algorithms are designed and developed for real-time systems, allowing system developers to build new and differentiated solutions quickly and easily.

For more information visit www.ti.com/c66multicore
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