

Introduction

In the last decade we have experienced huge changes in the way we communicate. We have moved from fixed and wired plain old telephone service (POTS) to briefcase-sized mobile phones, and more recently to smartphones. Behind the scenes we have moved seamlessly from the circuit switched technology of the public switched telephone network (PSTN) and early cellular networks to the packet switched technologies of the Internet. The growth in user services has placed pressure on service providers to support new applications (Figure 1) while maintaining their traditional quality. These services are supported by next-generation components and features in the backbone or transport networks. This makes the processing requirements of the backbone telecommunications networks a perfect example of the forces which are creating the need for multicore processor architectures.

Fig. 1 – Services carried over the telecommunications network have changed dramatically over the last two decades.

Historically, certain functions or applications within the network have been served by specific microprocessors. Digital signal processors (DSPs), for example, are ideally suited for processing both voice and video signals. In addition, DSPs are the workhorse processors for wireless connectivity and, as the complexity of network standards has rapidly increased, they have taken on an expanded role by performing more of the processing related to wireless protocols. Network processors have been architected to provide high packet throughput for real time communications and serve as the anchor for packet processing, which keeps packets moving through the network. Host processors or general purpose processors help operators manage and control the network, as well as collect the fees for their services. All of these processor types are now migrating toward multicore architectures.

The role of multicore in the evolution of communications

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White Paper

Voice Services

Voice, Video Services

Multi Service Delivery Platform

Public Switched Telephone Network (PSTN)

PSTN, VoIP, and IP Networks

Voice, Data, and Video over IP Networks
As the computing needs of each processor type grew with each passing year, the first response of the industry was usually to increase the clocking frequency of each processor’s core. But as processor frequencies increased, other issues such as device power, the inability to find sufficient parallelism in processing tasks and lagging memory bandwidth became obstacles to further advancements.

Increasing the clock frequency was often accompanied by a move from one chip fabrication process node to a new more advanced process that would enable smaller transistors as well as higher clock speeds. Silicon vendors often took advantage of these migrations to each successive process node to integrate new functions and drive down costs. Among the many new capabilities enabled by these advancements was a rapid expansion of network capability while maintaining affordability for consumers. The new capabilities took on many forms, depending upon the specific application. In telecommunications network equipment, one example of this is the integration of certain interfaces to peripheral input/output (I/O) technologies within the processor to accommodate Internet Protocol, Ethernet switching, Serial RapidIO®, PCI Express (PCIe) and others. For base station applications, the consolidation of functionality from multiple distinct devices into the prime processing device has often meant the elimination of expensive FPGAs or companion processors. This has resulted in a significant reduction in costs and power consumption.

Network content has had a significant impact on processor architecture over the past several years and will have an increasing influence in the coming years. This is especially true for DSPs. The traditional role of the DSP is to convert legacy circuit switched voice frames into packets suitable for transport on a packet network, convert voice from analog to digital signals, and transcode between the various voice encoding methods. With the introduction of digital video to the telecommunications network -- and especially high definition video -- the processing demands that are being placed on a DSP exceed the capabilities of a single DSP core. Multiple cores are now needed to process a single video stream. As more and more complex applications are deployed on the network, DSP architectures must be enhanced to accommodate increased network traffic and the more complex algorithms required by multimedia applications.

While network traffic has been exploding (Figure 2), the capital expenditures (capex) by service providers to expand network capacity have remained relatively the same year-over-year (Figure 3). One conclusion that could be drawn from these figures is that while the capex of carriers will remain flat, the percentage of capex likely to be spent on multimedia applications will have to increase dramatically to accommodate the significantly higher multimedia traffic on the network. In other words, multimedia processing requirements in the network will increase significantly over the next several years and this is another force behind the drive toward multicore DSPs.
The role of multicore in the evolution of communications

April 2011

Texas Instruments

Mobile and video traffic estimates

2009

- 40% video
- 90 PB/month
- 7M paid video subscribers

2014

- 66% video
- 3600 PB/month
- 700M paid video subscribers

10x growth of Internet

39x growth

Fig. 2 – Expansion of network traffic 2009-2014 from Cisco’s virtual networking index

Service provider capital expenditures worldwide

Capex-to-revenue ratio

Avg Capex in $U.S. billions

2010 2011 2012 2013 2014

Fig. 3 – Infonetics Research, service provider capex, opex, ARPU, and subscribers, Nov. 2010
Similarly, in wireless networks, with each evolutionary generation of the network, service providers have increased bandwidth capacity to satisfy the growing demand of consumers for the content traveling over the network. In the cellular network the role of the DSP has been expanded to serve advanced scheduling algorithms that maximize spectral efficiency as well as process signals to and from Multiple Input, Multiple Output (MIMO) antenna arrays, which provide higher user bandwidth without compromising how users experience network content.

Influences outside of the telecommunications industry are also being felt. Applications such as radar, medical imaging, mission critical and several others are now increasingly looking at multicore processors to satisfy the growing processing demands of their applications. Over time, these diverse applications will likely influence future device architectures.

The telecommunications industry has actually been ahead of others in some respects. One example is the inclusion in network equipment of chips that contain different types of processors or processing cores. Both homogeneous devices, which contain a single type of processing core, and heterogeneous devices, which contain diverse types of processing cores, are finding their way into the network. Homogenous chips are often classified as general purpose, network, DSPs and others. Heterogeneous processors are most often a system-on-chip (SoC), which can contain a mixture of core types and/or coprocessors. Coprocessors are usually defined as a hardware-implemented algorithms aimed at providing a specific, well defined function. Coprocessors are typically implemented for functions that are not likely to change over time, such as certain cellular signal acquisition techniques or crypto algorithms.

Today many heterogeneous devices provide some type of network encapsulation (protocol overhead), control plane functions or other functions that allow for a more compact and efficient solution. For example, TI’s TMS320C66x multicore DSPs for the base station marketplace have implemented an Ethernet switch and packet coprocessor on-chip, while the TMS320C6670 radio SoC features various coprocessors associated with cellular base stations.

One of Texas Instruments’ first multicore DSPs was the TMS320C80 introduced in 1995. The TMS320C80 had four parallel processors, one master processor with a floating point unit, one video controller and a transfer controller. This processor was targeted at video applications. Later, in 1998, the two-core TMS320C5420 was introduced. These multicore processors were ideally suited to the video and voice processing requirements of the time. Since then TI’s product line has reacted to demands for increased processing power and today it now includes several eight-core devices. In addition, TI has launched its innovative KeyStone multicore architecture, which simplifies the development of application-centric multicore devices that can more effectively meet today’s computing needs.
The KeyStone multicore architecture includes an enhanced inter-processor block communications capability, and reduced memory access latencies. It enables access to external processors via a high-speed serial interface. Also incorporated in the architecture is TI’s Multicore Navigator, which is comprised of more than eight thousand queues for unhindered communications between processor cores. For example, a fast direct connection may be established between a processor core and an I/O peripheral such as an Ethernet interface, between several processor cores or between memory and a peripheral. Low latency access to memory is provided by enabling direct access between each core and memory. Another benefit of this is increased data transfer speeds across the switching fabric since this removes traffic from the fabric. In cases where an external auxiliary processor is needed to complete a solution or a second similar device is required, the high-speed 50 gigabaud HyperLink 50 serial interface is provided. In essence, this interface allows the creation of clusters of processing devices. These and other architectural enhancements are aimed at increasing multicore efficiency and providing industry-leading solutions. They also lay a solid foundation for today’s multicore tools and programming aids.

To take full advantage of all of the capabilities of these multicore devices, a comprehensive, fast and efficient software development environment is a prerequisite for developers. A complete software ecosystem is composed of tools for software design, development and debug, and provisioning software that facilitates the migration of the final product from the lab into field deployment. TI provides a Multicore Software Development Kit (MCSDK) that incorporates all of these functions (Figure 4).

![Fig. 4 – TI’s multicore software development kit](image-url)
Moore’s Law is often cited in the semiconductor industry. It is based on the observation that the density of transistors in silicon has consistently increased over time. One could argue that the various processor technology innovations over the past several generations of devices have contributed to sustaining Moore’s Law. An interesting aspect of realizing these gains has been the various advancements that semiconductor manufacturers have made to keep pace with Moore’s Law. One could argue further that the introduction of the KeyStone architecture has allowed the industry to realize processor gains much faster than those that were accounted for in Moore’s Law. Recently introduced devices based on TI’s KeyStone architecture have shown that it is possible to make huge leaps in performance by integrating accelerating coprocessors onto a SoC. This technique enables performance gains that are independent of new fabrication processes and increasing transistor density, which is what Moore’s Law is based on. This is exciting for the future because it shows that the combination of advanced multicore architectures coupled with intelligently integrated and application-targeted accelerators can extend performance gains beyond the limits imposed by the physics of transistors.

Multicore driven

A single core can adequately process multiple voice channels. In order to scale to today’s core network densities thousands of channels must be processed per device. For voice applications, the challenge is to schedule or assign channels to cores and interconnect cores in order to facilitate conferencing and other applications. On the other hand video applications require that multiple cores be configured to manage a single channel. These are but two extremes in the traditional multicore application set. When we then consider wireless baseband applications which have begun to incorporate application centric acceleration we are only beginning to scratch the surface of what lies ahead. In addition, as DSP technology is deployed in broader markets for more diverse applications many new and exciting innovations can be anticipated. TI’s vast experience innovating multicore devices is unrivaled in the industry. The KeyStone architecture and extensive software tools are examples of how TI is leading the industry and developing innovative solutions that address today’s and tomorrow’s processing needs.

More information

For more information about TI’s KeyStone architecture and C66x multicore processors, visit www.ti.com/c66multicore
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